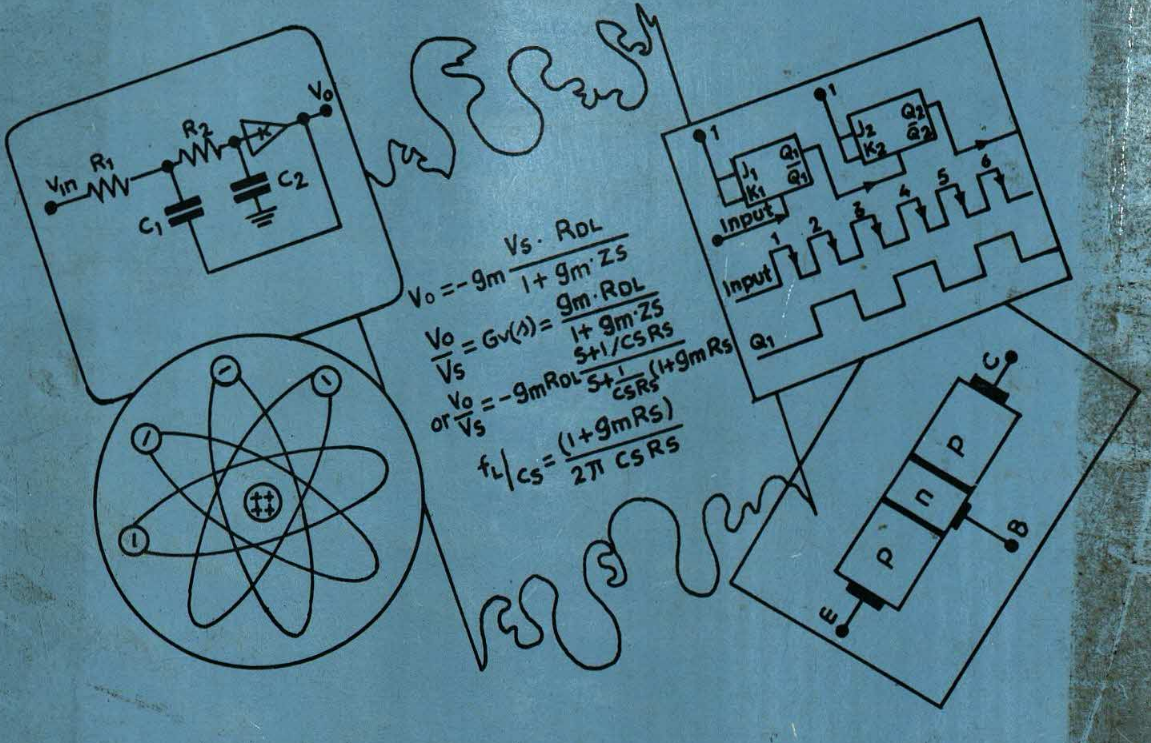
M. N. FARUQUI/S. L. MASKARA

Basic Electronics


Vin
R1
R2
C1
C2
K
Vo
Vo = -gm Vs · RDL / 1 + gm·ZS
Vo/Vs = Gv(s) = gm·RDL / 1+ gm·ZS
or Vo/Vs = -gmRDL S+1/CSRs / S+1/CSRs (1+gmRs)
fL|CS = (1+gmRs) / 2π CSRs
1
J1
K1
Q1
Q̄1
J2
K2
Q2
Q̄2
Input
1
2
3
4
5
6
Input
Q1
C
p
n
p
B
E

BASIC ELECTRONICS

M.N. FARUQUI

and

S.L. MASKARA

[illegible]

Indian Institute of Technology, Kharagpur

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PREFACE

Growth in electronics has been phenomenal and this in turn has changed the life style of people. The ease, precision, sophistication and flexibility provided by electronics in all kinds of modern systems such as communication, computer, control, automation and entertainment has made it a very important subject of study for engineers of all specialisations. Electronics has, therefore, been made a core subject in engineering curricula of all disciplines including those not specialising in Electrical Engineering.

This book on 'Basic Electronics' has been written as a text book fulfilling the needs of first year engineering curriculum. It aims at developing fundamental concepts, imparting a basic knowledge of the working of devices and explaining how the devices are used in circuits and systems. Any student having a background of Physics and Mathematics at the Higher Secondary level and an exposure to one course in Electrical Circuits can use this book effectively. It is also suitable for self reading and it is hoped that the practicing engineers will find it useful for refreshing fundamentals of electronic devices and circuits.

Greater emphasis has been laid on concepts rather than rigour and analysis is included only to support the physical ideas. Quantitative treatment of circuits and devices and a large number of worked out examples have been used to illustrate the concepts. The review questions at the end of each chapter are included to help the student guage his own depth of understanding and are meant for self testing. Some problems are also included and should be worked out at home to give a good grounding of the subject.

Chapter 1 is an introduction and Chapter 2 describes some of the physics needed to understand the working of electron devices. Chapter 3 deals with devices and is one of the most important chapters in the book. It describes the mechanism of operation of various electron devices. Technology of manufacture of some of the devices is given in Chapter 4. It also explains how the present ICs are fabricated. Chapter 5 introduces the idea of how a device can be represented as a circuit element. It also describes the properties and characteristics of ideal amplifiers. Once the reader understands some of the generalised circuit concepts described here, the analysis of a specific circuit will be easier to follow later on. Chapter 6 deals with amplifiers which are possibly the most important building blocks in any circuit or system. Single analysis of the operation of the amplifiers using BJT, FET and vacuum tubes, their terminal characteristics and frequency response are presented in the chapter. With this as a background, more complex amplifiers and other analogue circuits will be easier to understand.

The parameters of a device change from one unit to another and are sensitive to variations of temperature. Negative feedback is used to make an amplifier more reliable and stable against these variations and other circuit variations. Chapter 7 introduces the concept of feedback and shows how the terminal characteristics can be controlled by using feedback. With the advent of ICs many amplifiers can be packaged into a single chip as small as the size of an ordinary transistor. Instead of designing circuits around discrete devices, they are now designed functionally using Operational Amplifiers. Operational Amplifiers are described in Chapter 8 where some details of the input and output circuits and problems of stability are also discussed.

The world of Electronics itself is going through a digital revolution. Signal processing, storage, transmission and display of data have become much simpler with the use of digital technology. Very Large Scale Integration (VLSI) technology makes available large systems such as computers, communications and signal processors etc. on a single or a few chips. Chapter 9 is devoted to an explanation and description of logic and digital circuits. It explains how the devices are used to realise a given Boolean function and thereby an artithmetic (digital) operation. Sequential circuits like shift registers and counters which perform digital operations as a function of time are described in Chapter 10. The emphasis is on understanding of the underlying principles of the digital circuits.

Chapter 11 describes the generation of various waveforms like sinusoidal, triangular and pulse which are needed in all electronic systems. Finally Chapter 12 is devoted to a very essential subsystem of all electronic systems and that is the Power Supply. A brief analysis of some power supply circuits is presented. The book is concluded with a few appendices. Some experiments with details of circuits and procedures are suggested in Appendix A. Other Appendices give typical device data, physical constants and deci Bel (dB) conversion table for ready reference.

The book has more material than what can be covered in one semester. Alternative teaching programmes have been suggested and the teacher may decide, depending upon the interest of students and their requirements, the depth he can go to and the plan he wants to follow.

The subject matter of this book has been used for teaching more than 1200 engineering and science undergraduate students of all disciplines over the past three years at the first year level at the Indian Institute of Technology, Kharagpur. The students found the notes useful as a text material for the subject. We thank all the faculty members and the students for their valuable comments and suggestions. We are extremely indebted to Prof. S. Lal, former Director of IIT, Kharagpur who inspired and encouraged us to prepare this text book. We are grateful to Prof. G. S. Sanyal, Director, IIT, Kharagpur for his good wishes. We are thankful to the curriculum development cell of IIT, Kharagpur for providing financial support required for the preparation of the manuscript. Our sincere thanks are due to Prof. U. S. Bharadwaj of the Department of A.R.P., IIT, Kharagpur for his help in designing the cover. We are also thankful to Mr. K. Dutta, Mr. S. C. Dey, Mr. D. Dalui and Mr. M. Basu for their untiring efforts in typing the manuscript and preparing the drawings. Finally we thank all those who have contributed to the preparation of the book in various ways.

Nov. 12., 1984.

M. N. Faruqui
S. L. Maskara

Suggested Teaching Programmes

As has been suggested in the Preface, this book contains more material than what can be covered in a course of one semester only. Though the description of the devices and the analysis of the analogue and the digital circuits are interlinked they have been presented in a fashion which would enable the teacher to follow any one of teaching plans suggested below. In one scheme he may proceed in the conventional sequence of devices, analogue circuits and then digital circuits, as followed in the book. In an alternative scheme he may take up digital circuits immediately after the devices and cover analogue and linear circuits at the end. Either of the schemes can be followed with equal ease and facility.

Number of lectures including tutorials which can possibly be devoted to each topic has been given in the Table below. It is assumed that a total of 52 lectures plus tutorial hours are available in a semester. Two lecture plans are suggested. Depending upon the interest of the students and the requirements of a particular discipline/course, the teacher may choose either of the two plans or may draw his own plan. Some material particularly in the initial chapters may be left to the students to study at home. Important sections and subsections are mentioned in the Table.

Electronics is better understood if it is supported by experiments. The first level experiments suggested in the Appendix A are aimed at providing a 'hands on' experience to the students. The first two experiments are basically of demonstration type and are meant for familiarization with components, devices and instruments. One of the most important instruments used in the laboratory is the Cathode Ray Oscilloscope. A Section has been devoted to the description of Cathode Ray Tube in the Chapter on the devices. The students would appreciate the experiments better, if they are performed in the same order as given in the Appendix. The objectives and the procedures of an experiment may be introduced in the first hour of the laboratory class, or in the tutorial class attached to this course. The experiments on op-amps and logic circuits would create interest among the students and so they should be done first. Experiments with discrete devices such as the transistor amplifier should be done only when they are ready to appreciate the details.

TABLE OF LECTURE SCHEDULE

Chapter Number and Title	Number of lecture hours including tutorial and Important Sections.	
	Plan I	Plan II
1. Overview of Electronics	0	1
2. Phy. Prop. of Elect. Devices	4 (2.1, 2.2, 2.3, 2.4, 2.5.1, 2.5.2)	2 (2.1, 2.2, 2.3, 2.4, 2.5)
3. Elec. Char. of Electronic Devices.	8 (3.1, 3.1.1, 3.1.3, 3.1.4, 3.1.5, 3.1.6, 3.1.7, 3.2.1, 3.2.2, 3.2.3, 3.4 and 3.6)	8 (3.1, 3.1.3, 3.1.6, 3.1.7, 3.1.8, 3.2.1, 3.2.2, 3.3, 3.4, 3.6.1, 3.6.2,)
4. Technology of Devices.	2 (4.1.2, 4.2, 4.4)	1 (4.2)
5. Terminal Char. of Elect. Circuits.	4 (5.1.1, 5.1.2, 5.2.1, 5.3.1, 5.4)	4 (5.1.1, 5.1.2, 5.2.1, 5.3.1, 5.4)
6. Single State Amplifiers	8 (6.1.1, 6.2.1, 6.2.3, 6.3.2, 6.3.3, 6.5)	6 (6.1.1, 6.2, 6.3, 6.3.3, 6.5)
7. Feedback	6 (7.2.1, 7.2.2, 7.2.3, 7.4, 7.5, 7.6)	4 (7.2.1, 7.2.2, .3
8. Operational Amplifiers, their applications.	4 (8.2.3, 8.3.1, 8.3.2, 8.4, 8.5)	6 (8.2.3, 8.3.1, 8.3.2, 8.4, 8.5.1, 8.6)
9. Logic and Digital Circuits.	4 (9.1, 9.2, 9.4, 9.5, 9.6)	6 (9.1., 9.2, 9.3, 9.4.1, 9.4.2, 9.4.3, 9.4.4, 9.5.1)
10. Shift Registers, Counters and Timers.	5 (10.1.3, 10.1.4, 10.1.5, 10.1.6, 10.2, 10.3)	6 (10.1.3, 10.1.4, 10.1.5, 10.1.6, 10.2.1, 10.2.2, 10.3.1, 10.3.2, 10.3.3, 10.4)
11. Waveform Generators	5 (11.1.2, 11.1.3, 11.2.1, 11.3.1)	2 (11.1.2, 11.1.3)
12. Power Supplies	2 (12.1.1, 12.1.2, 12.5, 12.6)	6 (12.1.1, 12.1.2, 12.2, 1 .2.1, 12.2.2, 12.4.1, 12.5, 12.6)

GLOSSARY OF SYMBOLS

Symbols	*What they stand for*
A	**Ampere ; gain ; level**
$A(s)$	**generalised gain**
a, a_x	**acceleration**
A_c	**common mode gain**
A_d	**differential mode gain**
$A_f(s)$	**gain with feedback**
A_o	**constant ; nominal generalised midband gain**
B	**base terminal**
b_o	**constant**
C	**capacitor ; collector terminal**
c	**velocity of light**
D	**amount of deflection on the screen ; distortion amplitude**
d	**quantum level ; anode-cathode seperation ; deflection plate's seperation**
E	**energy ; electric field ; emitter terminal**
E_b	**anode potential**
E_F	**Fermi level**
E_g	**energy gap**
eV	**electron volt**
E_W	**work function**
E_x	**electric field intensity in x direction**
E_y	**electric field intensity in y direction**
f	**frequency**
$f(s)$	**feedback function**
$F(s)$	**feedback factor**
f_β	**frequency at which β falls by 3db**
f_c	**cut off frequency**
f_H	**higher cut-off frequency**
f_L	**lower cut-off frequency**
f_o	**midband feedback ratio**
f_r	**resonant frequency**
f_s	**unknown signal frequency**
f_T	**frequency at which gain becomes unity**
f_x	**known signal frequency**

Symbols	*What they stand for*
G_i	current gain ; input conductance
G_{ie}	external current gain
G_{ii}	internal current gain
g_m	transconductance
G_o	$\left(= \frac{1}{R_o}\right)$ output conductance
G_p	power gain
G_v	voltage gain
G_{vd}	differential voltage gain
G_{ve}	external voltage gain
G_{vi}	internal voltage gain
G_Y	transfer admittance
G_Z	transfer impedance
h	Planck's constant
h_{fe}	Small signal short circuit current gain in common emitter case $= \beta$
h_{FC}	d.c. current gain in inverse mode
h_{FE}	d.c. current gain in common emitter case
h_{11}, h_{12}, h_{21}, h_{22}, h_i, h_f etc.	hybrid parameters
$H(j\omega)$	transfer function with $s = j\omega$
$H(s)$	transfer function
Hz	Hertz, frequency unit
I	current
$i, i(t)$	instantaneous current
I_A	anode current ; current at operating point
I_{AQ}	quiescent anode current
I_a	input current in the OP-AMP.
I_{ac}	a.c. currrent
I_B	base current
I_{BQ}	quiescent base current
I_C	d.c. collector current
I_c	collector current
I_{CEQ}, I_{CQ}	quiescent collector current
I_{co}	reverse saturation current
I_{CBO}	collector current with $I_E = 0$
I_D	drain current
I_{d1}, I_{d2}	current through diodes
I_{dc}	d.c. current
I_{DSS}	drain current with $V_{GS} = 0$

Symbols	*What they stand for*
I_E	emitter current
I_L	load current
I_m	peak value of current
$I_{n'b}$	current due to n'_b electrons
I_{nc}	collector current due to n_c
I_{ne}	electron current at emitter terminal
I_o	output current
I_{pb}	hole current from base to emitter
$I_{p'e}$	current due to p'_c
I_{rms}	rms value of current
I_S	reverse saturation curren
I_s	source current
I_v	valley current
I_z	zener current
I_1	current at output port
I_2	current at input port
J	current density
K	degree Kelvin ; parameter
k	constant ; fraction ; Boltzmann const., parameter
L	inductance, distance of screen from the centre of the deflection plates
l	length of deflectron plates
mA	milli-ampere
n	number, electron carrier density
N_A	acceptor density
n'_b	thermally generated electron in the base
n_c	electrons diffused in collector
N_D	donor density
n_e	electrons injected in base from emitter
n_i	intrinsic carrier density
n_p	electron density in p material
n_t	thermally generated electron density
p	hole carrier density
P_{ac}	a.c. power
p_b	holes in base
p'_b	thermally generated holes in base
p_C	power dissipation in collector
p'_c	thermally generated holes in collector
P_D	power dissipation in the device
P_{DC}	power from the d.c. supply

Symbols	*What they stand for*
P_{dc}	d.c. power
p_e	holes injected into emitter
p_{load}	signal power in load
p_n	hole density in *n* region of a material
p_t	thermally generated hole density
P_1, P_2	power at the input and the output port
Q	operating point ; quality factor
q	electronic charge
R	resistance
R_B	base resistance
r_b, r_c, r_e	T-parameters of the transistor
$r_{bb'}$	base spreading resistance
$r_{b'c}$	base(internal) to collector resistance in the hybrid π model
$r_{b'e}$	base(internal) to emitter resistance in the hybrid π model
R_C	collector resistance
r_c	collector junction resistance
r_{ce}	collector emitter resistance in the hybrid π model
R_{CL}	parallel combination of R_C and R_L
R_D	drain resistance
r_d	small signal output resistance of FET
R_E	resistance emitter
r_e	emitter junction resistance
R_f	equivalent forward resistance of diode
r_f	forward resistance
R_i	input resistance
R_{iB}	input resistance at terminal B
R_{if}	input resistance with feedback
R_L	load resistance
R_l	resistance which accounts for the loss in inductance
R_o	output resistance
R_{oA}	output resistance at terminal A
R_{of}	output resistance with feedback
$r_o\left(=\frac{1}{h_{oe}}\right)$	open circuit output resistance
r_p	plate resistance
r_r	reverse resistance
r_s	internal source resistance
R_{SC}	current limit resistor
S	surface area ; stability factor ; signal amplitude

Symbols	*What they stand for*
s	quantum level
$s = \sigma + j\omega$	Laplace variable
S_d	deflection sensitivity
S_k	sensitivity to parameter K
T	temperature ; time period
$T(s)$	loop transmission function
t	time
T_H	number of loops which touch horizontal tangent line
T_s	time for spot to move
T_V	number of loops which touch vertical tangent line
V	voltage
v	velocity ; voltage
V_A	anode potential
V_{AQ}	quiescent anode voltage
V_a	accelerating potential, input voltage between positive and negative terminals
V_B	break-down voltage ; Thévenin's equivalent voltage at the base ; voltage at the base
V_{BE} (cut-in/ cut-off)	base emitter voltage when the transistor is in cut-in or cut-off
V_{B2B1}	voltage drop across the bar in UJT
V_{BB}	power supply in the base circuit ; plate supply voltage
V_{BE}	base-emitter terminal voltage
V_{BE} (sat.)	base-emitter voltage where transistor is in saturation
V_{be}	small signal equivalent base-emitter voltage
$V_{b'e}$	small signal equivalent base (internal) to emitter voltage
V_{BO}	Breakover or firing voltage
V_C	voltage at collector ; collector voltage with respect to ground
V_c	voltage across the capacitor, signal output at the collector ; common mode signal
V_{CC}	power supply in the collector circuit
V_{CB}	collector-base terminal voltage
V_{CE}	collector-emitter terminal voltage, collector-emitter drop
V_{CEO}	collector-emitter voltage open base
V_{CEQ}	quiescent collector emitter voltage
V_{CES}	collector emitter voltage ($V_{BE}=O$)
V_{CE} (sat.)	collector-emitter voltage when transistor in saturation
V_{DD}	drain supply voltage
V_{DS}	drain-source voltage

Symbols	*What they stand for*
V_d	barrier potential, threshold voltage across diode ; voltage across deflection plates, differential mode signal
V_E	emitter voltage with respect to ground
V_{EBI}	voltage drop (external) in UJT
v_{eb1}	voltage drop across lower portion of UJT
V_{EE}	emitter supply
V_G	grid-voltage
V_{GG}	gate supply voltage ; grid supply voltage
V_{GQ}	quiescent grid voltage
V_{GS}	gate-source voltage
V_{gs}	small signal equivalent gate-source voltage
V_L	load voltage
V_m	peak voltage
v_n	electron velocity
V_o	output voltage
V_{oA}	output voltage at A
V_P	pinch-off voltage
v_p	hole velocity
V_p	peak voltage in tunnel diode ; firing voltage in UJT ; total change in voltage across a capacitor while discharging.
V_R	reverse voltage
V_{REF}	reference voltage
V_s	source voltage
V_{SENSE}	sense voltage in OP-AMP
V_v	valley voltage in tunnel diode
V_z	zener voltage
V_1, V_2	typical voltage level at output and input terminals.
W	bandwidth
X	displacement
X_C	capacitive reactance
X_L	inductive reactance
Y	displacement, admittance
Y_I, Y_O	driving point input & output admittance
Y_1, Y_2	admittance
Z_E	impedance in emitter circuit
Z_I	driving point input impedance
Z_i	input impedance
Z_O	driving point output impedance
Z_o	output impedance

Symbols	*What they stand for*
α	current gain
α_I	current gain inverse mode
α_N	current gain normal mode
$\beta(= h_{fe})$	current gain
Δ	determinant
η	efficiency
θ	deflection
θ_1	ignition angle
θ_2	extinction angle
λ	wavelength
γ	ripple factor
μ	mobility ; amplification factor
μ_n	mobility of electron
μ_p	mobility of hole
τ	time constant
σ_n	electron conductivity
σ_p	hole conductivity
$\omega = 2\pi f$	radian frequency
$\omega_O = 2\pi f_o$	frequency of oscillation
$\omega_\beta = 2\pi f_\beta$	frequency where β falls by 3db
$\omega_T = 2\pi f_T$	transition frequency where gain equals unity
$\omega_C = 2\pi f_C$	cut-off frequency
$\varphi_1, \varphi_2 \ldots\ldots \varphi_f$	generalised voltage and or current
$\varphi_{d1}, \varphi_{d2}$	distortion voltage or current

Units

mV	millivolt
mA	milliampere
*K*Ω	kilo-Ohm
*M*Ω	mega-Ohm
μF	microfarad
cm	centimeter
μA	microampere
pF	picofarad.
dB	deci Bel

CONTENTS

Preface ... v
Suggested Teaching Programme ... viii
Glossary of Symbols ... x

I. An overview of Electronics :

1.0 Introduction ... 1
1.1 What is electronics ? ... 1
1.2 Scope of electronics ... 4
1.3 Scope of the book ... 6

II. Physical properties of electronic devices :

2.0 Introduction ... 8
2.1 Electronic structure of atoms ... 8
2.2 Formation of solid crystalline structure ... 9
2.3 Band structure and electric conduction in solids ... 12
2.3.1 Band structure ... 12
2.3.2 Electrical conduction ... 14
2.4 Intrinsic and extrinsic semiconductors ... 16
2.5 Electronic devices ... 20
2.5.1 p-n junction ... 20
2.5.2 External bias ... 23
2.5.3 Vacuum and gas diodes ... 24

III. Electrical characteristics of electronic devices :

3.0 Introduction ... 28
3.1 Semiconductor diodes ... 28
3.1.1 Rectifier diodes ... 32
3.1.2 Schottky barrier diode ... 37
3.1.3 Zener diode ... 39
3.1.4 Tunnel diode ... 41
3.1.5 Varactor diode ... 45
3.1.6 Light emitting diode ... 46
3.1.7 Photodiode ... 48
3.1.8 Solar cells ... 50
3.2 Transistors ... 50
3.2.1 Bipolar junction transistor ... 51
3.2.2 Junction field effect transistor ... 62
3.2.3 Insulated gate FET(IGFET) ... 66

3.3.4 Unijunction transistors (UJT) 69
3.3 Four layer devices 70
3.4 Vacuum tubes 75
3.4.1 Vacuum diode 77
3.4.2 Triode 78
3.4.3 Pentode 81
3.5 Cathode Ray Tube (CRT) 82
3.5.1 Electron gun 83
3.5.2 Deflection system 85
3.5.3 Screen 87
3.5.4 Deflection sensitivity 88
3.5.3 Oscilloscopes 91
3.6 Gas tubes 91
3.6.1 Hot cathode gas diode 93
3.6.2 Cold Cathode Diode (voltage regulator tube) ... 94
3.6.3 Thyratron 96

IV. Technology of devices :

4.0 Introduction 102
4.1 Preparation of semiconductors 102
4.1.1 Germanium preparation 103
4.1.2 Silicon preparation 104
4.2 PN junction formation 104
4.3 Fabrication of transistors 106
4.4 Silicon planar technology 107
4.5 Integrated circuits 110

V. Terminal characteristics of electronic circuits :

5.0 Introduction 113
5.1 Driving point transfer parameters ... 115
5.1.1 Transfer parameters 115
5.1.2 Driving point parameters 118
5.2 Ideal amplifier 121
5.2.1 Equivalent circuit of active device ... 123
5.3 Hybrid and T-parameters of transistors ... 127
5.3.1 Hybrid parameters 127
5.3.2 T-parameters 130
5.4 Frequency dependence of terminal characteristics ... 133
5.4.1 Low pass filter 136
5.4.2 High pass filter 139

VI. Single stage amplifiers :

6.0 Introduction 143
6.1 CE amplifier 145

6.1.1 Biasing of a CE amplifier 145
6.1.2 Capacitive coupling and analysis of CE amplifier ... 154
6.2 Frequency response of CE amplifier ... 162
6.2.1 Low frequency response 162
6.2.2 Effect of the emitter bypass 167
6.2.3 High frequency response 175
6.3 FET amplifier 187
6.3.1 Self bias 187
6.3.2 Modified biasing 190
6.3.3 Analysis of the FET amplifier 194
6.4 Vacuum tube amplifiers 200
6.4.1 Vacuum tube amplifier analysis 202
6.5 Emitter follower 207

VII. Feedback : ... 217
7.0 Introduction 217
7.1 Principles of feedback 219
7.2 Advantages and disadvantages of feedback ... 219
7.2.1 Desensitivity to parameter variation ... 220
7.2.2 Reduction of noise and distortion
7.2.3 Effect on the frequency response and the terminal impedance of the amplifier 223
7.2.4 Disadvantages of negative feedback ... 224
7.3 Types of feedback 224
7.4 Shunt-Shunt amplifier 226
7.5 Series-Series feedback 236
7.6 Stability and other considerations ... 242

VIII. Operational Amplifiers and their applications : ... 247
8.0 Introduction 247
8.1 Ideal operational amplifier 249
8.2 Amplifiers using op-amps 249
8.2.1 Non-inverting amplifier 251
8.2.2 Inverting amplifier 252
8.2.3 Difference amplifier 254
8.2.4 The Summing amplifier 255
8.3 Input circuit-differential amplifier ... 262
8.3.1 Common mode rejection ratio ... 264
8.3.2 Input impedance 266
8.4 Output circuits of op-amps 269
8.5 Actual op-amps 271
8.5.1 Compensation in op-amps. 273
8.5.2 Effect of stray capacitance ...

8.5.3 Other parameters of op-amps. 274
8.6 Applications of operational-amplifiers ... 275
8.6.1 Linear circuit applications 276
8.6.2 Non-linear circuit applications 287
8.6.3 Active filters 291

IX Logic and digital circuits :

9.0 Introduction 297
91 Function of binary variables 298
9.1.1 AND function 298
9.1.2 OR function 300
9.1.3 NOT function 300
9.1.4 NAND function 301
9.1.5 NOR function 301
9.1.6 Ex-OR function 302
9.2 Boolean theorems 303
9.3 Binary numbers 307
9.3.1 Conversion from decimal to binary number system ... 308
9.3.2 Binary arithmetic 309
9.4 Transistor as a switch 314
9.4.1 Transistor at cut-off 315
9.4.2 Transistor in saturation 316
9.4.3 Inverse mode operation of the transistor ... 317
9.4.4 Transistor switch in a logic gate ... 319
9.5 TTL gates 320
9.5.1 TTL integrated circuit gates 321
9.6 CMOS gates 325
9.6.1 CMOS NAND and NOR circuits ... 327

X. Shift registers, counters and timers

10.0 Introduction 333
10.1. SR Flip-Flop 333
10.1.1 NAND gates in SR Flip-Flops 334
10.1.2 Clocked flip-flop 336
10.1.3 J. K. Flip-flops 338
10.1.4 Master-slave flip-flop 339
10.1.5 JK Master-slave flip-flop 341
10.1.6 D Flip-flops 342
10.2 Shift registers 344
10.2.1 Serial shift register 344
10.2.2 Parallel shift register 346
10.3 Counters 346
10.3.1 Count of 4 and 16 ripple counters ... 347
10.3.2 Modulo 3 and 5 counters 349

10.3.3 Decade counter 351
10.3.4 Synchronous Counters 353
10.4 Timers 354
10.4.1 Monostable multivibrator 355
10.4.2 Astable multivibrators 357

XI. Waveform Generators :

11.0 Introduction 363
11.1 Sinusoidal oscillators 363
11.1.1 Criterion of oscillation 364
11.1.2 LC Oscillators 367
11.1.3 RC Oscillators 374
11.1.4 Negative resistance oscillators 386
11.1.5 Crystal Oscillators 388
11.2 Square wave generator 389
11.2.1 Transistor astable multivibrator 390
11.2.2 Op-amps square wave generator 394
11.3 Pulse generators 396
11.3.1 Collector coupled transistor monostable multivibrator 396
11.3.2 Monostable multivibrator using Op-amps. ... 399
11.4 Triangular wave generators 400

XII. Power Supplies :

12.0 Introduction 407
12.1 Diode rectifiers 407
12.1.1 Half wave rectifier 407
12.1.2 Full wave rectifier 411
12.2 Capacitor input filter ... ...
12.2.1 Full wave rectifier with capacitor input filter ... 420
12.2.2 Ripple factor calculations 423
12.3 Inductor input filters 425
12.3.1 Full wave rectifiers 427
12.4 LC filters 429
12.4.1 CLC filter 434
12.5 Bridge rectifier 434
12.5.1 Voltage doubler 435
12.6 Voltage regulator 436

Appendices :

A : Laboratory Experiments 443
B : Device Data 471
C : Some physical constants 483
D : deci Bel (dB) 484
Index : 487

1

An Overview of Electronics

1.0 Introduction

Electronics today stands at the forefront of the rapidly expanding horizon of science and technology. Global communication of information, digital computers, data processing at incredible speeds, robots control of machines and processes, control of energy, management of environment, detection of targets, remote sensing, fast medical diagnostics are the gifts of electronics.

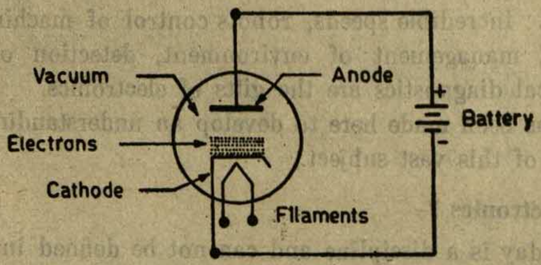
An attempt has been made here to develop an understanding of the basics and fundamentals of this vast subject.

1.1. What is Electronics ?

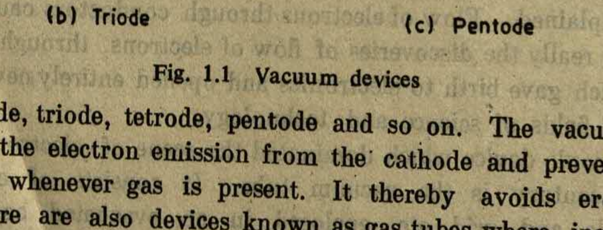
Electronics today is a discipline and can not be defined in brief. Primarily it is a subject dealing with devices where the generation and the flow of electronics are controlled. Circuits, subsystems and systems are instrumented using these electronic devices for carrying out different operations. The science and the engineering of electronics are less than 100 years old. Developments in electronics have been very fast, particularly over the past three decades, and the industrial and commercial applications have fortunately kept pace with these developments.

Even though electricity was discovered two centuries ago it was understood well only after the foundations of atomic theory were laid and the structure of matter was explained. Flow of electrons through conductors causes an electrical current. It is really the discoveries of flow of electrons through vacuum, gases and solids which gave birth to electronics and opened entirely new and unlimited avenues in all fields of science and technology.

The electronic device which dominated the scene of electronics for the first half of this century is the vacuum tube. It consists of electrodes called cathode, anode and grid etc. enclosed in an evacuated enclosure. In the simplest construction the tube has a cathode and an anode. The cathode emits electrons mostly by heating it, directly or indirectly, to high temperatures and the anode collects these electrons when kept at a potential higher than the cathode. Symbolically it is shown in Fig. 1.1 (*a*). Since the charge of the electrons is negative, they are attracted by the anode kept at a higher positive potential. Thus,a current flows from the positive terminal of the battery via the anode and the cathode to the negative terminal of the battery. Obviously, there is no current flow when the battery terminals are reversed since the negative anode now repels the electrons back to the cathode from where they came out. This device works as a valve since it allows current flow only in one direction and is appropriately known as a 'Electronic valve'. A third electrode with a grid type structure and known as the 'grid' is introduced in between the cathode and the anode as shown in Fig.1.1 (*b*). The grid controls the flow of electrons through the valve if its potential is negative with respect to that of the cathode. This device where the current flow in the valve can be controlled externally has tremendous capabilities. For improved working, greater control and flexibility more grid type electrodes are interposed between the anode and the cathode as shown in Fig. 1.1 (*c*). Depending upon the total number of electrodes the device is known as diode, triode, tetrode, pentode and so on. The vacuum inside the enclosure helps the electron emission from the cathode and prevents generation of positive ions whenever gas is present. It thereby avoids erosion of the electrodes. There are also devices known as gas tubes where inert gas at very low pressure is inserted. These devices find many special applications.



(a) Diode



(b) Triode

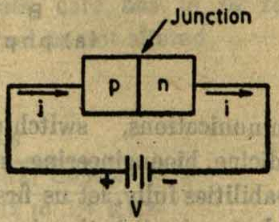
(c) Pentode

Fig. 1.1 Vacuum devices

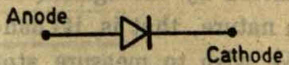
The second half of this century has seen a great revolution in the development of electronic devices. Control of the flow of electrons through solids, mainly semiconductors instead of vacuum resulted in solid state devices dispensing with the heating required to generate the electrons. These devices are orders of magnitude smaller in size. Semiconductors do not conduct at absolute zero temperature because of their stable atomic structure but allow a limited electrical conduction at room temperatures where their covalent bonds break resulting in generation of free electrons. Silicon, Germanium and Gallium Arsenide are good examples of semiconductors. When the number of electrons in the outermost shell of any atom are either more or less than the number required for a stable structure, the material has a higher conductivity. In semiconductors the presence of some impurities in small quantities upsets the atomic structure and causes electrical conduction. If these impurities are added to the pure semiconductor, then an extrinsic or doped semiconductor is obtained. The doped semiconductor having an excess of electrons is known as n-type semiconductor. An absence of an electron from a stable structure is called a 'Hole' for convenience and is said to possess a positive charge. The doped semiconductor having a lesser number of electrons than required for a stable structure is said to be having an excess of holes and is known as p-type semiconductor.

A composite semiconductor having two distinct p-type and n-type materials joined together by a metallurgical junction, as shown symbolically in Fig.1.2, has functions similar to that of a vacuum diode discussed earlier. Such a solid state device, when connected to the battery terminals as shown in Fig.1.2(*a*) allows the current to flow in one direction only.

The holes being the positive charge carriers are made to cross the pn junction when a positive potential is applied to the electrode on the p side. Electrons similarly, cross the junction in the other direction and come to the p-region. Reversal of the battery terminals prevents the electrons and the holes from crossing the junction and thus the current flow stops. It is to be noted that the current flow in these devices is due to the positive as well as the negative charge carriers.



(a) Semiconductor diode current flow



(b) Electrical symbol

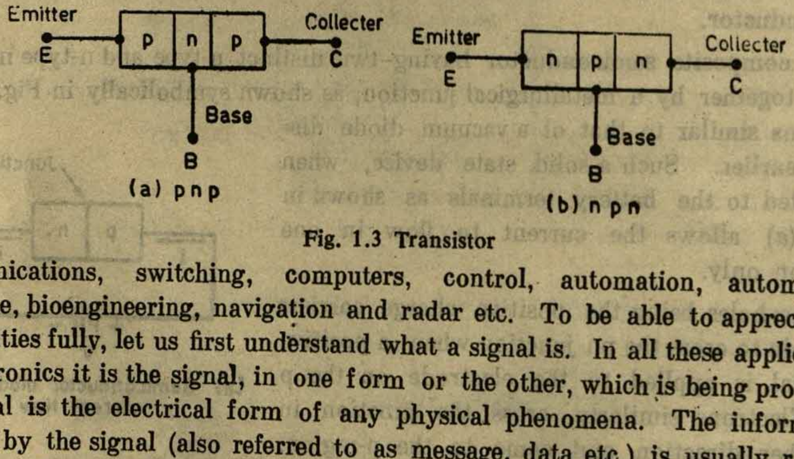
Fig. 1.2 Solid State Device

Two such pn junctions result in a three terminal device called a transistor as shown in Fig.1.3. The three terminals are known as the emitter E, the base B and the collector C. Given appropriate potentials the current flowing from E to C or vice versa is controlled by the current flowing through the terminal B. This solid state device is very small in size and consumes much less power than the vacuum tube but has similar capabilities of amplification, control, switching, etc. Its attractive features of small size, weight and power consumption has made it possible to replace the vacuum tubes in many applications. Sustained efforts in improving the technology are resulting in a phenomenal reduction in size of these solid state devices. They have been miniaturized to the extent of packaging 1500 to 2000 devices in a small chip of 1 mm × 1 mm area. The newer technologies are constantly aiming at increasing the packaging density. The technology is referred to as small, medium, large and very large scale integration (SSI, MSI, LSI and VLSI).

Both the vacuum tubes and the solid state devices are known as active devices because they normally require a power supply for operation and the current flow through them is unidirectional. The conventional electrical components such as resistances, capacitances, inductances and transformers are known as passive devices. Electronics is a science and engineering of fabricating these active and passive devices and connecting them together in order to carry out a particular desired operation.

1.2 Scope of Electronics

Scope of electronics is limited only by one's own imagination. Though it started with the idea of amplifying sound signals, it has now major applications in communications, switching, computers, control, automation, automobiles, medicine, bioengineering, navigation and radar etc. To be able to appreciate its capabilities fully, let us first understand what a signal is. In all these applications of electronics it is the signal, in one form or the other, which is being processed. A signal is the electrical form of any physical phenomena. The information carried by the signal (also referred to as message, data etc.) is usually random in nature, that is, it can not be foretold with certainty and varies with time. We wish to measure, store, process and convey an information, sometimes over very long distances. All this is possible with the help of electronics.



(a) pnp (b) npn

Fig. 1.3 Transistor

The electrical or the optical form of the signal is most suitable for transmission over long distances using either guided media such as pair of wires, cables, coaxial cables, circular and rectangular tubes (known as wave-guides) optical fibres etc. or free space. Generally the signal becomes quite weak when transmitted over long distances and it becomes necessary to amplify it to make it usable. This can be done by using vacuum or solid state active devices. Thus, starting with the generation of information bearing signals, their amplification and processing if any, their subsequent transmission over the desired medium and detection at the receiver, electronics plays a major role. In many industrial applications, manual or automatic, the signal actuates and controls operations made possible by electronics. Speech, television, written message and other natural signals are processed for ease of their storage, transmission and display. The electronic devices and circuits carry out these operations.

The signal can either be analogue having infinite amplitude levels or digital with finite and discrete number of levels. Instrumentation of systems becomes simpler and accurate with the digital form of the signal. Thus analogue signals are converted to digital form for storage, processing or transmission and are then reconverted back to the analogue form if so desired. One of the marvels of electronics is the modern digital computer which processes the information digitally. Faster and bigger computers are being designed today which perform millions of arithmetic and non-arithmetic operations in fractions of a second. With the enormous size of the memory at its command the computer has become a major and possibly the most important tool in automatic industrial processing and control, data processing of various types and vital decision making processes.

The signals we have been describing so far are all functions of time and can also be represented in the frequency domain with the help of Fourier series and Transforms. The frequency domain description may not be unique but in many applications it is important to know the frequency (spectral) content of the signals. Table 1.1 shows the frequency content of some of the most important natural signals.

When we consider the processing of these signals, care has to be taken to see that the spectral content of the recovered signal is not altered.

Table 1.1
Spectral Content of Signals

Signal	Spectral Content
Telephone Speech	300Hz to 3.4 KHz
Entertainment quality speech and music	20Hz to 20 KHz
Television picture	dc to 6 MHz
Teleprinter Signals	10 to 75 Hz

Most of the mathematical problems can be solved numerically. Since the electronic devices have two states of either a flow or a no flow of currents through them, they can be electrically controlled and are used to represent binary numbers. Thus these devices can carry out mathematical operations, like addition, subtraction multiplication and division etc. of binary numbers. Today's calculators, micro, mini and large computers are based on binary operations performed by the electronic devices.

We, thus, realize that electronics has made it possible to amplify, store, process, transmit and display information bearing signals. It can carry out computation, control and automation operations as well. In terms of these basic operations we can employ the techniques of electronic processing for any other sophisticated instrumentation.

1.3 Scope of the Book

As one can appreciate, the vast field of electronics with its ever increasing applications cannot be contained in a single volume. Only underlying principles of some of the basic devices, circuits and their applications have been dealt with in this book, Depending upon one's requirements and interests, either further higher level courses have to be taken or advanced books have to be read. This book only serves as a first small step to the whole new world of electronics.

In the previous sections we have given a bird's eye-view of what electronics is and what it does. It should be clear by now that to appreciate electronics and its applications the physical properties of the devices and its applications have to be understood. In the second chapter, therefore, we have discussed the properties of the materials and the devices made with these materials. Atomic and crystal structure of materials have been discussed and properties of materials suitable for electronic devices have been explained. These devices are required to be connected in a circuit to form a subsystem or a system which would perform a desired task. For this purpose it is important to understand the terminal behaviour of these devices. Chapter III has been devoted to an explanation of the characteristics of many commonly used devices. 'How are these devices made ?' is a natural question of any beginner in Electronics. Knowledge of the technology of making these devices enhances the understanding of the devices and one can then make a better use of them. Chapter IV deals with the technology of the devices. In fact technology of these devices by itself has been of great value to the modern developments in Science and Technology in almost all fields.

Devices in isolation cannot do anything. One has to learn to connect them in circuits which form a part of a subsystem or a system. The most important single electronic circuit is the Amplifier. Other circuits can be thought of as some variation of the amplifier and its associated passive circuit. Thus the subject matter of chapter V and VI is circuits and amplifiers. In all automation, control and practical systems the concept of feedback is very important. One has to observe the output of any useful system and compare it with what is desired (which may either be an isolated reference or the input itself) in order to correct any deviations. This is known as feedback and the concept is exhaustively used in Electronics. Therefore a full chapter on feedback has been included in the book. The early devices could carry out most of the operations but reducing the size of electronic devices and compoments been a very important requirement for many applications. In fact, miniaturization has opened many new areas of application altogether. The greatest developments in electronics in recent years have been in miniaturization and micro-miniaturization where large number of devices and components have been packed in a very small area resulting in Integrated

Circuits (IC). Integrated circuit amplifiers have been explained in Chapter VIII. One may ask a question viz. what is the necessity now of learning the basic devices when the ICs are available. The answer to this question is that the ICs after all consist of active devices, and in order to make their proper use and to find new applications, we have to understand these basic devices well. Understanding of these devices may not be necessary for a layman or a housewife using electronic gadgets but it is very important for an engineer, who has to maintain and make these gadgets and who has to find their newer applications, to know these devices well.

A major thrust and achievement of electronics is in the area of computer communication and instrumentation where accuracy and reliability are of prime importance. Digital Electronics forms the basis of these applications and is explained in Chapter IX and X.

In many Communication and Instrumentation applications, there is a need to generate different kinds of electrical waveforms such as sinusoidal, triangular, rectangular and so on. Generation of some of these important waveforms has been given in Chapter XI.

Most electronic circuits and many electrical systems require D. C. power sources. Since common electrical power sources are A.C. a conversion of AC to DC is very important. Further, in many applications it is required to keep either the electrical voltage or the current fixed even when the supply and the load voltages change because of some practical reasons. The fundamental principles underlying this power conversion and regulation have been discussed in Chapter XII.

Review Questions

1.1 What are the differences between a vacuum and a solid state electronic device ?

1.2 Name the different electrodes of a Triode and explain their purpose.

1.3 Why is an electronic device called a valve ?

1.4 When does a material act as an insulator, a semiconductor, a conductor ? Explain with reference to their electronic structure.

1.5 What are the n-type and the p-type semiconductors ?

1.6 What is an active device ?

1.7 What is a signal ?

1.8 What is a digital signal ?

1.9 What is the spectral content of (*a*) telephone quality speech signal (*b*) Television signal.

1.10 What can electronics do to information bearing signals ?

2

Physical Properties of Electronic Devices

2.0 Introduction

In this chapter we shall discuss the structure of atoms and explain the conditions under which a particular material becomes a conductor, an insulator or a semiconductor. After a brief description of the crystalline structure of materials we shall go over to the solid state devices and explain their properties in terms of the atomic and the crystalline structure and the externally applied electric fields.

2.1 Electronic Structure of Atoms

Since we are primarily concerned here with the flow of electrons, through either vacuum, gases under low pressure, or semiconductors, a knowledge of the structure of atoms is essential. In the Bohr's model of an atom, almost the entire mass and the total positive charge of the atom are concentrated in the nucleus at the centre and the electrons with their negative charge surround the nucleus like a cloud as shown in Fig. 2.1. The electrons occupy specific orbits with discrete energy levels known as the quantum levels. Their distrbution amongst different energy levels follows well known quantum-mechanical laws including the Pauli's exclusion principle. The electrons nearest to the nucleus have the lowest energy level and are tightly bound to the nucleus. They require the largest amount of

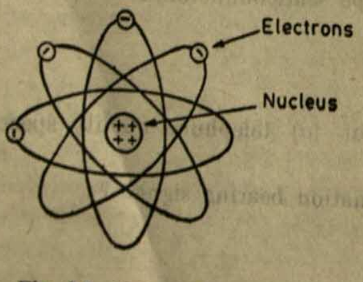


Fig. 2.1 Bohr's Atomic model

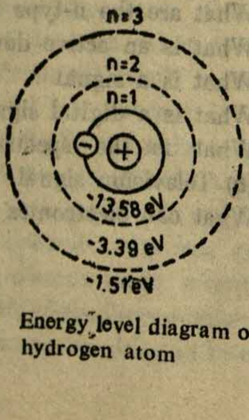


Fig. 2.2 Energy level diagram of a hydrogen atom

energy to move from their orbits. On the other hand the electrons away from the nucleus are obviously less tightly bound to it and have the highest energy. They require much less energy to be removed from their orbits. The energy level diagram of an hydrogen atom is shown in Fig. 2.2, where we see that the electron in the first orbit designated $n = 1$ has an energy of —13.58 eV. The electron-volt (eV) is a unit of energy and is equivalent to the work done in making an electron move through a potential difference of 1 volt. Energy associated with 1 eV $= 1.602 \times 10^{-19}$ joules.

The dotted circles show other energy levels which the electron can occupy. The electron can move to higher energy levels i.e., to the outer orbits by acquiring energy from an external source. Similarly, an electron can undergo a transition from higher to alower state by losing energy in the form of radiation. For example in moving the electron from the level $n=1$ to $n=2$, an external energy, equal to 10.19 eV (13.58—3.39), is to be supplied to the atom. Similarly when the electron comes back from the level $n = 2$ to $n = 1$, it releases 10.19 eV of energy in the form of radiation. An energy of 13.58 eV will be required to remove the electron completely from the atom. We must remember that electrons cannot occupy intermediate levels between 1 and 2 or 2 and 3 etc. For example, if an energy of say 8 eV is given, the electron does not move and occupy a level intermediate between 1 and 2. Since the electrons occupy discrete orbits havig discrete energy levels, they emit or absorb discrete amount of radiation energy in transition. The energy E and the frequency of radiation f are related by

$$E = h.f$$

where h = Planck's const $= 6.625 \times 10^{-34}$ joule-sec, E is in joules and f is in hertz.

Example 2.1.1

In a hydrogen atom the electron was excited to the level $n = 2$ Calculate the frequency of the radiation when the electron comes back to the original stable state $n = 1$

$$f = \frac{E}{h}$$

$$= \frac{10.19 \times 1.602 \times 10^{-19}}{6.625 \times 10^{-34}}$$

$$\text{or } f = 2.464 \times 10^{15} \text{ Hz}$$

With this understanding of the structure of the atoms, we now see how solids are formed by a congregation of many atoms.

2.2 Formation of solids—crystalline structure

There are two forms in which solids exist —crystalline and non-crystalline (or poly-crystalline). The crystalline solids have almost perfect structures and have been studied very well. They are suitable for the solid-state devices of our concern and we shall focus our attention on them only.

A molecule consists of many atoms of either similar or dissimilar elements and the solid consists of many molecules or atoms together. The relationship between the molecules and the solid is similar to one existing between the electrons and the atom. Just as an electron in an atom has energy, the atoms and the molecules in the solid have energy. Primarily, the electrostatic attraction and the quantum mechanical forces are involved in keeping the atoms and the molecules together in a solid. There are three important kinds of bonding amongst the atoms and the molecules of a solid. These are (i) Ionic (ii). Covalent and (iii) (iii) Metallic bonds.

Some molecules are formed and are held together by the transfer of electrons from the outermost shell of one atom to another. In this process both the atoms get ionised. The atom which loses the electron is ionised positively and the atom which gains an electron is ionised negatively. This establishes an electrostatic attraction between the two atms and they are bonded together by what is known as the Ionic bond. One may wonder why the two oppositely ionised atoms do not fuse into one another due to this electrostatic attraction. The reason for their not fusing together is that as the two atoms start coming closer, their outer-most shells overlap and the electrons are concentrated in a small volume. This sets up a repulsive force in the system. Further, Pauli's exclusion principle prevents overlap of two atoms whose outer shells are occupied. Thus, the atoms come to a certain stable distance with respect to each other and the molecule so formed is stable. We can consider sodium chloride as an example of the ionic bond. Sodium is an alkali metal and has one electron in its outermost shell. Chlorine is a hallide and has one electron less in its outermost shell. The excess or shortage is with respect to the stable state. The transfer of the single electron from the outermost shell of the sodium atom to the chloride atom leaves the sodium atom positively charged while the chlorine atom becomes negatively charged. With this ionic bonding between the sodium and the chlorine atoms we get sodium chloride as shown in Fig. 2.3.

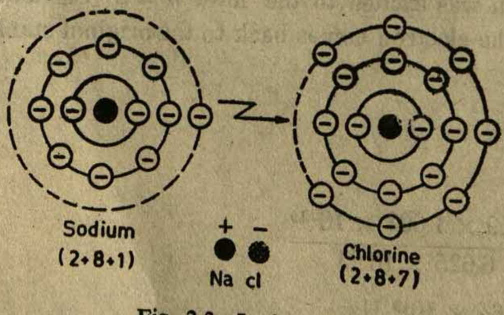


Fig. 2.3 Ionic bond

In covalent bonding the electrons in the half filled outermost shells of an atom are shared with the electrons in the half filled outermost shells of other nearby atoms. Elements like carbon, silicon, germanium and gray tin have four electrons in their outermost shells. The outermost shell should have eight electrons for an atom to be stable. An atom of these elements shares one electron each from the outermost shells of the nearby four atoms as shown in Fig. 2.4. Thus a stable structure with 8 electrons results.

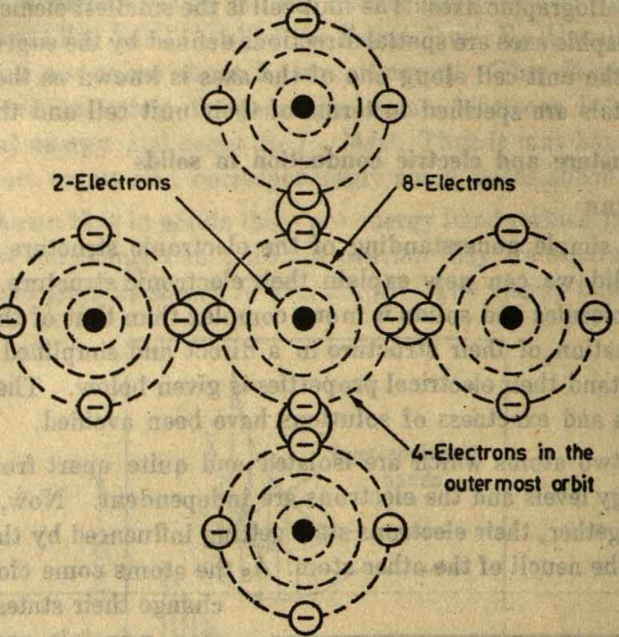


Fig. 2.4 Sharing of electrons in the covalent bonds. Example shown is for Silicon

Most of the metals have a cohesive crystalline structure because of the metallic bonding. The atoms of the metals come very close and as a result they disturb each other's outermost energy levels. Each atom of the metal contributes one or two free valence electrons. These electrons are free and mobile in the sense that they are not bound to the atoms and are free to move throughout the volume of the metal. The other electrons of the atom are not free to move through the metal. There are about 10^{29} electrons per cubic metre. A metal is electrically neutral because the negative charge on the free electrons is exactly balanced by the net positive charge of the ionised atoms. The atoms remain fixed in position as positive ions, and the electrical conduction in metals is solely due to the free electrons.

In all the types of bonding discussed above, the atoms come very close i.e., a few Angstroms and the distance is such that they have minimum energy while forming the crystalline solid. The atoms in a crystal are arranged in a well defined array called the crystal lattice. Crystals have well-defined geometrical shapes in their natural state which are known as growth planes. Cleavage planes exist in them along which they tend to split. Some of the important crystal structures are simple cubic, face-centred cubic, body centred cubic, diamond or tetrahedral and zinc blende.

The whole crystalline solid can be developed by translation of a unit cell along the crystallographic axes. The unit cell is the smallest element of the lattice. The crystallographic axes are spatial directions defined by the edges of the unit cell. The length of the unit cell along one of the axes is known as the lattice spacing. Thus, the crystals are specified in terms of their unit cell and the axes.

2.3 Band structure and electric conduction in solids

BAND STRUCTURE

With the simple understanding of the electronic structure and bonding of atoms in a solid we can now explain their electronic structure. The electronic structure of molecules and solids is more complex than that of the atoms. However an explanation of their structure in a direct and simplified fashion with a view to understand their electrical properties is given below. The rigour of quantum mechanics and exactness of solutions have been avoided.

Imagine two atoms which are isolated and quite apart from each other so that their energy levels and the electrons are independent. Now, if the atoms are drawn close together, their electrons start getting influenced by the presence of the electrons and the neucli of the other atom. As the atoms come closer the electrons change their states. Pauli's exclusion principle applies to the molecule as a whole and the two electrons can not occupy the same energy level. To accommodate the electrons of both the atoms therefore the individual energy levels split into two closely spaced states. Such a picture can be extended to the case of a molecule of *N* atoms where each state would split into *N* states as shown in Fig. 2.5 The energy of each of these split states is nearly the same.

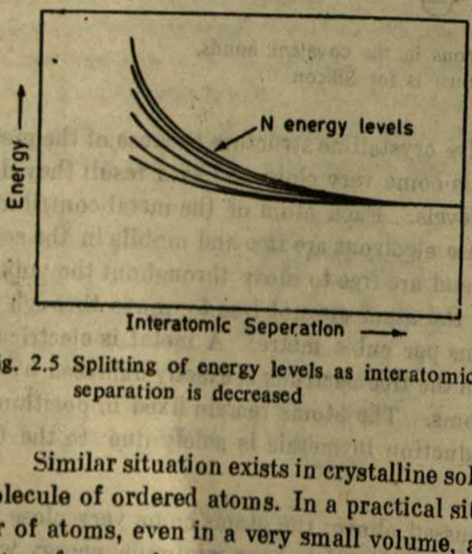
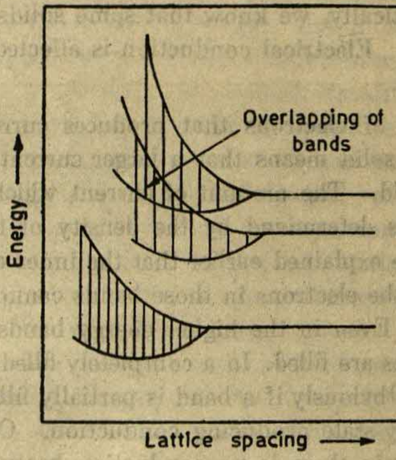


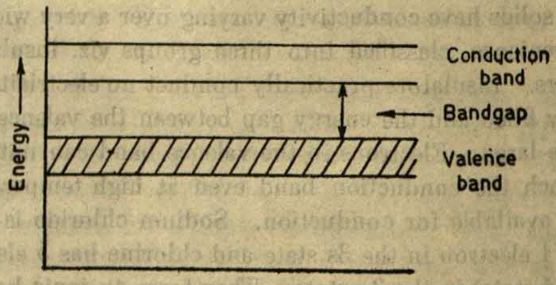
Fig. 2.5 Splitting of energy levels as interatomic separation is decreased

Similar situation exists in crystalline solids which may be considered as a large molecule of ordered atoms. In a practical situation a solid will have a large number of atoms, even in a very small volume, and hence an equally large number of states of approximately the same energy. The states can hardly be differentiated and the energy levels merge into an energy band, as shown in Fig. 2.6. More than one energy level may split into bands. In various solids these energy bands may remain seperate or overlap. For example, several of these bands overlap in the case ot sodium as shown in Fig. 2.6(a). In the case of solids where the bands do not overlap, the spaces between the bands are known as the forbidden energy gaps. There are no electrons in the solid having these energy levels. In solids also, the lower-most energy band is filled with electrons first and the band with higher energy is filled subsequently and so on. The energy level of the highest filled band is called the Fermi level, E_F. Usually all the states below E_F are filled and those above E_F are all empty. This is particularly true at $0°K$. However, at other temperatures some electrons below E_F acquire sufficient thermal energy and cross the E_F level. Thus it may happen that a few states below E_F are empty and correspondingly some states above E_F get filled.

We have shown that in solids there are energy bands which may or may not overlap. In case the energy bands do not overlap they are separated by what is known as the band gaps as shown in Fig. 2.6(b). The energy band in which the valence electrons reside are known as the valence band and may be completely or partially filled. There is an energy gap immediately above the valence band. The first allowed energy band above this forbidden band is known as the conduction



(a) Overlapping of bands



(b) Bandgap

Fig. 2.6 Energy bands in solids

band. Normally all the allowed energy levels in the bands below the valence band are completely filled, the valence band is partially or completely filled and the conduction band is completely empty. Electrons from the valence band overcome the band gap and go into the conduction band if they receive sufficient energy through external excitation. Electrical conduction takes place in a solid if there are electrons in the conduction band. It is important to realise that the valence, the forbidden and the conduction bands mainly determine the electrical properties of solids. The inner bands below the valence bands do not take part or affect the electrical conduction in solids.

ELECTRICAL CONDUCTION

Naturally the most important electrical property of a solid is its ability to conduct electricity. This ability depends basically on the structure of solids as discussed above. Heuristically, we know that some solids are better conductors of electricity than others. Electrical conduction is affected by the purity and the temperatures of the solid.

It is the movement of electrons that produces current flow in the solids. Larger conductivity in a solid means that a larger current would flow through it under a given external field. The amount of current which can flow or, in other words, the conductivity is determined by the density of the electrons and their ease of motion. We have explained earlier that the inner energy states in a solid are completely filled and the electrons in those bands cannot move and contribute to electrical conduction. Even in the higher energy bands electron movement is not allowed if all the states are filled. In a completely filled state there is no place for the electrons to go. Obviously if a band is partially filled, an electron, if excited, can move to an empty state producing conduction. Of course if the band is completely empty then again there is no conduction because there is no electron to move, even though there is a place for it to move.

Usually, the solids have conductivity varying over a very wide range of values and are, for convenience, classified into three groups viz, insulators, conductors and semiconductors. Insulators practically conduct no electricity. Their valence band is completely filled and the energy gap between the valence and the conduction bands is quite large. Electrons in the valence band can not get enough thermal energy to reach the conduction band even at high temperatures. Thus no free electrons are available for conduction. Sodium chloride is one such insulator. Sodium has 1 electron in the 3s state and chlorine has 5 electrons (one short of completely filled state) in the 3*p* state. They form an ionic bond between them and have all the states completely filled. The forbidden energy gap is of the order of 10 ev and is quite large for an electron to overcome. The insulators have resistivity ranging from 10^4 ohm-m to 10^{18} obm-m.

The energy bands in conductors overlap resulting in almost continuous energy states. The electrons thus have a great amount of freedom to move. Further, their valence bands are not completely filled—in fact they are only half-filled, and therefore there are enough electrons to move. We can see, for example, the energy band structure of copper which is a very good conductor of electricity. Copper has 1 electron in the *4s* state and, thus, it is half filled. Also, the *3d* and *4s* energy bands of the solid copper overlap giving rise to an abundance of available energy states. The resistivity of condctors range from 10^{-10} ohm-m to 10^{-4} ohm-m.

We now consider the third group of solids viz, the semiconductors. As the name suggests they fall in between the insulators and the conductor in terms of the resistivity. Basically they are like insulators at absolute zero temperature when their valence energy states are completely filled and the conduction band is empty. They differ from the insulators, however, in one major way and that is the size of their energy bandgap. The bandgap in semiconductors is only of the order of 1 eV. This narrow energy band gap can be crossed by electrons easily when they acquire thermal energy at room temperatures. Two interesting things happen. Firstly, when the electrons thus excited transfer from the valence to the conduction band a vacancy known as 'hole' is created in the valence band and an electron is available in the conduction band which was otherwise completely empty. Secondly the vacancy or the hole in the valence band can be filled by another electron within the valence band but this only results in another hole somewhere else. Thus, in the process of filling the holes the electrons in the valence fnad move and in turn create new holes. The excited electron which was transferred to the conduction band has many available energy states to move. The material thus is conducting at room temperature though it did not conduct at the absolute zero temperature. The most striking feature of the conduction in the semiconductors is that the conduction is due to electrons as well as holes together.

We should remember that the thermal energy releases an electron-hole pair and that the number of electrons and holes are equal. The concept of hole as a mobile carrier of positive charge is an artifice that allows us to describe the complex motion of the bound electrons in a simple fashion.

Silicon and germanium are two very good examples of semiconductors. The electron occupancy of silicon is $(1S)^2$, $(2S)^2$, $(2P)^6$, $(3S)^2$, $(3P)^2$ and for germanium it is $(1S)^2$, $(2S)^2$, $(2P)^6$, $(3S)^2$, $(3P)^6$, $(3d)^{10}$, $(4S)^2$, $(4P)^2$. We observe that in both silicon and germanium the valence state has four electrons only and four more electrons are required for a stable configuration. They share four electrons from the four neighbouring atoms to form a covalent band as discussed earlier. They thus get a stable structure in the solid form. At absolute zero temperature germanium and silicon behave like insulators. Their energy band gap is however quite small, e.g. 1.1,eV for silicon and 0.79 eV for germanium. At room temperature both of them become conductors with resistivities of 0.6 ohm-m for germanium and 3000 ohm-m for silicon. These two materials form the base of most of the semiconductor devices.

Another semiconductor material of great importance today is Gallium Arsenide. Gallium is an element in the 3rd group of the periodic table and has 1 electron in the $4P$ state. Arsenic is an element of the fifth group and has 3 electrons in the $4P$ state. In the gallium-arsenic crystalline solid, the $4P$ states of both are shared to form a covalent bond. The silicon and germanium crystals have a diamond lattice structure where all the atoms are of the same kind, that is either silicon or germanium. The gallium arsenide crystals have a zincblende lattice where one of the sublattices is gallium and the other is arsenic. The band gap in gallium-arsenide at room temperature is 1.43 eV which is larger than those of both germanium and silicon.

2.4 Intrinsic and extrinsic semiconductors

We have shown that in pure semiconductors, the valence band is completely filled and the conduction band is completely empty at absolute zero temperature. Such materials therefore will not conduct electrically at 0°K. However, at the room temperature some of the electrons are thermally excited and jump to the conduction band from the valence band leading to conduction in the material. The conduction is due to two kinds of charge carriers—the 'holes' as well as the 'electrons'. This process of electron-hole pair generation is intrinsic, that is, it is a property of the crystal. Such semiconductors are known as intrinsic semiconductors. The carrier densities, p of the holes and n of the electrons in an intrinsic semiconductor, are equal and depend on the temperature T and the energy gap E_g. The parameters n, p, T and E_g are related as follows

$$n = P$$

$$p \propto T^{3/2}.\ e^{-E_g/2kT} \tag{2.4.1}$$

where K is the Boltzmann's constant.

The intrinsic carrier density n_i is defined as

$$n_i = \sqrt{np} \tag{2.4.2}$$

Since $n = p$ in intrinsic semiconductors

$$n_i = n = p$$

The values of n_i for germanium and silicon at 300°K are 2.4×10^{19} and 1.5×10^{16} per m^3 respectively. We note that n_i is smaller for silicon because the E_g is larger.

An electric current will flow if an electric field E is applied to the intrinsic crystal. The current density J is given by

$$J = nq\, v_n + pqv_p \tag{2.4.3}$$

where q is the charge of the election and v_n and v_p are the electron and hole velocities respectively. Since the hole is an absence of the electron, its hypothetical charge is considered to be equal to that of an electron but with a positive sign.

We can now find the conductivity σ of the semiconductor as

$$\sigma = \frac{J}{E} = \frac{nqv_n}{E} + \frac{pqv_p}{E} \tag{2.4.4}$$

The velocity of the charge carrier in an electric field E will depend on the mobility μ of the charge carrier and is given by

$$V = \mu E \tag{2.4.5}$$

From Eq. (2.4.4) and (2.4.5),

$$\sigma = nq\,\mu_n + pq\,\mu_p \tag{2.4.6}$$

and for intrinsic semiconductor

$$\sigma = n_i\,q(\mu_n + \mu_p)$$

So far we have assumed that the crystals are pure. In practice they may have many defects and impurities. Defects arising from the absence of an atom in the crystal lattice produce distortion in the band structure of the crystal and consequently affect its electrical characteristics Another very important defect in crystals is the presence of impurities. The impurities are the presence of atoms of a different material in the lattice structure. These foreign impurity atoms have different properties—different from the parent crystal atoms. The foreign atoms may either replace the crystal atoms in the lattice or may lie in the interstitial space of the lattice. These impurity atoms once again affect the electrical behaviour of the crystal. Fortunately, we take advantage of these impurities in a controlled fashion in making semiconductor devices.

To understand the effect of these impurities better let us assume that an atom of say Arsenic from the fifth group of the periodic table replaces an atom of germanium in the germanium semiconductor crystal. In the pure form, the atoms of germanium are bound together by the covalent bonds and each atom shares the electrons of the 4 neighbouring atoms. Arsenic has however 5 electrons in the outermost shell. Four of these electrons are shared with the four neighbouring germanium atoms in the usual manner and the fifth electron is loosely bound to the atom. The binding energy of this electron is quite small. The normal states of the fifth group of elements like arsenic are near the conduction band. Energies much smaller than the bandgap of the semiconductor excite the electrons of these elements to go to the conduction band. Extra electrons are thus available for conduction. Since these elements contribute an extra electron they are known as 'donor' elements or donor impurities. We observe that the donor atom itself is positively ionised when its electron is excited to the conduction band and moves away. The important thing to observe is that no hole is created in the donor by this process—in direct contrast with the intrinsic semiconductor where an electron-hole pair is always generated. The conductivity of the crystal having donor impurities has some interesting features. The semiconductor has now many more electrons than holes as charge carriers. These semiconductors are known as extrinsic semiconductors and are termed *n*-type because of the excess of negative charge carriers.

Next an atom from the third group of the periodic table, say Boron, may be substituted into the germanium crystal lattice. Boron atom has three electrons only in its outermost shell and these three electrons are shared with the three neighbouring germanium atoms as usual. There appears a 'hole' in the covalent bond with the fourth germanium atom. An electron from a neighbouring germanium atom can jump into this vacancy creating a hole elsewhere. This electron requires much smaller energy to leave the parent atom as compared to the bandgap. Thus the hole is said to be weakly bound to the impurity atom. Such impurity atoms are known as 'acceptors' and make the crystal *p*-type because there is now an excess of holes or possitive charge carriers. The acceptors sit near the valence band and are left negatively ionized as a result of capturing an electron from the valence band. Compared to the energy gap of about 0.7 eV in germanium, the binding energy of the donors and the acceptors is about 0.01 eV only.

The relation

$$n_i^2 = n.p \tag{2.4.2}$$

where n and p are electron and hole densities respectively, always hold true. For an *n*-type doped semiconductor the electron density is

$$n = N_D + n_t$$

where N_D is the donor density and n_t is the thermally generated electron density. If the thermally generated hole density is p_t, then

$$n_i^2 = (N_D + n_t)\, p_t$$

Thus

$$\cong N_D.p_t\ ;\ \text{since } N_D \gg n_t \tag{2.4.7}$$

$$p_t \cong \frac{n_i^2}{N_D} \tag{2.4.8a}$$

Similarly for the *p*-type semiconductor,

$$n_t = \frac{n_i^2}{N_A} \tag{2.4.8b}$$

wher N_A is the acceptor density. The conductivity in the extrinsic semiconductors is mainly due to the impurity atoms.

$$\sigma_n = n.q.\mu_n + p.q.\mu_p$$

$$= (N_D + n_t)\, q\,\mu_n + p_t.q.\mu_p$$

$$\cong N_D\, q\, \mu_n\ ;\ \text{since } N_D \gg n_t = p_t \tag{2.4.9}$$

Similarly

$$\sigma_p = N_A.\, q\mu_p \tag{2.4.10}$$

In a *p*-type semiconductor the holes are known as the majority carriers and the electrons the minority carriers. Similarly in the *n*-type material, the holes are the minority carriers and the electrons are the majority carriers. We see that by adding large amount of impurities, the majority carriers increase and simultaneously the minority carriers are reduced. The discussion above applies equally well when we take S_i or *GaAs* instead of *Ge* as the semiconductor material. The concentration of impurity atoms in a doped silicon semiconductor is about $2 \times 10^{19}/m^3$, whereas the number of atoms is of the order of $10^{29}/m^3$. Thus there is one impurity atom for every 10 billion atoms of silicon. Although this concentration appears to be relatively small we should note that there are twenty thousand billion charge carriers in 1 cc of the doped silicon available for conduction. It indeed is remarkable that such small concentratins of impurity modify the properties of the semiconductors to make them useful for a wide range of electronic devices.

A process which we have not mentioned so far is the process of recombination going in the semiconductor material all the time. The thermally generated holes and electrons move in a random manner through the crystal as a result of collison with other particles. It is possible that in their random wandering a free electron and a hole may come close together. The electron and the hole may cancel each other by a recombination process where the electron jumps into the empty covalent bond represented by the hole. The probability of recombination is very high in the regions of imperfections such as dislocations in the lattice and impurities.

Example 2.4.1

A silicon material is uniformly doped with phosphorous atoms at a concentration of $2 \times 10^{19}/\text{m}^3$. At the temperature of interest the mobilities of holes and electrons are

$$\mu_p = .05 \text{ m}^2/\text{volt-sec.}$$

$$\mu_n = 0.12 \text{ m}^2/\text{volt-sec.}$$

$$\text{and} \quad n_i = 1.5 \times 10^{16}/\text{m}^3$$

Find the electron and hole concentrations and the electrical conductivity.

Now $q = 1.602 \times 10^{-19}$ coulombs.

The concentration of holes using Eq. (2.4.8a), is given as

$$p_t = \frac{n_i^2}{N_D} = \frac{(1.5 \times 10^{16})^2}{2 \times 10^{19}}$$

$$= 1.125 \times 10^{13} \text{ per m}^3$$

The concentration of electrons is

$$n \cong N_D = 2 \times 10^{19} \text{ per m}^3.$$

The conductivity σ_n is obtained as, using Eq. 2.4.9,

$$\sigma_n = 1.602 \times 10^{-19} \times 2\text{x}10^{19} \times 0.12$$

$$= 3.84 \text{ mhos per meter.}$$

2.5 Electronic Devices

As we have said earlier, the basic property of the electronic or electrical devices is the flow of electrons through them. In solid state devices the flow of electrons is through the solid crystal, in vacuum devices it is through the vacuum and in gaseous devices it is through the intervening gas between two electrodes. Let us discuss these devices in greater detail, beginning with the solid state devices.

p-n JUNCTION

We have seen that a *p*-type semiconductor material consists of acceptor impurities and has excess of holes over electrons in it. The n-type semiconductor has donor impurities and the electrons concentraton is higher than that of the holes in it. Now suppose that these two semiconductor materials, as shown in Fig. 2.7, are joined together metallurgically. There are many ways of forming this junction and all we shall assume here is that the junction is an abrupt one, that is, the impurity concentrations change abruptly from one side of the junction to the other. Near the junction plane, therefore, there is a concentration gradient of holes from *p* to *n* side and of electrons from *n* to *p* side. The holes from the *p* region will diffuse into the *n* region and similarly the electrons from the *n* region will diffuse into the *p* region. The *n* region which was electrically neutral earlier will become positively charged because of the presence of the extra holes which have diffused into it. The *p*-region will similarly become negatively charged because of the extra electrons which have diffused into it.

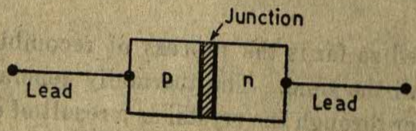
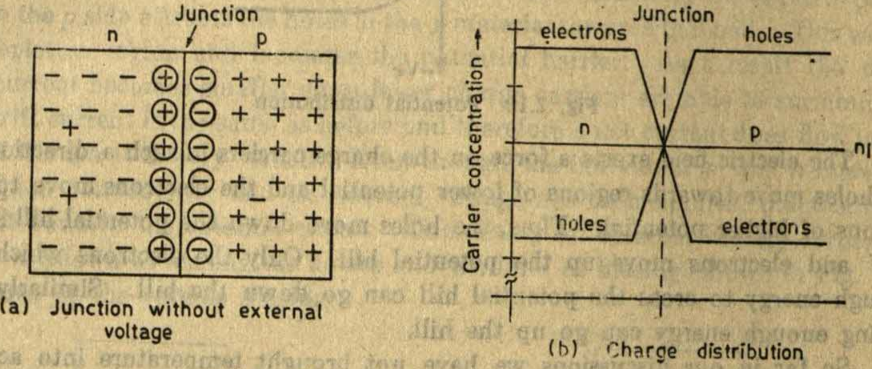


Fig. 2.7 *p-n* junction

The migration of these diffused holes and electrons has created a situation where the *p* and the *n* regions are no longer electrically neutral. However, the diffusion of carriers does not go on for ever because the carriers which have already diffused tend to oppose further migration of holes and electrons across the junction. In other words the potential difference created by the movement of the charge carriers acts as a barrier.

Let us now look at the diffusion process and the creation of the potential barrier in more detail. Consider the situation shown in Fig. 2.8(a) where the holes move from the *p* region into the *n* region due to the concentration gradient we talked about earlier. The idea of the 'hole' was really that of a vacancy of an electron in the covalent bond. When the hole moves into the *n*-region it creates a vacancy there. Since there is a large number of free electrons there the 'vacancy' gets filled up by an electron jumping into it. In this process the atom of the *n* region which had the vacancy and acquired an electron becomes neutral. The donor impurity atom which contributed the free electron now becomes positively charged. It is important to remember that atoms are fixed in the lattice and do not move but the electrons and holes only participate in the movement. The hole in the *p* region was originally associated with the acceptor impurity, but once the hole moves out the "vacancy" is created in a non-impurity atom. Thus vacancy moving into the *n*-region has, therefore, created a situation where one of the donor impurity atoms becomes positively charged. Since this impurity atom has all its four covalent bonds filled, it is stable though positively charged. It is also known as the bound positive charge because it does not take part in any exchange of charge carriers any further.

In a very similar fashion the electron from the *n*-region diffuse into the *p*-region. Once an electron moves into the free vacant position available in the acceptor impurity atom, it gets bound to it. All the four covalent bonds are thus filled up and the atom is negatively charged. This will give rise to a bound negative charge. Since the concentration of holes in the *p*-region and electrons in the *n*-region is quite high the migrated charge carriers do not penetrate much and therefore the bound charges exist very near the junction plane only. We can thus visualise layers of positive and negative charges as shown in Fig. 2.8(a). This layer is appropriately called the space charge layer because of bound charges. Since the region of the space charge does not have free charge carriers present in it, it is also known as the depletion region. The distribution of the charge carriers is shown in Fig. 2.8(b). The ordinate is the carrier concentration on a logarithmic scale. The charge density on both sides of the junction is shown in Fig. 2.9.



(a) Junction without external voltage

(b) Charge distribution

Fig. 2.8 Charges in *p-n* junction

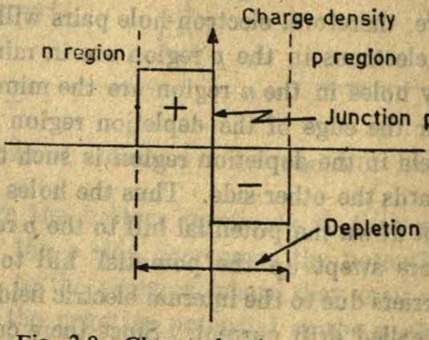


Fig. 2.9 Charge density across the junction

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It is clear that the positively charged layer in the *n* region will inhibit further movement of holes into it. Similarly the negatively charged layer will inhibit further movement of electrons into the *p* region. Thus we see that a potential barrier is created across the junction which limits the movement of charge carriers. In other words since the two layers of charges are of opposite polarity an electric field exists across the junction. Associated with this electric field there is a potential difference. The variation of the potential is shown in Fig. 2.10. This electric field opposes the diffusion of the holes and the electrons across the junction.

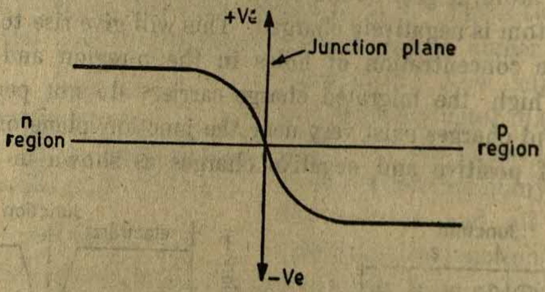


Fig. 2.10 Potential distribution

The electric field exerts a force on the charge carriers in such a direction that the holes move towards regions of lower potential and the electrons move towards regions of higher potential. Thus, the holes move down the potential hill in Fig. 2.10 and electrons move up the potential hill. Only the electrons which have enough energy to cross the potential hill can go down the hill. Similarly holes having enough energy can go up the hill.

So far in our discussions we have not brought temperature into account. It is known that charge carriers are also generated in pairs due to thermal excitation. At room temperature, therefore, electron-hole pairs will be available in both the *n* and *p* regions. The electrons in the *p* region are in minority and are called minority carriers; similarly holes in the *n* region are the minority carriers. Some minority carriers come near the edge of the depletion region during their random movement. The electric field in the depletion region is such that it aids the minority carriers in drifting towards the other side. Thus the holes in the region approaching the junction are swept down the potential hill to the *p* region. The electrons in the *p* region similarly are swept up the potential hill to the *n* region. This movement of the charge carriers due to the internal electric field constitutes a current across the junction and is called drift current. Since there cannot be a current in a device without external field, the postulate of the drift current seems to be fallacious unless it is counterbalanced in actual practice. It indeed is so because there is a diffusion current flowing across the junction in the opposite direction as explained below.

It has been shown that the potential barrier opposes the movement of the majority charge carriers across it. However, due to thermal excitation some of the majority carriers acquire enough energy to cross the barrier and move into the other region. The movement of such carriers across the junction constitutes the diffusion current. Both the diffusion and drift currents are functions of temperature. The diffusion current is equal and opposite to the drift current in equilibrium and therefore there is no net flow of charge carriers across the junction. If the drift current increases due to some reasons the diffusion current also goes up.

EXTERNAL BIAS

We have described so far a device which has a junction and two leads connected to the opposite faces of the crystal without any external voltage applied to it. There are drift and diffusion currents across the junction in the device which balance each other. Now we consider the device with an externl voltage applied to its terminals as shown in Fig. 2.11.

It is simple to understand that the positive potential on the *n*-side of the device attracts the free electrons towards that end. Similarly the negative potential on the *p* side attracts the holes in the *p* material towards that end. This widens the depletion region and increases the potential barrier. As a result the diffusion current becomes smaller since fewer charge carriers are able to surmount it. The drift current is the same as before and therefore a net current does flow in the circuit though it is very small. Even though the individual *p* and *n* materials have good conductivity and an external voltage has been applied, practically no current flows in the external circuit. Connecting an external voltage across the device is known as biasing the device and the kind of biasing shown in Fig. 2.11 is known as the reverse biasing.

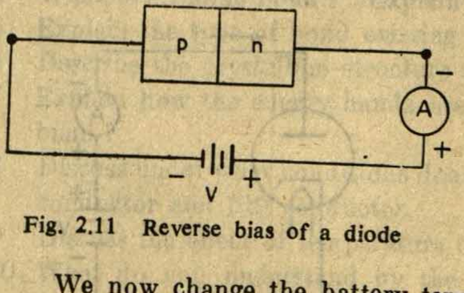


Fig. 2.11 Reverse bias of a diode

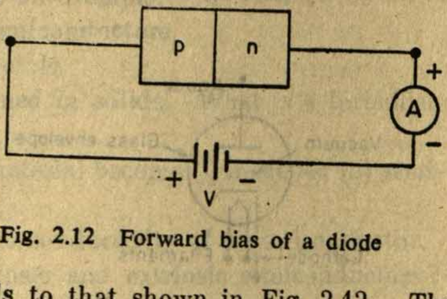


Fig. 2.12 Forward bias of a diode

We now change the battery terminals to that shown in Fig. 2.12. The positive potential on the *p* side overcomes the potential barrier and pushes the holes of the *p*-region to the *n*-region where they may recombine with the excess electrons. Similarly the negative potential at the *n* side pushes electrons of the *n*-region to the *p*-region where again they may recombine with the holes. The potential barrier becomes much lower and the diffusion current increases over the drift current considerably.

The movement of charge carriers, both electrons and holes, across the junction under the influence of this applied electric field increases much more. An ammeter connected in the external circuit will record the current flow. Since the electrons and the holes have opposite charges the actual current is therefore only in one direction. The direction of conventional current flow is assumed to be the opposite of the direction of electron flow. This kind of external voltage is known as the forward bias. The amount of current in the forward biased device is much larger than that in the reverse biased device.

We know that the current through a resistance flows in both the directions but here we have made a device where the current flow is only in one direction i.e., it is unidirectional. Such a characteristic finds many applications which will be discussed in later chapters. The device is known as 'diode' and is shown symbolically in Fig. 2.13.

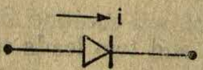


Fig. 2.13 Diode

The detailed characteristics of the diode and its fabrication are discussed in subsequent chapters. Other solid state electronic devices consisting of more than one *pn* junction which have important applications are discussed in the next chapter.

VACUUM AND GAS DIODES

Let us now consider a vacuum device with similar characteristics, that is conduction in only one direction. Here we have a cathode and an anode shown symbolically in Fig. 2.14. We have shown that when energy is supplied to a material the electrons in the outer most shells get excited to the higher states. If the supplied energy is sufficient then the electrons leave the material and are emitted. For example, when a material like tungsten, thoriated tungsten or oxide coated tungsten is heated to a sufficiently large temperature of say 1000°K and above, electrons are emitted. The cathode may be heated directly or it may be heated indirectly by passing a current through a filament as shown in Fig. 2.14. The

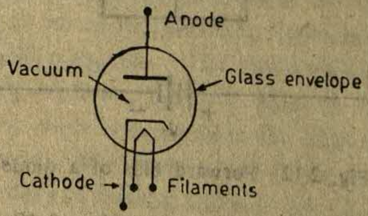


Fig. 2.14 Vacuum diode

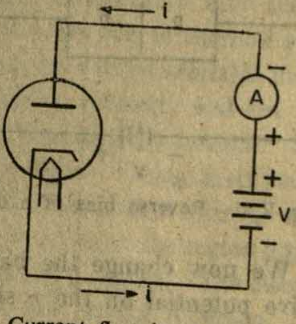


Fig. 2.15 Current flow in a vacuum diode

electron emission would be easier and the material of the cathode at such high temperatures would not corrode if the whole process is performed in vacuum. An electrode called anode is kept at a certain distance from the cathode. Now if we apply a positive potential to the anode with respect to the cathode, the electrons emitted from the cathode are attracted by the anode. Thus the electrons flowing through the vacuum strike the anode and cause a current flow in the circuit as shown is Fig. 2.15. Obviously the reversal of the polarity of the voltage stops the current flow because the electrons are repelled back towards the cathode. This is exactly what happened in the semiconductor diode. The vacuum devices are bigger in size, require large biasing voltage to operate, need external heating power for generation of electrons and require a vacuum. These reasons have made them less useful as compared to their solid-state counterpart.

In gaseous devices, the vacuum is replaced by an inert gas at low pressure. The gas has to be inert in order that it does not corrode the anode and the cathode materials. It has to be at low pressure so that the electron emission from the cathode is not obstructed. Application of positive potential at the anode accelerates the electrons which may collide with the gas molecules and ionise them resulting in positive and negative ions. These positive and negative ions, in the presence of the field, start moving towards the cathode and the anode respectively. Thus a heavy conduction takes place. One of the very important characteristics of this device is that the potential drop across the anode and the cathode remains constant even when the current through it is changing. This property along with other properties make the gaseous devices very useful particularly in Industrial/Power electronics. Of course the solid state counterpart for gaseous devices are now available and are finding wide applications.

Review questions

2.1 Describe the electronic structure of a helium atom.

2.2 Explain how transition of electrons take place from one level to another in an atom.

2.3 Explain what you understand by the crystalline structure of a solid.

2.4 What is an ionic bond ? Explain with an example.

2.5 Explain the type of bond existing in semiconductors.

2.6 Describe the crystalline structure of metals.

2.7 Explain how the energy bands are formed in solids. What is a forbidden band ?

2.8 Discuss under what conditions does a material become (i) insulator (ii) semiconductor and (iii) conductor.

2.9 Discuss the effect of temperature on the conductivity of a semiconductor.

2.10 What do you understand by the intrinsic and extrinsic semiconductors ? Explain with examples of Donors and Acceptors.

2.11 What is a 'hole' ? How does it contribute to flow of current in a semiconductor ?

2.12 What is Fermi level ? Describe the energy levels of *p*-type and *n*-type semiconductors.

2.13 Explain how a potential barrier is formed in a *pn* junction. Describe the potential distribution across the junction.

2.14 Describe the distribution of charge carriers throughout a *pn* device.

2.15 Explain the current flow nechanism in a *pn* junction diode at room temperature when it is

(i) unbiased (no external voltage applied)
(ii) forward biased
(iii) reverse biased

2.16 Explain how electrons are emitted from a cathode.

2.17 Explain the current-flow in a vacuum diode.

2.18 Describe the current-flow mechanism in a gas diode. How does it differ from a vacuum diode ?

Problems

P 2.1 Express 10 electron-volts in joules.

P 2.2 A material is radiating infrared rays at a wavelength of $\lambda = 900$ nanometers. Calculate the difference of energy in eV between the two states of an atom which would give rise to this radiation.

P 2.3 Calculate the conductivity of an intrinsic silicon semiconductor material having

$n_i = 10^{16}$ per m^3 at 300°K
$\mu_p = 0.05$ m^2/volt-sec.
$\mu_n = 0.12$ m^2/volt-sec.

What will be the value of resistance of a pellet of silicon 1 cm long and 1 mm in radius.

P 2.4 In a *p* type germanium semiconductor the intrinsic carrier density is 2.4×10^{19} per m^3. If the doping concentration is 10^{23} per m^3, calculate the approximate concentration of holes and electrons in the material.

P 2.5 In the problem P 2.3 if the silicon crystal is doped with an impurity concentration of 10^{20} per m^3, calculate the resistance of the pellet. Compare with the resistance of the intrinsic pellet.

P 2.6 In a thick-film circuit a resistance is formed by doped silicon. If the size of the resistor is to be 15 mm$\times$0.01 mm^2 and its value is 100 KΩ, calculate the doping concentration. Other parameters are the same as given in P 2.3

3

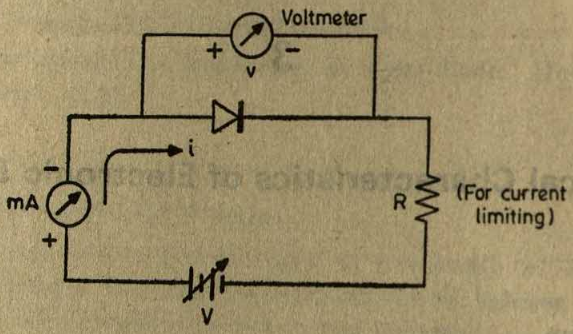
Electrical Characteristics of Electronic Devices

3.0 Introduction

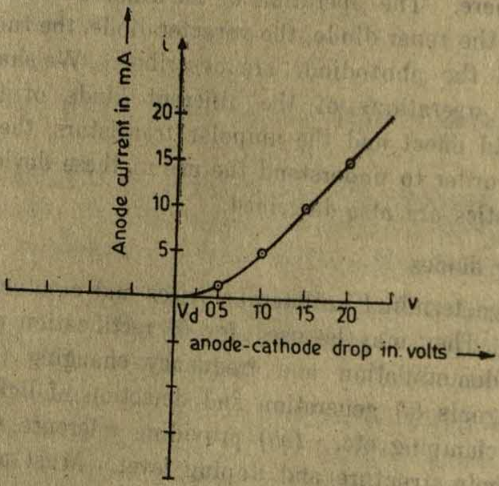
The physical principles underlying the electronic devices have been explained in the previous chapter. We shall discuss the principles of operation of different electronic devices here. The operation of the different kinds of diodes such as the junction diode, the zener diode, the varacter diode, the tunnel diode, the light emitting diode and the photodiode are described. We shall follow it with a description of the operations of the different kinds of transistors such as the bipolar, the field effect and the unipolar transistors, the thyristors and the vacuum tubes. In order to understand the use of these devices in circuits, their terminal characteristics are also described.

3.1 Semiconductor diodes

Diodes are two terminal unilateral devices and conduct current only from anode to cathode. They may be used for (*i*) rectification of a.c. (*ii*) switching (*iii*) modulation, demodulation and frequency changing (*iv*) generation and amplification of signals (*v*) generation and detection of light (*vi*) wave shaping such as clipping, clamping etc. (*vii*) providing reference voltages, and so on depending upon their structure and doping level. Most of the semiconductor diodes are junction diodes formed by growing a metallurgical junction detween *p*-type and *n*-type semiconductors. The current flow mechanism in these diodes has been explained in chapter 2. The terminal characteristics of a semiconductor junction diode can be experimentally determined by connecting the diode in the circuit shown in Fig. 3.1. The current is measured by applying different voltages from a variable voltage supply V. For each current value the voltage drop v across the diode is measured. A v-i characteristic as shown in Fig. 3.2 is obtained. Let us observe the special features of this characteristic and try to explain them. We see that the current is very small, in fact practically zero, when the voltage is small, say less than 0.5 volt. Above about 0.5 volt, the current starts increasing exponentially first and then almost linearly later. We also observe that there is practically no current for the negative voltages i.e., when the polarity of the applied voltage is reversed. It has been explained in the previous chapter how a depletion region is formed near the *pn* junction by the diffusion of holes from the *p* to the *n*-region and of electrons from the *n* to the *p*-region. With the application of the forward bias voltage the width of the depletion layer decreases and a small current flows. The depletion layer has a potential barrier of 0.3v for Ge and 0.7v for Si at 300°K. When the applied potential is smaller than the barrier potential V_d the current flow is very small. Once the applied potential is larger than the barrier potential the current increases exponentially according to the following equation



3.1 Circuit for the *v-i* characteristic of the diode



3.2 *v-i* Characteristic of the diode

$$i = I_s\, exp\,(\frac{v}{kT/q}) - 1 \tag{3.1.1}$$

where I_s is the reverse saturation current (explained later)
k = Bolzman constant $= 1.38 \times 10^{-23}$/Joule/°K
or $k = 8.62 \times 10^{-5}$ eV/°K
T = Temperature
q = charge of an electron $= 1.602 \times 10^{-19}$ Coulomb.

At 290°K the term $\frac{kT}{q}$ is calculated to be

$$\frac{kT}{q} = \frac{1.38 \times 10^{-23} \times 290}{1.602 \times 10^{-19}} = 0.0250 \text{ Volt}$$

Therefore at 290°K,

$$i = I_s \frac{v}{(e^{0.0250} - 1)}$$

$$= I_s \left(e^{40v} - 1 \right) \qquad (3.1.1\ (a))$$

This relation shows that i is strongly dependent on v. When v is small, i is small but if v is large then i is very large. However, we see in Fig. 3.2 that experimentally the current does not increase exponentially for large voltages. In fact the relationship is linear for larger voltages. The reason for this is that the equation (3.1.1) holds true for small and moderate voltages only. At large voltages the resistance of the neutral semiconductor material and the metal—semiconductor terminal contact comes into picture. Thus the current can increase only linearly with the applied voltage. The effect of the ohmic resistance is neglected when the current is small.

We have considered only the majority carriers in the p and n type semiconductors and the current flow through the diode has been discussed in terms of the movement of the majority carriers. This is true when the diode is forward biased. We next consider the case of the reverse biased diode. Ideally there would be no current flow under the reverse biased condition because the holes of the p-region would be attracted towards the negative end of the applied potential and the electrons in the n-region would be attracted towards the positive end. Thus the width of the depletion layer will increase and the potential barrier would be larger. However, in addition to the majority carriers, minority carriers will also be present in both the p and the n type semiconductors. The minority carriers under the reverse biased condition would move across the junction and give rise to a current, though very small. Let us, as an example, calculate the concentration of the minority carriers. We shall assume that the intrinsic carrier concentration in Ge at 300°K is

$$n_i = 10^{19}\,/\text{m}^3$$

If the impurity concentration in the p and n regions are

$$N_A = 10^{24}\,/\text{m}^3$$

$$\text{and} \quad N_D = 10^{22}/\text{m}^3$$

then the number of holes in the p-region are

$$p = 10^{24}/\text{m}^3$$

and the number of electrons in the n-region are

$$n = 10^{22}/\text{m}^3$$

Therefore p_n the density of the holes in the n region is

$$p_n = \frac{n_i^2}{n} = \frac{10^{38}}{10^{22}} = 10^{16}/\text{m}^3$$

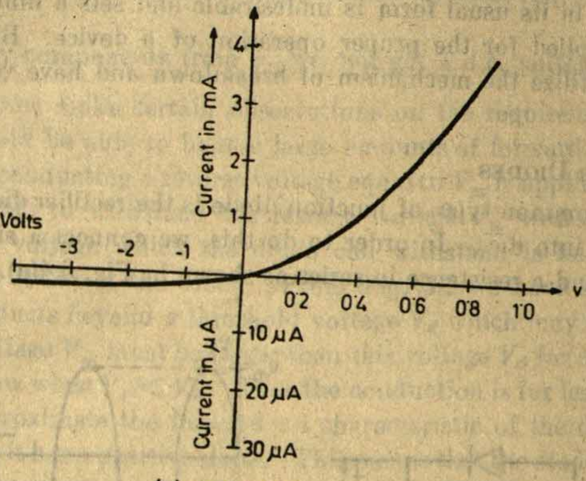
Similarly n_p the density of the electrons in the p-region will be

$$n_p = \frac{10^{38}}{10^{24}} = 10^{14}/\text{m}^3$$

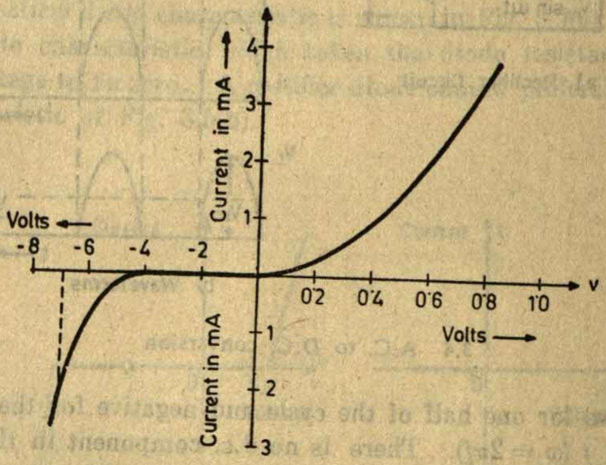
Thus, in the p region there are $10^{24}/\text{m}^3$ majority carriers and only $10^{14}/\text{m}^3$ minority carriers, that is, for 10^{10} majority carriers there is only one minority carrier. The situation on the n-side is similar where there are 10^6 majority carriers for every minority carrier. The reverse current caused by the minority carriers would thus be quite small. The electrons on the p side are pushed by the negative potential and are also aided by the potential barrier. Therefore, they go easily to the n side and then to the positive terminal of the battery. Similarly the holes from the n-side come to the negative terminal of the battery. I_s in eqn. (3.1.1) is this reverse saturation current. It depends on the density of the minority carriers, their rate of diffusion towards the junction and the temperature. This current reaches a saturation value even at a small reverse voltage because the density of the minority carriers is limited. They range in practical devices from 10 μA to 10 nA. The v-i characteristics for small forward and reverse voltages is shown in Fig. 3.3 (a).

What will happen if we go on increasing the reverse voltage across the diode ? From Fig. 3.3 and also eqn. 3.1.1 it appears that the current will reach a limiting value of I_s when the voltage is increased. But it is observed practically that if we continue to increase the reverse voltage, the reverse current suddenly shoots up as shown by the curve in Fig. 3.3(b). The voltage at which this phenomenon takes place is called the breakdown voltage. Under the breakdown condition the current really becomes unlimited and may burn up the device unless restricted by the external resistance or some other means. This breakdown is usually a reversible phenomenon. There are two distinct ways in which a breakdown occurs *viz.* Zener break down and avalanche breakdown. When the applied reverse potential is quite large, the electric field (potential per unit distance) in the device becomes quite large. Such a large electric field causes field emission of electrons i.e., the electrons from the valence band tunnel through the forbidden gap. This tunneling of electrons produces a large current and a Zener break down of the device is said to have occurred.

The second mechanism of breakdown, that is the avalanche breakdown, usually takes place in junctions having wide depletion regions. When the reverse voltage is increased the electrons from the *p* region are accelerated and gain enough energy to ionize the lattice. An electron with large energy knocks out a bound electron and raises it to the conduction band. It creates a hole in the valence band, and thereby an electron-hole pair is generated. The electron-hole pair in the transition region causes other pairs to be generated because it would knock out other bound electrons in turn. Thus the process multiplies such electron-hole pairs. The holes are accelerated in the opposite direction and they also generate electron-hole pairs. Since the creation of the electron-hole pair is



(a) near v = 0



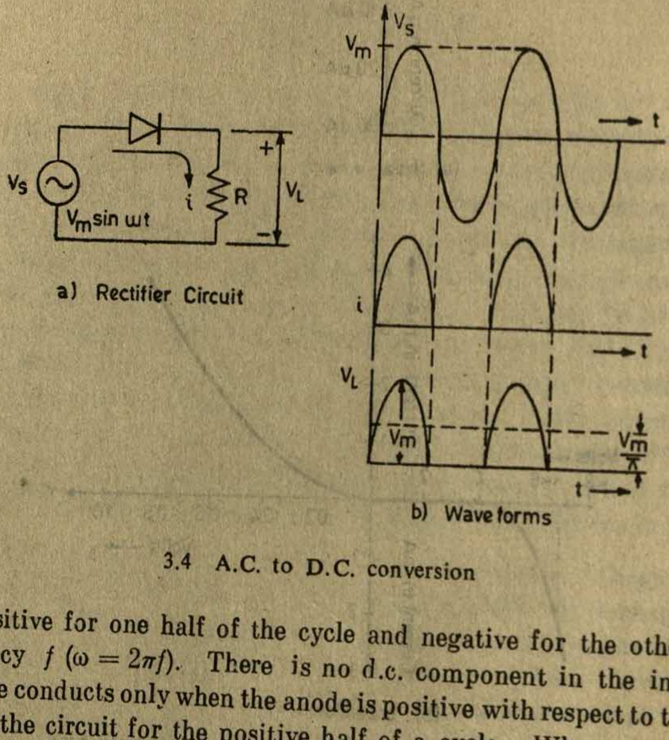
(b) breakdown

3.3 Diode characteristics under forward and reverse bias multiplicative, the current increases rapidly resulting in the breakdown of the device. The mechanism is known as avalanche breakdown.

Breakdown in its usual form is undesirable and sets a limit on the voltage which can be applied for the proper operation of a device. But some devices, discussed later, utilize the mechanism of breakdown and have very useful applications.

3.1.1 RECTIFIER DIODES

The most common type of junction diode is the rectifier diode. Its purpose is to convert a.c into d.c.. In order to do this, we connect a sinusoidal voltage source, a diode and a resistance in series as shown in Fig. 3.4(a). The sinusoidal voltage is positive for one half of the cycle and negative for the other half and has a frequency f ($\omega = 2\pi f$). There is no d.c. component in the input signal. Since the diode conducts only when the anode is positive with respect to the cathode, we get a i in the circuit for the positive half of a cycle. When v_S goes positive the anode becomes positive and the current i flows as shown in Fig. 3.4(b) When v_S is negative, no current flows as the diode is reverse biased. The voltage across the resistance R will have a waveform similar to that of the current i. The voltage v_L is a periodic waveform and can be analysed by the Fourier series. If the period of the waveform of v_L is $1/f$ and the maximum voltage is V_m then the Fourier series analysis shows that



a) Rectifier Circuit

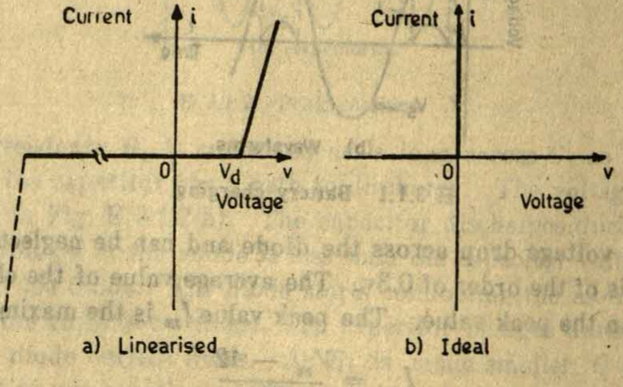
b) Wave forms

3.4 A.C. to D.C. conversion

$$v_L = \frac{V_m}{\pi}\left(1 + \frac{\pi}{2}\sin \omega t - \frac{2}{3}\,\text{Cos}\,2\omega t - \frac{2}{15}\cos 4\omega t + \ldots\ldots\right) \qquad (3.1.2)$$

We get a zero frequency or a d.c. component in the output v_L having an amplitude of $\frac{V_m}{\pi}$ and other high frequency components. By removing or filtering out the other frequency components from v_L we can get a d.c. voltage alone.

We can now make certain observations on the requirements of the diode. The diode should be able to handle large amounts of forward current ($\approx V_m/R$). When it is not conducting a reverse voltage equal to V_m is applied across the diode. It should be able to withstand the reverse voltage V_m without any breakdown. The maximum voltage which the diode can withstand is known as the peak inverse voltage (PIV) of the diode. From Fig. 3.2 we have seen that the diode practically conducts beyond a threshold voltage V_d which may be 0.3 or 0.7 volts. The applied voltage V_m must be larger than this voltage V_d for conduction. There is no current flow when $V_s < V_d$. Thus the conduction is for less than a half cycle. Even if we approximate the forward v-i characteristic of the diode by a straight line we find that it has a positive slope. This means that the diode offers a resistance to the forward current and that there would be a voltage drop across the diode. The output voltage would thus be reduced by this amount including V_d. A limearised practical diode characteristic is shown in Fig. 3.5(a). Fig. 3.5(b) shows an ideal diode characteristic which takes the diode resistance as well as the threshold voltage to be zero. A rectifier diode should preferably be closer to the ideal characteristic of Fig. 3.5(b).



a) Linearised b) Ideal

3.5 Characteristics of a diode

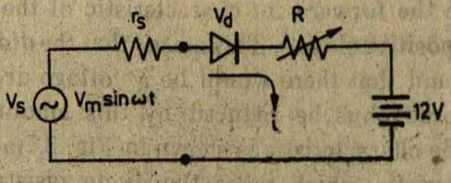
Under the forward biased condition when the diode conducts the resistance offered by it is called the forward resistance r_f of the diode. Similarly, when the diode is reverse biased the resistance offered by it is called the reverse resistance r_r of the diode. Typically r_f may be 50 to 100 ohms and r_r may be 50K to 100K ohms.

Example 3.1 Battery Charges

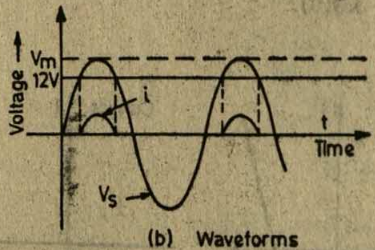
Unidirectional current is required for charging a battery. A diode is used to convert the alternating current into a unidirectional current as explained. A 12V battery is charged using a rectifier diode and an a.c. supply by a circuit arrangement shown in Fig. E3.1.1(a). The resistance r_s is the source resistance associated with the a.c. supply and may be neglected as it is very small in practical circuits. Whenever V_m sin (ωt) is more than 12 volts the diode conducts and a current i flows in the circuit as shown in Fig. E3.1.1(b). The variable resistance R can be adjusted to give the desired value of the charging current. The instantaneous charging current i is given by

$$i = \frac{V_m \sin \omega t - 12 - V_d}{r_s + R} \quad \text{for } v_S > 12\text{V}$$

$$i = 0 \quad \text{for } v_S \leqslant 12\text{V}$$



(a) Circuit



(b) Waveforms

E 3.1.1 Battery charging

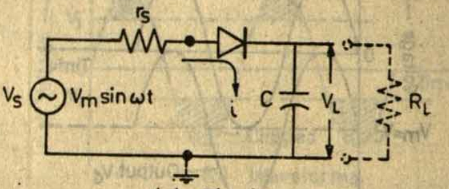
where V_d is the voltage drop across the diode and can be neglected with respect to V_m, since it is of the order of 0.3v. The average value of the charging current is much less than the peak value. The peak value I_m is the maximum of i and is

$$I_m = \frac{V_m - 12}{R}$$

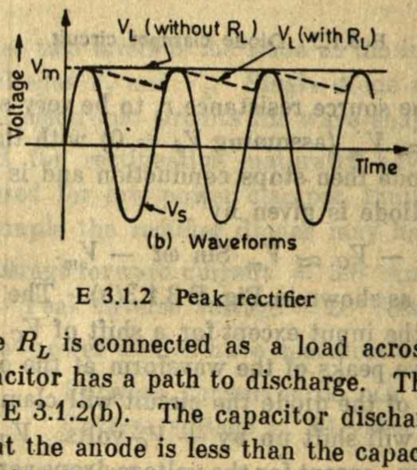
The average current can be computed using Fourier series. Normally the average charging current of a 12V battery is about 4A with $V_m \approx 18$ Volts.

Example 3.2 Peak rectifier

A peak rectifier using a diode is shown in Fig. E 3.1.2. Peak rectifiers are used where it is desired to obtain a d.c. voltage equal to the peak value of the input voltage. Let us assume that the capacitor C is uncharged and the supply voltage $v_S = V_m \sin \omega t$ is applied at $t = 0$. As the voltage v_S increases the diode conducts in the forward direction and C is charged. If the source resistance is very small then drop across it is negligible and the voltage v_L across C is almost equal to v_S at every instant till v_S reaches the peak value V_m. Thus the capacitor is charged to V_m. Now as the voltage v_S decreases the diode stops conducting because the cathode is at a potential V_m which is higher than the anode potential v_S. Since the capacitor C does not have a path to discharge, the charge accumulated in it is trapped. It is to be noted that the diode also does not conduct for the negative half cycle. The voltage across the capacitor is thus maintained at V_m and the voltage v_L is as shown in Fig. 3.1.2(b) (full line).



(a) Circuit



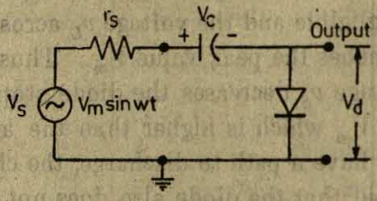
(b) Waveforms

E 3.1.2 Peak rectifier

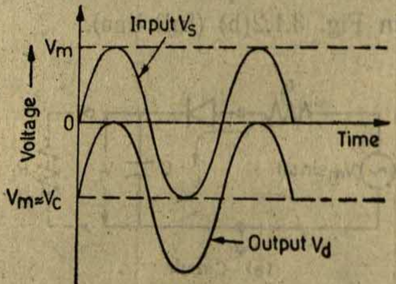
Now if a resistance R_L is connected as a load across C, as shown in Fig. E. 3.1.2(a), then the capacitor has a path to discharge. The voltage waveform is as shown dotted in Fig. E 3.1.2(b). The capacitor discharges during the period when the input voltage at the anode is less than the capacitor voltage appearing at the cathode of the diode. The diode starts conducting the moment the input voltage exceeds the capacitor voltage. The capacitor charges during this period and a pulsating diode current flows. As R_L is made smaller C discharges by a greater amount in every cycle and the ripple becomes larger in magnitude. By a proper selection of C and R_L a d.c. voltage which is almost equal to V_m can be obtained across R_L. This is in contrast with the rectifier circuit of Fig. 3.4 where a d.c. voltage of $\frac{V_m}{\pi}$ only is obtained.

Example 3.3 Clamper

When the diode and the capacitor in Fig. E 3.1.2 are interchanged, we obtain what is called a clamper circuit shown in Fig. E 3.1.3(a). As explained earlier the capacitor will be charged when the diode is conducting during the positive



(a) Circuit



(b) Waveforms

E 3.1.3 Diode clamper circuit

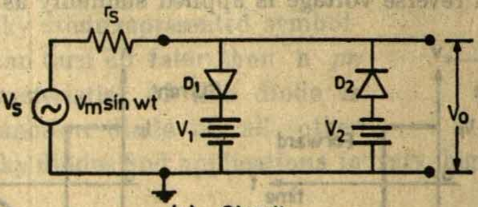
half cycle. Assuming the source resistance r_s to be very small, the capacitor will charge to a voltage $V_C \approx V_m$ (assuming $V_d = 0$) with the polarity as indicated in the diagram. The diode then stops conduction and is an open circuit ideally. The output across the diode is given by

$$V_d = V_m \text{ Sin } \omega t - V_C \approx V_m \text{ Sin } \omega t - V_m.$$

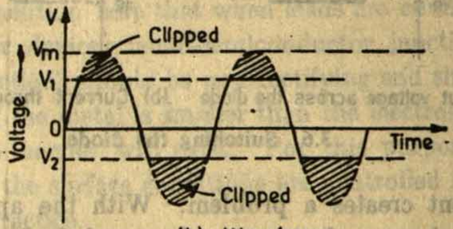
The output is, therefore, as shown in Fig. E 3.1.3(b). The waveform at the output is the same as that of the input except for a shift of $V_C \approx V_m$ Volts. Thus the circuit clamps the positive peaks of the waveform at the output to zero volts. If we reverse the direction of the diode the circuit will clamp the negative peaks to zero and the waveform will shift up by $+ V_C$ volts. V_C is almost equal to V_m volts, as mentioned earlier, except for the voltage drops across the r_s and the diode. Clampers find wide applications in TV circuits and voltmeters etc.

Example 3.4 Clipper

One of the important applications of the diode is as a limiter or a clipper as shown in Fig. E 3.1.4(a). Once the input voltage v_s exceeds V_1 the diode D_1 conducts, but D_2 does not because it is connected in the reverse direction. As a result the voltage v_o does not go above V_1. Similarly on the negative swing of the input the diode D_2 conducts but D_1 does not and thus clips the input voltage so that the output does not exceed $-V_2$ Volts. The output voltage v_o is as shown in Fig. E 3.1.4(b). The source resistance r_s should be much larger than the forward resistance of the diodes but should be much smaller than the reverse resistance of the diodes. This circuit thus limits the output to $+V_1$ and $-V_2$. The output



(a) Circuit



(b) Waveforms

E 3.1.4 Diode limiter

waveform between these two levels is the same as the input. The clipping levels are adjusted by the voltages V_1 and V_2. Single diode and double diode limiters are used extensively in electronic circuits for wave shaping.

The diodes used for rectification naturally have voltage-current ratings different from those used for low power clamper, limiter and peak rectifier etc. applications. For example the rectifier diodes may have following ratings.

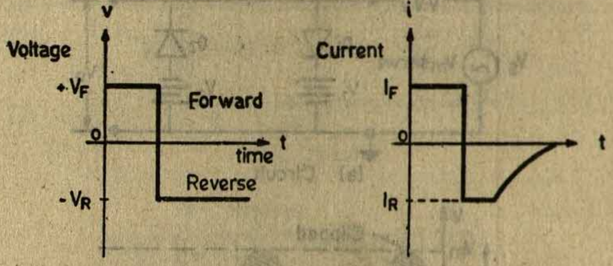
Average forward current = 3.8 Amperes
Peak inverse voltage = 20 Volts

On the other hand low power diodes have specifications like

Forward current = 35 mA
Reverse voltage = 30 Volts.

3.1.2 SCHOTTKY BARRIER DIODE

A diode acts as a switch by allowing a current to flow when the anode to cathode voltage is positive. If the voltage is made negative or is removed from the anode then the diode should ideally switch off the current. This is shown in Fig. 3.5(b) where there is no current when the voltage is negative. This ideal characteristics is not achieved in the junction diodes particularly when the speed at which the diode is required to be switched off is very high. The cause of the failure is the life time of the carriers. When a forward voltage is applied, the electrons from the *n*-side are injected across the transition region into the *p*-side where they are minority carriers. Near the junction, thus, there is an excess of minority carriers. They either recombine with the holes or are swept out by the field. The recombination is dependent upon the life time of the carriers. During this period there is a storage of charge carriers. When the forward voltage is either removed or a reverse voltage is applied suddenly as shown in Fig. 3.6, the

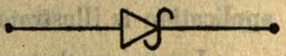


(a) Input voltage across the diode .(b) Current through the diode

3.6 Suitching the diode

stored charge present creates a problem. With the application of the reverse voltage these stored charges, electrons in the *p* and the holes in the *n* region, move in the opposite direction giving rise to a large reverse current flowing across the junction when ideally it should have been zero. The reverse current approaches zero gradually as the excess minority carriers move out of the transition region. Thus the diode would not work as a switch or as a rectifier at very high frequencies.

Instead of a *pn* junction diode, a metal-semiconductor junction diode can also be made. These diodes do not have the problem of carrier storage. They are known as Schottky barrier diodes. The Schottky diode consists of a junction between a metal such as platinum, gold or silver and an extrinsic *n* or *p* type semiconductor. Let us assume an *n*-type semiconductor for the purpose. Metals have a work function defined as the minimum energy required for an electron to escape into vacuum. This energy is the difference of the energy between the Fermi and the vacuum levels. For semiconductors the difference between energy of the vacuum level and that of the bottom of the conduction band is known as electron affinity. When a junction is formed between a metal and a semiconductor, the Fermi levels on both sides get aligned or line up. The difference of energy between the work function of the metal and the electron affinity of the semiconductor forms a barrier to the electron flow. Due to this barrier, known as the Schottky barrier, the electrons at thermal equilibrium can not go from the semiconductor side to the metal. side. Now if forward bias is applied, the electrons gain enough energy to cross the barrier and go to the metal side where there are already a large number of electrons. The electrons are majority carriers in the semiconductor and remain so in the metal after crossing over to the other side. This is very unlike a *pn* junction where the electrons after crossing over become minority carriers in that region. If a reverse voltage is applied to the device, the electrons in the metal cannot overcome the barrier and therefore no conduction takes place. The metal-semiconductor junction is thus unidirectional and behaves as a diode. Obviously, there is no charge storage in the metal-semiconductor junction, hence the diode would switch off as soon as the reverse potential is applied. The Schottky diode represented symbolically as in Fig. 3.7 can turn off fater than a *pn* diode. The *v-i* characteristics of this diode is similar to the *pn* junction diode in all other respects. The Schottky diodes find applications in very high frequency and fast digital circuits.

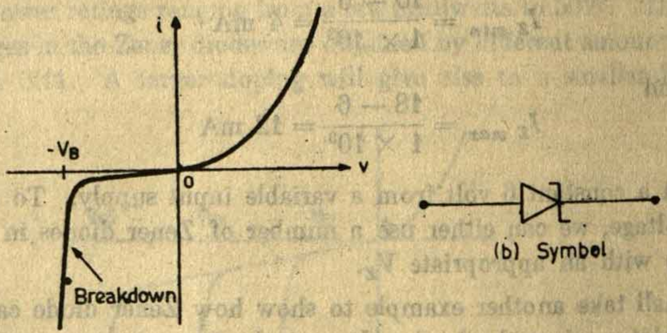


3.7 Schottky diode

It is relevant to mention here that when leads are connected to the *pn* diodes or other semiconductor devices metal-semiconductor junctions are automatically formed. But these junctions should be non-rectifying and should be purely ohmic. If the work function of the metal is smaller than the electron affinity of the *n*-type semiconductor then no barrier will exist. For this purpose therefore the metal is chosen carefully and the surface conditions are controlled in addition to produce an ohmic contact in practice.

3.1.3 ZENER DIODES

We have shown that when a *pn* junction is reverse biased it breaks down at a particular voltage V_B as shown in Fig. 3.8. We observe from the characteristic



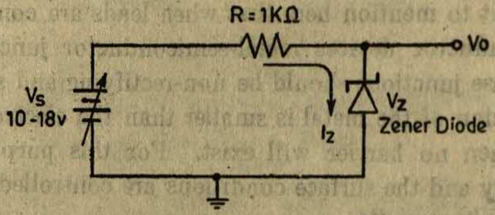
(b) Symbol

(a) Breakdown Characteristic

3.8 Zener diode

that the reverse current is small for small reverse voltages. When the reverse voltage equals $-V_B$, the reverse current shoots up and is limited by the external circuit only. The voltage V_B remains constant for a wide range of currents. If now the reverse voltage is reduced below V_B, the current again becomes small. Thus as the reverse voltage is brought back to zero, the characteristic of Fig. 3.8 is retraced. Such a breakdown is therefore called a reversible breakdown. Large breakdown current may destroy the diode because of excessive heating. To prevent destruction of the diode, the current should be limited by external curcuit and proper heat dissipation capability should be provided. This diode is known as the Zener diode. The characteristic of the Zener diode can be utilized with advantage to produce a voltage reference. That is, this diode can be used as constant voltage source particularly where the variations of either the load current or the input supply voltage are likely to change the load voltage. Such an application is illustrated by the following example.

Let us say that we want a 6 Volt source when we have available a supply V_S varying from 10 to 18 Volts. We shall choose a Zener diode with a Zener voltage $V_Z = V_B = 6V$ and connect it as shown in Fig. 3.9. Since the Zener diode is reversed biased and the V_S is always larger than V_B, a breakdown occurs. The voltage V_O across the diode is +6 Volts as desired. The resistance R is connected in order to limit the current. The minimum and maximum Zener currents are



3.9 Use of Zener diode as a constant voltage source

$$I_{Z\,min} = \frac{10-6}{1 \times 10^3} = 4 \text{ mA}$$

and

$$I_{Z\,max} = \frac{18-6}{1 \times 10^3} = 12 \text{ mA}$$

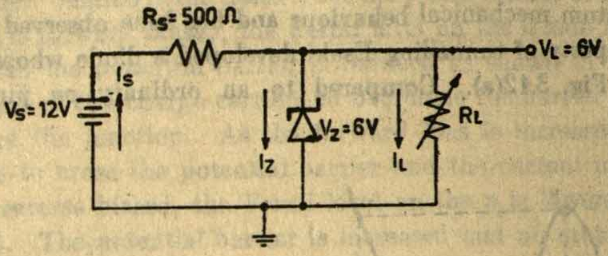
Thus we get a constant 6 volt from a variable input supply. To obtain a higher reference voltage, we can either use a number of Zener diodes in series or use a Zener diode with an appropriate V_Z.

We shall take another example to show how Zener diode can be used as a voltage regulator when the load voltage is kept constant even though the load current is changing. The load voltage varies for different load currents because of the change in the voltage drop across the source resistance. Let us suppose that the load current I_L is likely to change from 0 to 8 mA but the load voltage is required to be constant at 6V. Taking a 12V supply and a 6V Zener diode we can connect them in the circuit shown in Fig. 3.10 to achieve the desired regulation. An $I_L = 0$ will mean that the effective load is open circuit and an $I_L = 8$ mA mean that $R_L = V_L/L_L = 750\ \Omega$.

Now, for $R_L = \infty$ and $I_L = 0$, we have the Zener current $I_Z = I_S$ and

$$I_S = \frac{V_S - V_L}{R_S}$$

$$= \frac{12-6}{500} = 12 \text{ mA}$$



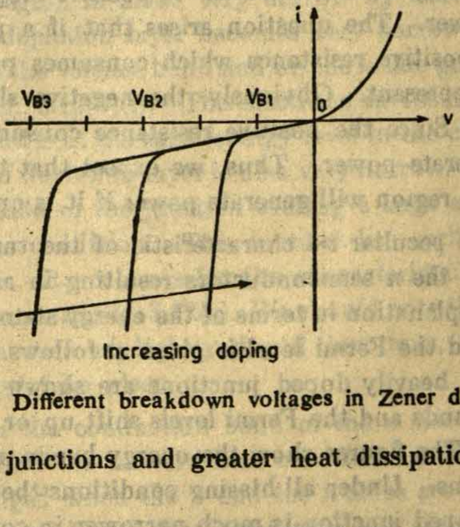
3.10 Zener voltage regulator

when $R_L = 750\ \Omega$ and $I_L = 8$ mA, I_S remains the same because V_S, V_L and R_L are constant. Since $I_S = I_Z + I_L$, I_Z changes as I_L does.

Thus $\qquad I_Z = I_S - I_L = 12 - 8 = 4$ mA.

Since V_S is higher than V_B and the Zenor current is varying between 12 and 4 mA, the Zener breakdown is maintained and the voltage across R_L is held at 6V in spite of the changes in the load current.

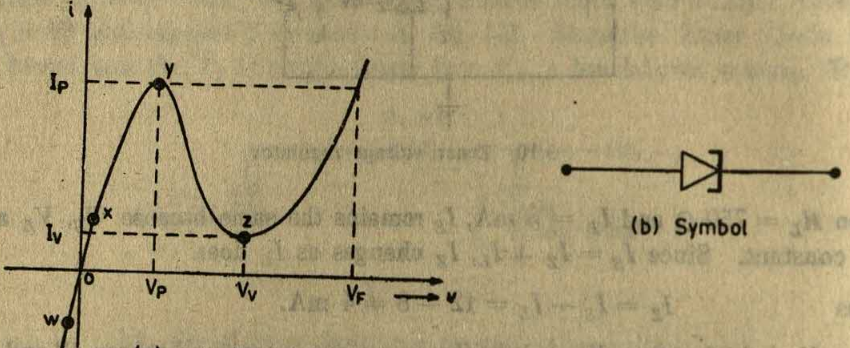
Zener diodes for a wide range of voltages from 3 to 100 Volts are available. They have wide power ratings ranging from a few milliwatts to 50W. The different breakdown voltages in the Zener diodes are obtained by different amount of doping as shown in Fig. 3.11. A larger doping will give rise to a smaller breakdown voltage. Larger size junctions and greater heat dissipation capability will give large power rating.



3.11 Different breakdown voltages in Zener diodes

3.1.4 TUNNEL DIODE

We know that the depletion layer which constitutes a potential barrier in the *pn* junction depends on the impurity concentrations. When the doping is increased heavily the width of the depletion layer reduces considerably. If the depletion layer is very narrow i.e., of the order of 100 A° or less the electrons can tunnel through the potential barrier and go to the other side of the junction. This is a quantum mechanical behaviour and has been observed in many devices. Using this property of tunnelling Esaki developed a diode whose *v-i* characteristic is shown in Fig. 3.12(a). Compared to an ordinary *pn* junction diode, the characteristic of the tunnel diode is very different and interesting. The most significant part of the characteristic is the small range of voltage V_p to V_v where the current decreases as the applied voltage across the diode increases. Usually the current increases as the voltage is increased and the *v-i* curve has a positive slope in most of the devices and circuits. A positive slope indicates a resistance which consumes power. The question arises that if a positive slope of the *v-i* curve represents a positive resistance which consumes power than what does a negative *v-i* slope represent. Obviously, the negative slope should represent a negative resistance. Since the positive resistance consumes power, the negative resistance must generate power. Thus, we expect that the tunnel diode having a negative resistance region will generate power if it is operated over this region.



(a) v-i characteristics

(b) Symbol

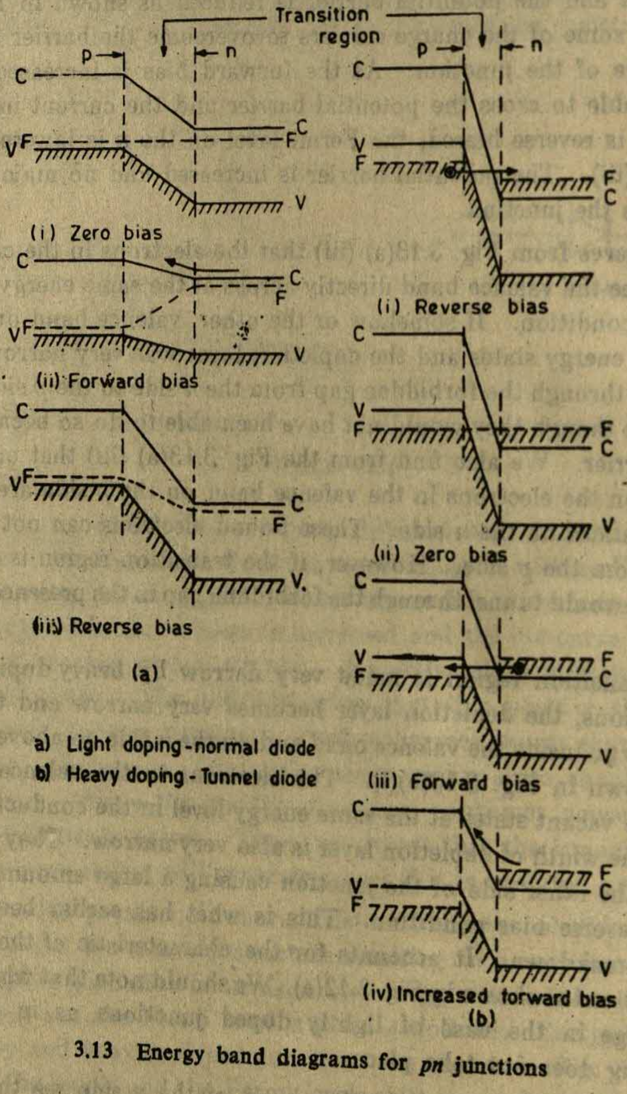
3.12 Tunnel diode

The key to the peculiar *v-i* characteristic of the tunnel diode is the heavy doping of the *p* and the *n* semiconductors resulting in a very narrow transition region. A simple explanation in terms of the energy states of the condition band, the valence band and the Fermi level is given as follows. Energy band diagrams for both lightly and heavily doped junctions are shown in Fig. 3.13(a) and (b) respectively. The bands and the Fermi levels shift up or down when an external voltage is applied. The figures show the energy bands under zero, forward and reverse bias conditions. Under all biasing conditions the width of the transition region for heavily doped junction is much narrower in comparison to that of the lightly doped ones. With heavy doping the bands are steeply tilted. Let us now consider the current flow in both these types of junctions. In the normal diode with light doping, the Fermi levels on the *p* and the *n* sides are aligned under zero bias conditions as shown in Fig. 3.13(a) (i). Because of the potential barrier, the electrons from the conduction band of the *n* side cannot go to the conduction band of the *p* side. Similarly the holes from the *p* side cannot come to the *n* side. As the junction is forward biased, the Fermi level on the *n* side rises above that on the *p* side and the potential barrier is reduced as shown in Fig. 3.13(a) (ii). This enables some of the charge carriers to overcome the barrier and go over to the other side of the junction. As the forward bias is increased, more charge carriers are able to cross the potential barrier and the current increases. When the junction is reverse biased, the Fermi level on the *n* is lowered as shown in Fig. 3.13(a) (iii). The potential barrier is increased and no majority carriers are able to cross the junction.

We observe from Fig. 3.13(a) (iii) that the electrons in the conduction band are able to see the valence band directly across at the same energy level under the reverse bias condition. If somehow or the other, valence band on the *p* side had some vacant energy states and the depletion layer was very narrow, the electrons could tunnel through the forbidden gap from the *n* side to the *p* side and cross the junction even though they would not have been able to do so because of the large potential barrier. We also find from the Fig. 3.13(a) (iii) that under the reverse bias condition the electrons in the valence band on the *p* side are able to see the unoccupied states on the *n* side. These bound electrons can not normally go to the *n* side from the *p* side. However, if the transition region is made extremely narrow, they would tunnel through the forbidden gap in the presence of high electric field.

The transition region is made very narrow by heavy doping. In heavily doped junctions, the depletion layer becomes very narrow and the Fermi levels on the *p* side go inside the valence band and on the *n* side go above the conduction band as shown in Fig. 3.13(b)(i). The electrons in the valence band on the *p* side now see vacant states at the same energy level in the conduction band of the *n* side and the width of depletion layer is also very narrow. They therefore tunnel through to the other side of the junction causing a large amount of current even under the reverse bias condition. This is what has earlier been referred to as the Zener breakdown. It accounts for the characteristic of the tunnel diode in the 3rd quadrant as shown in Fig. 3.12(a). We should note that when the transition width is large in the case of lightly doped junctions, as in Fig. 3.13(a)(iii), the tunneling does not take place.

The electrons in the conduction band of the *n* side see the forbidden gap both under the zero and the forward bias conditions in lightly doped junctions. This situation is changed when the *p* and the *n* sides are heavily doped. When such a junction is forward biased the Fermi level goes above the conduction band on the *n* side and below the valence band on the *p* side as shown in Fig. 3.13(b) (iii). The electrons from the *n* side tunnel through to the *p* side under small forward bias conditions and we get a current as shown by the point *x* inFig. 3. 12(a). At the zero bias condition, the Fermi levels are aligned on both the *p* and the *n* sides as shown in Fig. 3.13(b) (ii). Here the electrons in the conduction band on the *n* side see the filled states in the valence band of the *p* side and there is no current at the zero bias. As the forward bias is increased, the forward current increases



3.13 Energy band diagrams for *pn* junctions

because more and more electrons see more and more vacant states on the other side of the junction. This way the current keeps on increasing as the small forward voltage is increased until it reaches the maximum point, marked *y* in the Fig. 3.12(a). When the forward bias is further increased, the electrons in the conduction band on the *n* side start overlapping the forbidden gap on the *p* side and lesser number of electrons see the empty valence band states directly across on the opposite side. This reduces the tunnel current. As the bias goes on increasing, larger number of electrons see the forbidden band and the current goes on reducing until it becomes small, corresponding to the point z in Fig. 3.12(a). The energy band diagram for this situation is shown in Fig. 3.13(b) (iv). Beyond this forward voltage, the bottom of the conduction band on the n side is at or above the top of the valence band on the p side and none of the electrons see any empty states directly across. In fact they see only the forbidden gap. The tunneling therefore stops.

With a further increase in the forward voltage the electrons would cross the potential barrier as in the lightly doped diode resulting in the conventional diode current. The characteristic of the tunnel diode is similar to that of a conventional *pn* junction diode beyond this forward voltage. Thus we see that the tunneling current flows with small reverse voltage as shown by the point w and keeps on steadily increasing till the forward voltage corresponding to the point y is reached, Fig. 3.12(a). The tunneling current starts decreasing with further increase in the forward voltage and gives rise to the famous negative-resistance characteristic. Once the tunneling current reaches the minimum level, the normal diode current starts flowing with the increasing forward bias. We can say that the Zener breakdown taking place for the reverse voltages and extends even for small forward voltages. The discussion above has all through been confined to the movement of electrons only, but it holds for the movement of holes as well.

Since the tunnelling takes place at very high speed, almost the speed of light, the tunnel diodes find applications in high speed switching. Tunnel diodes are also used to make microwave amplifiers and oscillators.

3.1.5 VARACTOR DIODE

In a *pn* junction the majority carriers move away from the junction when it is reverse biased. As a result more immobile charges are uncovered near the junction. The charges are of opposite polarity and the width of the space charge increases with the applied voltage. Change of charge with voltage produces a capacitive effect given by

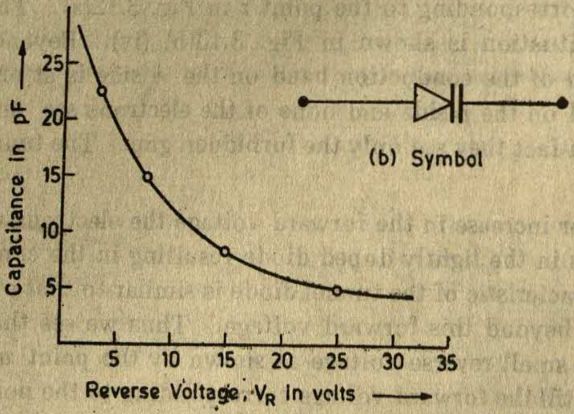
$$C = \frac{dq}{dV} \tag{3.1.2}$$

This capacitance is known variously as the transition, space charge, barrier or depletion region capacitance. It varies with the reverse voltage V_R as

$$C \propto V_R^{-n}$$

where n is a number depending on the type of junction and the level of doping. For an abrupt junction $n = 0.5$. Typical transition capacitance as a function of reverse voltage V_R is shown in Fig. 3.14(a).

The *pn* junction diodes specially made for the purpose of producing voltage variable capacitance are known as Varactors, Varicaps or Voltacaps. The term varactor comes from variable reactor and the varactor diode is symbolically represented as in Fig. 3.14(b). The varactor diodes are used in parametric amplifiers, harmonic generators, mixers, modulators and voltage variable tuning circuits. We know that the resonant frequency of a parallel tuned circuit of L and C is given by

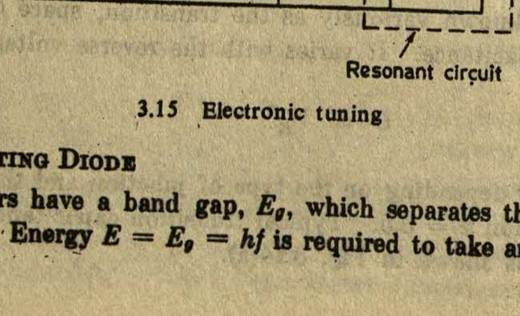


(a)

3.14 Varactor diode

$$f_r = \frac{1}{2\,\pi\,\sqrt{LC}}$$

If a varactor diode is connected in parallel with C, the circuit can be electronically tuned by simply varying a voltage as shown in Fig. 3.15. In fact, tuning can now be done from remote locations.



3.15 Electronic tuning

3.1.6 LIGHT EMITTING DIODE

Semiconductors have a band gap, E_g, which separates the valence and the conduction bands. Energy $E = E_g = hf$ is required to take an electron from the valence band to the conduction band. Such a transition generates an electron-hole pair. When the excited electron falls from the conduction band to the valance band while recombining with the hole, the energy $E = hf$ is emitted in the form of radiation. In the *pn* junction diodes the recombination of charge carriers takes place somewhere inside the structure. The recombination in the Silicon and Germanium takes place mostly through traps and the liberated energy goes into heating of the crystal. We do not get this energy in the form of light. But the semiconductors of III-V group such as the Gallium Arsenide and the Gallium Phosphide have direct band gap i.e. the minimum of the lowest conduction band and the maximum of the highest valance band are at the same wave vector in the Brillouin zone. As a result of this the recombination is direct and the energy released appears as a radiation. The radiation will be at a frequency f, or wave wave length λ, which is equal to E_g/h Thus

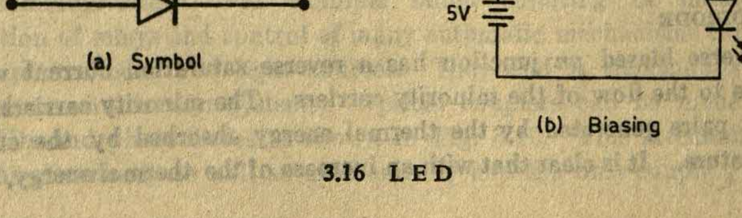
$$\lambda = \frac{c}{f} = \frac{c.h}{E_g}$$

For GaAs, the bandgap $E_g = 1.45$ eV

Therefore,
$$\lambda = \frac{3 \times 10^8 \times 6.625 \times 10^{-34}}{1.45 \times 1.602 \times 10^{-19}} \text{ m}$$
$$= 850 \text{ nm}$$

We know that the range of visible light is from about 400 to 720 nm. Thus the radiation ($\lambda = 850$ nm) from the GaAs diode is in the infra-red region. The bandgap of GaAsP (with a particular doping) is about 1.9 eV and the radiation is at 650 nm (red) which is visible. Thus, by a proper choice of the bandgap and the material, radiation of desired wave length may be obtained.

Such a *pn* diode which is specifically made to give emission in the visible region is known as the Light Emitting Diode (LED) and is shown symbolically in Fig. 3.16(a). Since the radiation occurs when the electrons and the holes recombine, the majority carriers are required to cross the junction. The diode is therefore,

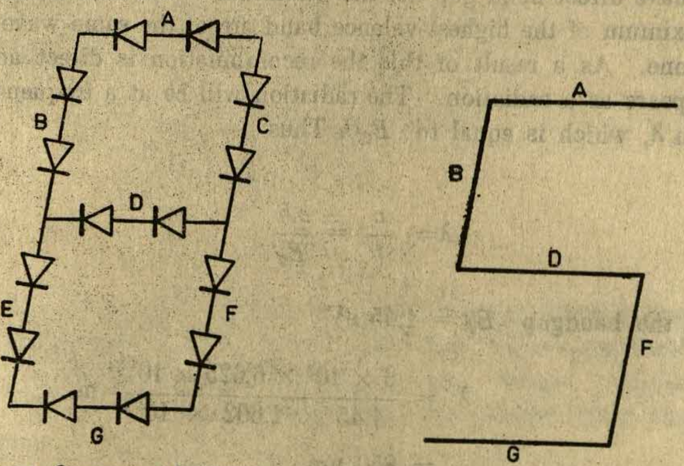


(a) Symbol (b) Biasing

3.16 LED

forward biased to produce a radiation as shown in Fig. 3.16(b). The LED takes tens of milliamperes of current.

Compared with the incandescent light sources, the LEDs consume much less power and have longer life. An important feature of the LED is that it can be switched on and off at a fast speed. LEDs find many applications in numeric displays, like watches, calculators, instrument panels etc. and optical communication. In numeric displays one or more LEDs are arranged per segment in a 7-segment configuration as shown in Fig. 3.17 (a). The LEDs of each segment have separate drive circuits to switch them on. A particular numeral is displayed depending on the segments that are driven. For example driving and switching on the segments A B D F and G displays the numeral 5. If all the seqments are switched on simultaneously we shall get a display of 8 (eight).



(a) Seven Segments ABCDEFG

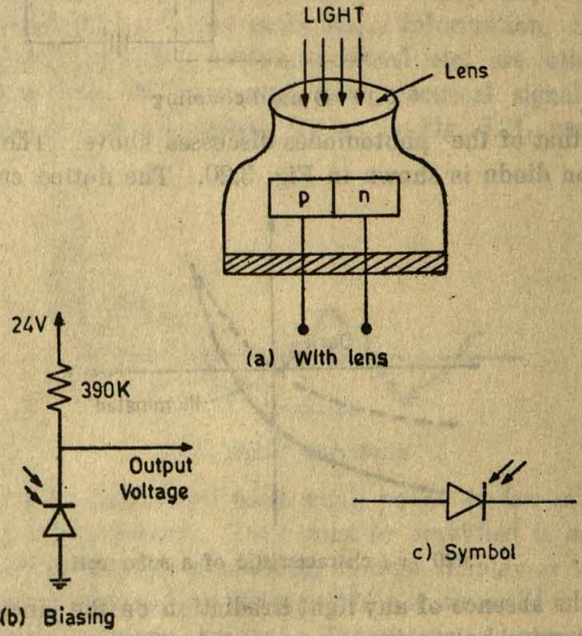
(b) Numeral 5

3.17 LED numeric display

The light emitted by the LEDs is incoherent in the sense that all the emitted photons are not emitted in phase primarily because recombination occurs at random times. When the photons are emitted in phase, particularly when the radiated photon is in phase with the incident photon, we get a coherent light. A coherent light source is called a LASER (Light Amplification by Stimulated Emission of Radiation). Under certain appropriate conditions *pn* junctions are made to radiate coherent light.

3.1.7 PHOTODIODE

The reverse biased *pn* junction has a reverse saturation current which is primarily due to the flow of the minority carriers. The minority carriers are the hole-electron pairs generated by the thermal energy absorbed by the crystal at room temperature. It is clear that with an increase of the thermal energy, brought about by an increase of the temperature, more electron-hole pairs will be generated resulting in an increase in the reverse saturation current. Now, if the *pn* junction is irradiated by light energy, in place of the thermal energy, then once again the electron- hole pairs would by generated and the current through the diode would increase. Thus light can be detected using a reverse biased *pn* junction diode known as the photodiode. Sometimes, a lens is placed on the junction side of the photodiode so that incident light can be focussed on to the surface for maximum activity, as shown in Fig. 3.18 (a). Reverse biasing of the photodiode is shown in Fig. 3.18 (b) and the symbol for the photodiode is shown in Fig. 3.18 (c). The reverse current through the diode increases when light is incident on it and the voltage drop across the resistance increases. The changes in the output voltage are proportional to the incident light. This output signal is amplified by a low-noise high input impedance amplifier for further processing.



(a) With lens

(b) Biasing

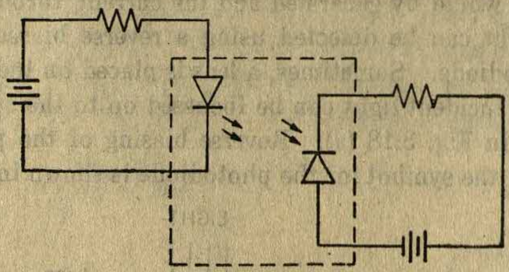
c) Symbol

3.18 Photodiode

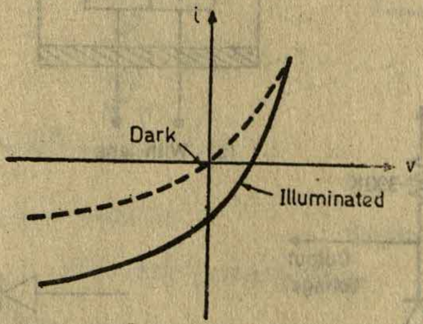
Photodiodes find many applications, in instrumentation, control, automation and communication. For example batch counting of industrial products, operation of relays and control of many automatic mechanisms can be carried out using photodiodes and light sources. They find a tremendous application in optical communication systems. Optical couplers can be made with the help of LEDs and photodiodes as shown in Fig. 3.19. This mechanism isolates two systems electrically as well as mechanically and the only coupling is by means of light.

3.1.8 SOLAR CELLS

Solar cells are large area Photodiodes operated at zero bias voltage. They convert solar light energy into electrical energy. The principle of their operation is the same as that of the photodiodes discussed above. The *v-i* characteristics of a *pn* junction diode is shown in Fig. 3.20. The dotted curve marked 'dark' is obtained in the absence of any light irradiation on the junction. As light falls on the junction extra hole-pairs are generated. These carriers would produce a short circuit current when the diode is externally shorted by a wire. Thus the Photodiode acts as a current source with zero external bias. It amounts to saying that the characteristic of the diode is shifted. The solid curve in Fig. 3.20 shows the characteristic under illumination. We observe from the curve that at zero current there is a voltage across the diode. The open circuit voltage of the Silicon solar cell is 0.55V and the short circuit current is about 35mA/cm². The power conversion efficiency is about 15%. Many such cells are mounted on big panels to generate large quantities of electrical power. Satellites and space vehicles depend solely on solar cells for their power requirements to operate various electronic and other equipments. The solar cells are receiving more attenton even for the terestrial electric power generation.



3.19 Optical coupling

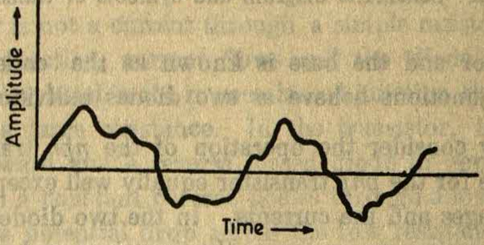


3.20 *v-i* characteristic of a solar cell

3.2 Transistor

Transistors are three terminal semiconductor devices. They find a number of applications in electronic circuits. In analogue circuits their basic function is to amplify a signal while in digital circuits they act as a switch or a gate. We shall describe the amplification property of the transistor in some detail first and take up the discussion of digital circuits later.

To start with let us understand what we mean by the term 'signal' and its amplification. Information, message or intelligence existing primarily in any form when converted into the electrical form will be known as a signal. The signal is unpredictable and varies with time. Examples of signals in engineering, science and everyday life are countless in number. For instance, the variations of physical parameters like fluid pressure, fluid velocity, stress, strain, temperature, heartbeat of a patient etc. are a few examples of information. Similarly speech, image, television, still pictures, written material etc. are other examples of information. These can be converted into electrical signal by appropriate transducers. These transduced signals, shown in Fig. 3.21, usually have small amplitudes (a few microvolts) and have small power (a few microwatts) at the source where they are generated. They must be amplified in amplitude as well as in power for any subsequent processing, storage, display or transmission to a distant place. It is important that the signal is not distorted in any fashion and its waveform is preserved by the amplifier. Transistors and vacuum tubes perform the task of this amplification very well.

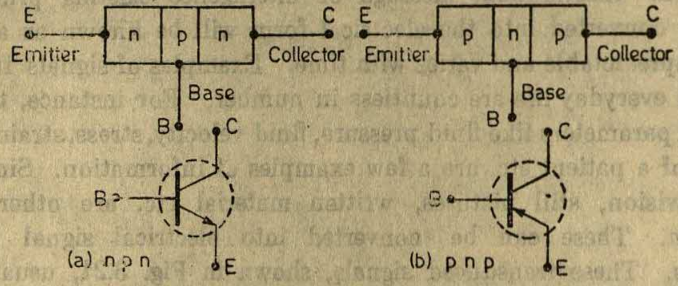


3.21 Signal warveform

Primarily there are two kinds of transistors—the unipolar and the bipolar. When the charge carriers in a transistor are only of one kind we have what is called a unipolar transistor such as the Field Effect Transistor (FET). There are many varieties of FETs now. If both the majority and the minority charge carriers participate in the operation of the device then we get what is called a Bipolar Junction Transistor (BJT). Historically the BJT was commercially manufactured earlier. We shall describe the operation of the junction transistors first.

3.2.1 BIPOLAR JUNCTION TRANSISTOR

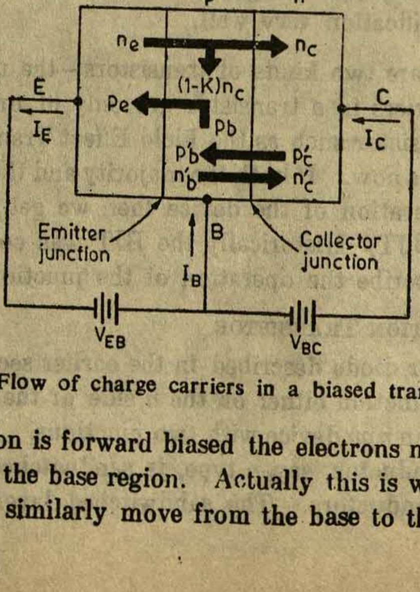
A semiconductor diode described in the earlier section has one *pn* junction. If we grow another junction either on the *n* side or the *p* side of the diode then we shall get a *pnp* or an *npn* device with two junctions. Here one layer of a particular type of semiconductor, say *p* type, is sandwitched between the two layers of the *n* type semiconductors. The sandwitched layer is very thin. Both the *npn* and *pnp* devices act as transistors and are shown schematically and symbolically in Fig. 3.22. Each of the three layers have metal contacts and terminals are brought out marked as Emitter E, Base B and Collector C. The junction between the emitter and the base, Fig. 3.22, is called the emitter junction and the junction between the collector and the base is known as the collector junction. In fact each of these two junctions behave as two diodes individually.



3.22 Schematic diagram and symbols of transistors

We shall now consider the operation of the *npn* transistor in detail. The arguments hold true for the *pnp* transistor equally well except for the change in the polarity of the voltages and the currents. In the two diodes of the *npn* transistor, thus, the majority carriers move across the junctions and create potential barriers at the thermal equilibrium. The depletion layers at the two junctions prevent further movement of free carriers across the junctions.

We now apply external voltages in such a way that the emitter junction is forward biased and the collector junction is reverse biased as shown in Fig. 3.23.



3.23 Flow of charge carriers in a biased transistor

Since the emitter junction is forward biased the electrons move from *n* to *p* region i.e. from the emitter to the base region. Actually this is why this region is called the emitter. The holes similarly move from the base to the emitter region in the forward bias condition. However, the movement of the electrons injected into the base region is more interesting to us here. These electrons are the minority carriers in the base region and their density at the emitter junction is high. They diffuse through the small base region and go to the collector junction without any significant recombination with the holes in the base region. It is easy to see that in order to avoid recombination in the base region the base region has to be very narrow. Once the electrons reach the collector junction they are swept away by the accelerating field of the reverse biased collector junction. They are once again the majority carriers in the *n*-region of the collector. As a result of this kind of biasing, therefore, the main action that takes place is that the emitter injects majority carriers which diffuse through the base as minority carriers without much recombination and are collected by the collector as majority carriers. Thus electrons flow from emitter to collector or equivalently a current flows from C to E in an *npn* transistor. In a *pnp* transistor the holes move from the emitter to the collector.

This current flow is not a current through a simple resistor. Let us see why. In a forward biased junction, current flows and the diode offers only a small resistance. One the other hand in the reverse biased junction there is no conduction and the diode offers a large resistance. In the transistor, however, the current flowing through a forward and a reverse biased diode in series is practically the same. In other words a constant current floews through a low resistance and then a high resistance. The potential drop across the low resistance is small and that across the high resistance is large. If we can associate the input signal voltage with the forward biased junction and the output signal voltage with the reverse biased junction then we can get the desired signal amplification. It is indeed interesting to know that the word TRANSISTOR has been derived from Transfer Resistor which takes place between the two junctions.

So far we have discussed only the flow of electrons injected across the forward biased emitter junction and their subsequent fate. There will be no injection of electrons into the base from the collector across the reverse biased junction. But the thermally generated holes from the *n* type collector and the electrons from be the *p* type base would be crossing the collector junction.

We can now have a balance sheet of the flow of various charge carriers and the resulting currents at the E, B and C terminals external to the device.

At the Emitter — (1) Electrons n_e injected by the emitter into the base give rise to a current I_{ne} coming out of the terminal E.

(2) The holes p_e which have been injected by the base into emitter side give a current I_{pb} coming out of the emitter.

Therefore the emitter current $I_E = I_{ne} + I_{pb}$ (3.2.1(a))

At the Base — (1) Out of n_e electrons from the emitter say kn_e diffuse to the collector. The rest $(1\text{-}k)\ n_e$ recombine in the base region to give a current (1-k) I_{ne} into the base terminal.

(2) The holes p_b give I_{pb} into the base ;

(3) The thermally generated electrons n'_b give a current $I_{n'b}$ out of the base terminal.

(4) The thermally generated holes from collector $p'_c = p'_b$ give a current $I_{p'c}$ out of the base terminal.

Therefore, the base current $I_B = (1\text{-}k)I_{ne} + I_{pb} - I_{n'b} - I_{p'c}$ (3.2.1(b))

At the Collector — (1) The diffused electrons $n_c = kn_e$ from the base give a current $I_{nc} = kI_{ne}$ into the collector terminal.

(2) Thermally generated holes p'_c give a current $I_{p'c}$ into the collector terminal.

(3) Thermal by generated electrons from the base region $n'_b = n'_c$ give a current I'_{nc} into the collector.

Therefore the collector current

$$I_C = kI_{ne} + I_{p'c} + I_{n'c} \qquad (3.2.1\text{ (c) })$$

Hence $I_B + I_C = (1\text{-}k)\, I_{n\varepsilon} + I_{pb} - I_{n'b} - I_{p'c} + kI_{nc} + I_{p'c} + I_{n'c}$

(3.2.1 (d))

We know that $I_{n'c} = I_{n'b}$ and $I_{p'c} = I_{p'b}$.

Hence eqn. (3.2.1 (d)) can be simplified to

$$I_B + I_C = I_{ne} + I_{pb} \qquad (3.2.2)$$

The right hand side of eqn. (3.2.2) is the same as the emitter current I_E of eqn. (3.2.1 (a)). Thus

$$I_E = I_B + I_C \qquad (3.2.3)$$

The eqn. (3.2.3) can also be obtained intuitively by applying Kirchoff's current law to the device as a whole.

Now $I_{p'c} + I_{n'c} = I_{co}$ and is defined as the reverse saturation current. Therefore, the collector current in eqn. (3.2.1 (c)) can be written down as

$$I_C = I_{nc} + I_{co} \qquad (3.2.4)$$

where $k = \dfrac{I_{nc}}{I_{ne}}$. Now defining $\dfrac{I_{nc}}{I_E} = \alpha$, we obtain

$$I_C = \alpha\, I_E + I_{co} \qquad (3.2.5)$$

Thus $I_C = \alpha\,(I_C + I_B) + I_{co}$ since $I_E = I_C + I_B$

Therefore $(1 - \alpha)\, I_C = \alpha\, I_B + I_{co}$

$$\text{or } I_C = \frac{\alpha}{1-\alpha}\, I_B + \left(\frac{I_{co}}{1-\alpha}\right)$$

The quantity $\frac{\alpha}{1-\alpha}$ is defined as β

Hence $I_C = \beta I_B + (1+\beta) I_{co}$ (3.2.6)

We have defined two parameters α and β which are nothing but ratios of currents flowing through the transistor. Let us understand their implications in more detail. From eqn. (3.2.5)

$$\alpha = \frac{I_{nc}}{I_E} = \frac{I_C - I_{co}}{I_E}$$

$$\text{or} \quad \alpha = \frac{I_C}{I_E} \text{ since } I_{co} \text{ is very small as compared to } I_C.$$

If the recombination in the base region is made small by proper doping and sufficiently narrow bandwidth, the values of α may range from 0.9 to 0.995. Thus the collector current is always less than the emitter current. Now from eq. (3.2.6)

$$\beta = \frac{I_C - I_{co}}{I_B + I_{co}}$$

$$\text{or} \quad \beta = \frac{I_C}{I_B}, \text{ provided } I_C \gg I_{co} \text{ and } I_B \gg I_{co}.$$

since $\beta = \frac{\alpha}{1-\alpha}$, the range of values of β would be from 9 to 199. We find that β has values always greater than one and α has values always less than one.

The collector is quite often taken as the output terminal and either the base or the emitter as the input terminal to get a voltage gain from the device by way of the 'resistance transfer' action between the reverse and the forward biased junctions.

The reverse biased collector junction is equivalent to a high resistance r_c and the forward biased emitter junction is equivalent to a low resistance r_e. If we, for instance, take the emitter as the input terminal and inject a signal current ΔI_E in addition to the biasing current I_E, we shall get at the collector a signal current $\Delta I_C = \alpha . \Delta I_E$ in addition to I_C. Since α is less than unity, we get an attenuation in the signal current. But the situation is different if we consider the voltage output at collector which is $\alpha r_c \Delta I_E$. The signal voltage at the emitter is $r_e . \Delta I_E$. Since $\alpha \approx 1$ and $r_c \gg r_e$, the signal voltage at the collector is much larger than that at the emitter giving rise to a voltage amplification. The product of the signal voltage and the signal current at the input and the output terminals indicates that the power also at the output is larger than that at the input. Thus the transistor amplifies the power of the signal. A word of caution is necessary here. We shall not get the amplification by the simple connection shown in Fig. 3.23. Proper arrangements, to be discussed later, have to be made to take the signal voltage and power out.

If we feed a signal current ΔI_B at the base terminal in addition to the bias current I_B, we shall get a collector signal current of $\beta.\Delta I_B$. Thus a large current gain is obtained over and above the voltage and power gain obtained in a manner similar to the previous case.

We normally require two input and two output terminals. The transistor has only 3 terminals and therefore we have to make one terminal common between the input and the output. Since collector is the output terminal, we may make the base as the common terminal while feeding the input to the emitter or reverse their roles and make the emitter as the common terminal. We thus get either the common base or the common emitter configuration depending on the terminal we have made common.

Many times we feed the signal at the base and take the output at the emitter terminal by making the collector as the common terminal. This gives rise to the common collector configuration where the current relations are as follows

$$I_C = \alpha I_E + I_{co} \tag{3.2.5}$$

$$\text{or, } I_E - I_B = \alpha I_E + I_{co}$$

$$\text{or, } (1-\alpha).\ I_E = I_B + I_{co}$$

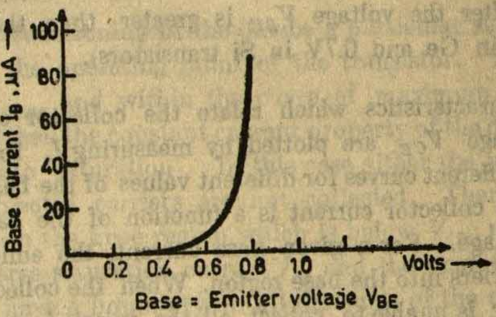
$$\text{Therefore, } I_E = \left(\frac{1}{1-\alpha}\right)(I_B + I_{co}) \tag{3.2.7}$$

Assuming $I_{co} \ll I_B$, we can approximate I_E as

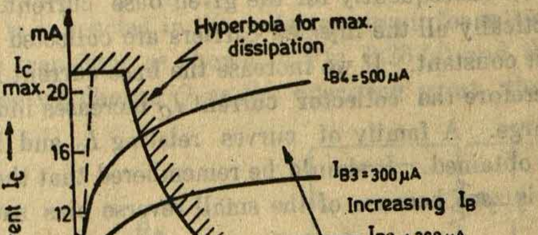
$$I_E = \frac{1}{1-\alpha} \cdot I_B \tag{3.2.8}$$

In this configuration we do not get any voltage gain because both the input and the output are in the forward biased base-emitter junction circuit. But we do get a current gain because $\frac{1}{1-\alpha} \gg 1$. Thus, once again we do get power gain in this configuration also.

The arrow in the emitter lead of the transistor symbol shows the direction of the current flow. Thus the current comes out of the emitter terminal in an *npn* transistor. For the *pnp* transistor the current would enter the emitter terminal. Since we have an access to the input and the output terminals only we can measure the *v-i* characteristics of the device at those terminals experimentally. Typical input and output *v-i* characteristics for a *CE npn* transistor are drawn in Fig. 3.24.

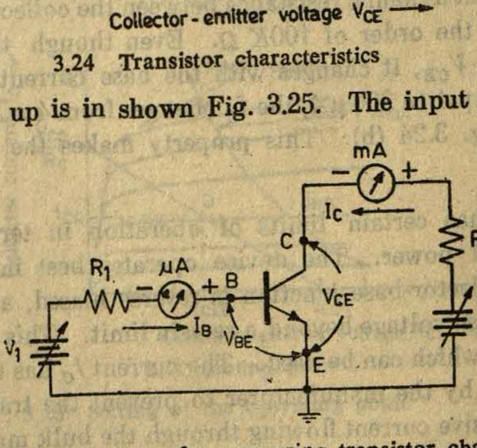


(a) Input characteristics



3.24 Transistor characteristics

The experimental set up is in shown Fig. 3.25. The input characteristics relate



3.25 Experimental set-up for measuring transistor characteristics

the base current I_B and the base-emitter voltage V_{BE} and are measured by applying a variable voltage to the *BE* junction. The *BE* voltage V_{BE} is measured with a high input impedance voltmeter. The measured values of V_{BE} and I_B are plotted in Fig. 3.24 (a). Since the *BE* junction is a forward biased diode, the I_B vs V_{BE} characteristic is basically that of a diode. The current I_B starts flowing practically after the voltage V_{BE} is greater than the threshold voltage (approximately 0.3V in Ge and 0.7V in Si transistors).

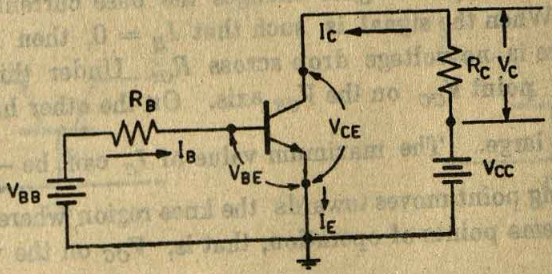
The output characteristics which relate the collector current I_C and the collector-emitter voltage V_{CE} are plotted by measuring I_c for different V_{CE} for a given I_B. We get different curves for different values of the base current as shown in Fig. 3.24 (b). The collector current is a function of the base current and the collector emitter voltage. For a given base current, the emitter injects certain number of charge carriers into the base region. When the collector-emitter voltage is small the collector is unable to collect all the injected carriers. Hence the collector current is small for low V_{CE}. As V_{CE} is increased the collector current rises first and levels off subsequently for the given base current. When the V_{CE} is large enough, practically all the injected carriers are collected by collector and the I_c remains almost constant. If we increase the base current I_B, more carriers are available and therefore the collector current I_C increases independent of V_{CE} as long as V_{CE} is large. A family of curves relating I_C and V_{CE} for different values of I_B are thus obtained. It should be remembered that the I_C is not equal to zero when the I_B is zero because of the small reverse bias saturation current.

We have seen that the current at the collector terminal remains almost constant over a region as the collector voltage varies. This property makes the transistor behave like a current source. The resistance of the current source is defined as the ratio of the change in the collector-emitter voltage ΔV_{CE} to the change in the collector current $\Delta\ I_C$. The ratio $(\Delta\ V_{CE}/\Delta\ I_C) = r_c$ is also known as the equivalent dynamic resistance between the collector and the terminal. The value of r_c is of the order of $100K\ \Omega$. Even though the collector current is independent of the V_{CE}, it changes with the base current I_B. For example, if i_B changes from 100 μA to 200 μA, the I_C changes from 4 *mA* to 8 *mA* approximately as seen in Fig. 3.24 (b). This property makes the transistor a current amplifier.

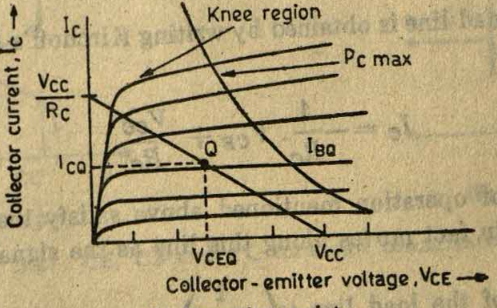
The transistor has certain limits of operation in terms of the terminal voltages, currents and power. The device operates best in a certain specified region. Since the collector-base junction is reverse biased, a break-down occurs if we increase the reverse voltage beyond a certain limit. This sets the limit on the maximum *CE* voltage which can be used. The current I_C has to be below a certain value $I_{C\ max}$ specified by the manufacturer to prevent the transistor from being damaged from a excessive current flowing through the bulk material of the device. The voltage drop V_{CE} across the device and the current I_C flowing through it results in a power of $V_{CE} \cdot I_C$ being consumed in it. The device gets heated in dissipating this power. There is, thus, a limit on the amount of power dissipated by a transistor. We can plot a curve of $P_C = V_{CE} \cdot I_C$ on the output characteristic in Fig. 3.24 (b). This curve is a hyperbola and sets the limit on the combination of voltages and currents to be used.

For the proper functioning of the device a particular set of I_B. I_C and V_{CE} are selected to give the operating point of the transistor. This operating point should be below $I_{C\ max}$ and within the curve of maximum dissipation. If we make V_{CE} very small then the constant current property of the device is lost because the transistor goes into 'saturation'. In this case either the junction gets forward biased or all the injected carriers are not collected. Therefore, the operating point should not be in the knee region which is below V_{CE} min. Below $I_B = 0$ we only get the reverse saturation current I_{co} and the operating point should be above it. Thus we have a boundary on all the sides of the output characteristics and the operating point should be within it. It should be such that the signal excursion does not make the operating point cross the boundaries.

A resistance is connected in the collector circuit for setting the desired value of the V_{CE} of the transistor as shown in Fig. 3.26 (a) and the output is taken across it. Suppose we choose Q as the operating point, the base current I_{BQ} the collector current I_{CEQ} and the collector-emitter voltage V_{CEQ} are the required terminal currents and voltage of the device. The operating point is indicated in Fig. 3.26 (b).



(a) Circuit



b) Operating point

3.26 Setting of the operating point

For a given operating point Q and power supplies V_{CC} and V_{BB}, we are required to calculate the values of R_C and R_B. The resistance R_B determines the base current I_B which in turn controls I_C. R_B can be calculated from the following equation :

$$R_B = \frac{V_{BB} - V_{BE}}{I_{BQ}} \tag{3.2.9}$$

R_C can be calculated as

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} \tag{3.2.10}$$

Usually for circuit applications V_{BE} is assumed to be 0.3 Volts for germanium and 0.7 Volts for silicon transistors. The equations (3.2.9) and (3.2.10) are really not independent because $I_{CQ} = \beta\, I_{BQ}$. Once I_{CQ} is given and the β of the transistor is specified, I_{BQ} and hence R_B can be determined without recourse to the actual characteristics of Fig. 3.26 (b).

The operating point shifts when a signal is applied to the base for the purpose of amplification. The applied signal changes the base current and hence the collector current. When the signal is such that $I_B = 0$, then $I_C \approx 0$ and $V_{CE} = V_{CC}$ because there is no voltage drop across R_C. Under this condition the operating moves to point V_{CC} on the V_{CE} axis. On the other hand, if I_B is very large then I_c is also large. The maximum value of I_C can be $\frac{V_{CC}}{R_C}$ only. For large I_B, the operating point moves towards the knee region where $V_{CE} \approx 0$. The line joining the extreme points of operation, that is, V_{CC} on the voltage axis and $\frac{V_{CC}}{R_C}$ on the current axis, is known as the load line as shown in Fig. 3.26 (b).

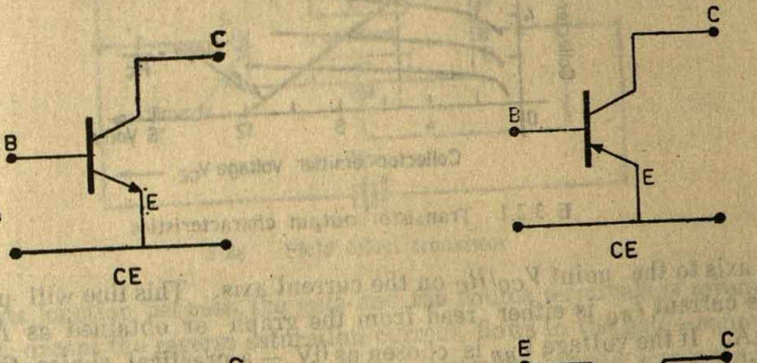
The equation of the load line is obtained by writing Kirchoff's Current Law (KCL) in the CE circuit as

$$I_C = -\frac{1}{R_C} \cdot V_{CE} + \frac{V_{CC}}{R_C} \tag{3.2.11}$$

The extreme points of operation mentioned above satisfy the equation (3.2.11). The operating point in fact moves along this line as the signal changes the base current. The slope of the load line is $\left(-\frac{1}{R_C}.\right)$

The signal output v_C is taken across R_C. To get a large output voltage R_C should be increased because $v_C = I_c \cdot R_C$ and for a large collector current R_C should be made small. It is observed from the Fig. 3.26 that as I_B is increased due to an increase in the signal amplitude, the collector current increases but the collector voltage reduces. This shows that the signal voltage at the collector is 180° out of phase with the input signal.

The input and output characteristics can be drawn for the common base configuration and a similar load line can be drawn to find the active region within the permissible boundaries. Characteristics and load lines can also be drawn for *pnp* transistors in the same way. In the case of *pnp* transistors, the voltages and currents would be of opposite sign to those of *npn* transistor. The *CE*, *CB*, *CC* configurations for both *npn* and *pnp* transistors are shown in Fig. 3.27.



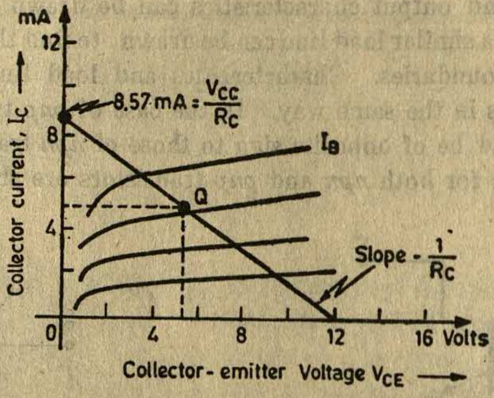
3.27 CE, CB and CC transistor configurations

Example 3.2.1

The silicon transistor in the circuit of Fig. 3.26 (a) has a $\beta = 100$ and $V_{CC} = 12$V. It is desired that the quiescent collector current $I_{CQ} = 5$mA and $V_{CEQ} = 5$ volts. Select suitable values for R_C, V_{BB} and R_B.

Since the voltage drop across the transistor is 5 Volts, the rest of the voltage (12 – 5 = 7 Volts) will drop across R_C. The resistance R_C is therefore 7 Volts/

5mA = 1.4K Ω. We draw a load line of slope —1/1.4K Ω passing through the point Q as shown in Fig. E 3.2.1. We can as well join the V_{CC} point on the voltage axis to the point V_{CC}/R_C on the current axis. This line will pass through Q. The current I_{BQ} is either read from the graph or obtained as $I_{BQ} = I_{CQ}/\beta$ = 50 μA. If the voltage V_{BB} is chosen as 6V — a practical choice, the resistance R_B is given by



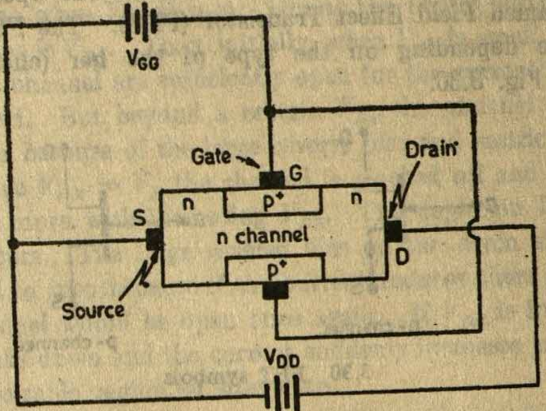
E 3.2.1 Transistor output characteristics

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{6 - 0.7}{50 \times 10^{-6}} = 106 \text{ K } \Omega$$

If $V_{BB} = V_{CC} = 12$V, for a single supply operation then R_B = 226K Ω.

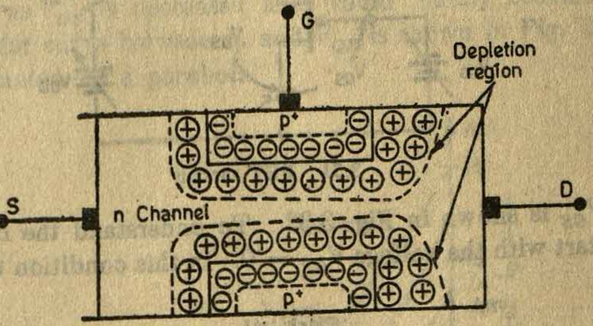
3.2.2 JUNCTION FIELD EFFECT TRANSISTOR

In bipolar junction transistors both the majority and the minority carriers constitute the current flow. In contrast to this the majority carriers only transport the current in the field effect transistors. For this reason it is also known as a unipolar device. Its structure is quite simple. An n-type or a p-type semiconductor bar is taken and contacts are made at the two ends to take out the source and the drain leads as shown in Fig. 3.28. The n-type bar, for example, would have electrons as majority carriers and a current would flow along the bar when a voltage V_{DD} is applied between the drain and the source. The electrons as the majority carriers enter the bar through the source terminal and leave the bar through the drain terminal. If we change the polarity of the battery V_{DD} the magnitude of the current flow will be the same but will be in the opposite direction. The flow of current through the bar can be controlled by constructing pn junctions on the two sides of the bar as shown in Fig. 3.28. The two pn junctions are formed by heavily doping ($p+$) the n type bar with acceptor impurities. Normally the two $p+$ regions are joined together and a common terminal called 'Gate' is brought out. We now apply a voltage V_{GG} between the gate and the source terminals with the polarity as shown in the figure. Let us now see how a controlled flow of current is obtained in this device.



3.28 Field effect transistor

The *pn* junction between the gate and the source terminals is reverse biased. No current, except the reverse saturation current, flows in the gate—source circuit. Further, due to the reverse bias the depletion layers are formed across the junctions and immobile charges are uncovered on both the sides as shown in Fig. 3.29.



3.29 Depletion regions in FET

Without the *pn* junctions the current could flow through the bar across the whole of its cross-section. However, as the junctions are formed the cross-sectional area is reduced. It is further reduced because of the increased depletion regions resulting from the application of the reverse gate voltage. In fact area available for the movement of the free charges is reduced due to the reverse biasing of the gate. This effectively increases the resistance from the drain to the source and the current decreases even when the drain to the source voltage is kept the same. It is clear that the gate voltage would control the width of the depletion layers and thus the drain-source current. The bar can now be thought of having a channel whose width is controlled by the gate voltage. We thus have a

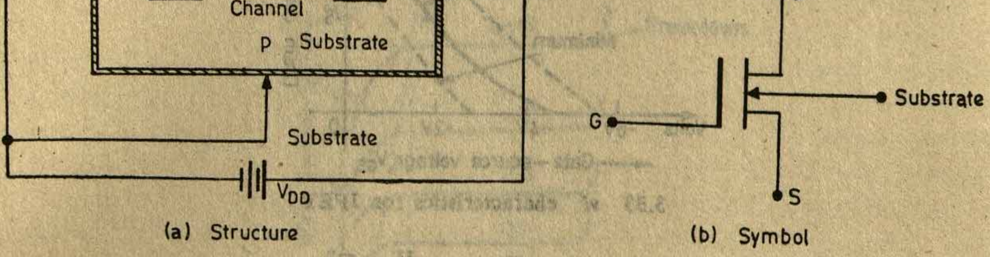
If the gate voltage is made positive with respect to the source the drain current increases because the junction gets forward biased and the depletion layer decreases making the channel wider. However, this is not a desirable region of operation because the gate-source terminals will have low resistance under the forward bias conditions.

When a signal is applied at the gate, the current I_D will change and the drop across R_D would change accordingly. Because of the constant current property of the device we can make R_D large in order that a large voltage is developed across it and an amplification is obtained. Compared to a transistor, the FET has better input characteristics in the sense that the input resistance of the reverse biased *GS* junction is much higher. The corresponding base-emitter junction in the transistor is forward biased and has a low resistance. Just like a transistor the FET also has three configurations of operation viz. common source, common gate and common drain modes.

3.2.3 INSULATED GATE FET (IGFET)

The Insulated Gate Field Effect Transistors (IGFET), also known as Metal Oxide Semiconductor Field Effect Transistors (MOSFET), are finding increasing applications in large scale, integrated circuits. They have two special features viz, (1) low power consumption, and (2) small chip area, which make them very attractive. There are two types of MOSFETs, the depletion mode and the enhancement mode. Each of them of course could have an *n*-channel or a *p*-channel.

The structure of an *n*-channel depletion MOSFET is shown in Fig. 3.34. A lightly doped *p*-type semiconductor is taken as a substrate and two highly doped



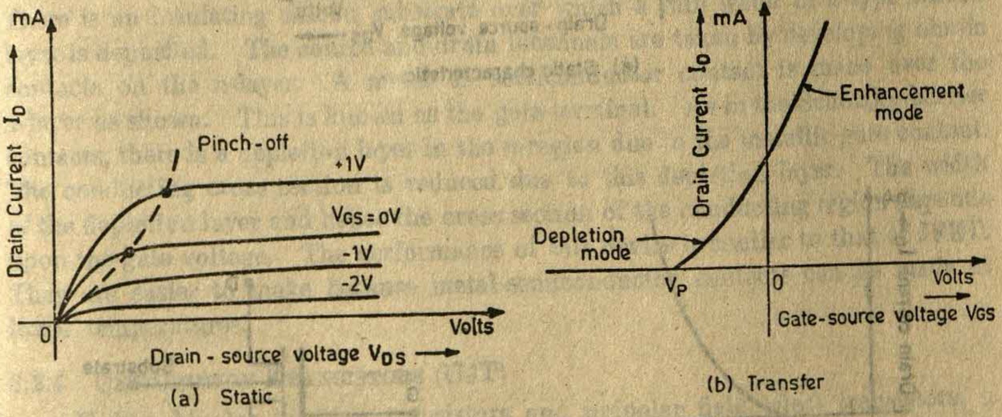
(a) Structure (b) Symbol

3.34 Depletion mode MOSFET

n+ regions are formed which act as source and drain respectively. Between the two *n*+ regions, a shallow *n* region, called channel, is diffused. An insulated layer of Sio_2 is deposited overlapping the $n+$ and n regions except for regions where S and D terminals are taken out. A metallic film is deposited over the n region as shown in the figure and acts as the gate. The gate G here does not form a junction with the source and the drain contrary to the JFET. Because of the sandwiched insulated layer, the device is known as insulated gate FET.

When $V_{GS} = 0$ and the drain is biased positive with respect to the source, a current will flow from D to S trough the n region due to the presence of electrons which are the majority carriers. The p-substrate is connected to the source. A negative potential is applied to the gate with respect to the source. The gate and the n-channel with the in-between insulated layer act as a parallel plate capacitor. A positive charge is induced on the n-channel, when the gate side of the capacitor has a negative potential. This positive charge depletes the channel and reduces its conductivity. Thus the negative potential on the gate controls the conductivity and hence the current flow through the channel from the drain to the source just as in the case of the JFET.

The static and the transfer characteristics of the MOSFET are drawn in Fig. 3.35. We note that the device works well even when V_{GS} is made positive as shown in the characteristics. With a positive voltage on the gate, negative charge is induced in the channel and the conductivity of the channel increases. The current is controlled in the same fashion as before but it is increased instead of being decreased. This is the enhancement mode of operation of the MOSFET. The gate is not made positive in the n-channel JFET in order to avoid forward biasing of the gate-source junction, but there is no such junction here and therefore there is no question of its forward or reverse biasing. In fact the gate terminal has large input resistance under both positive and negative voltages due to the insulated layer. The two types of gate voltages result in two modes of working

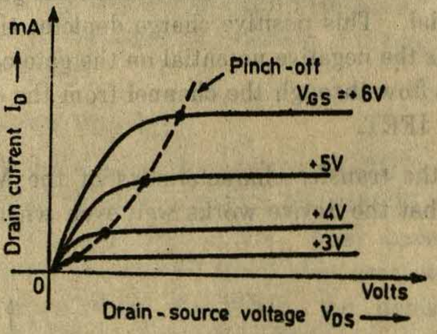


(a) Static

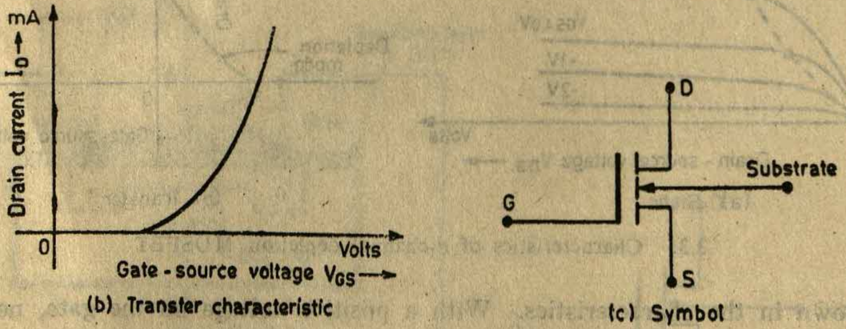
(b) Transfer

3.35 Characteristics of n-channel depletion MOSFET of the MOSFET—the depletion mode with V_{GS} negative and the enhancement mode with V_{GS} positive. One can as well operate the device at $V_{GS}=0$ with the signal having positive and negative swings.

The MOSFET as discussed above is known as depletion MOSFET irrespective of the fact that it may work in the depletion mode or the enhancement mode. There is another variety of MOSFET which is known as enhancement MOSFET where there is no n-channel between the source and the drain. Thus, when $V_{GS} = 0$ no current flows. Only if V_{GS} is made positive, current flows as shown in the characteristics in Fig. 3.36(a) and (b). The n-channel is induced in the substrate when the gate voltage is applied. The symbol for the n-channel enhancement FET is also shown in the Fig. 3.36. Both the depletion and enhancement MOSFETs can be also be p-channel by a proper selection of channel material. The polarity of the battery and the direction of the arrow in the symbol are reversed for the p-channel.



(a) Static characteristic

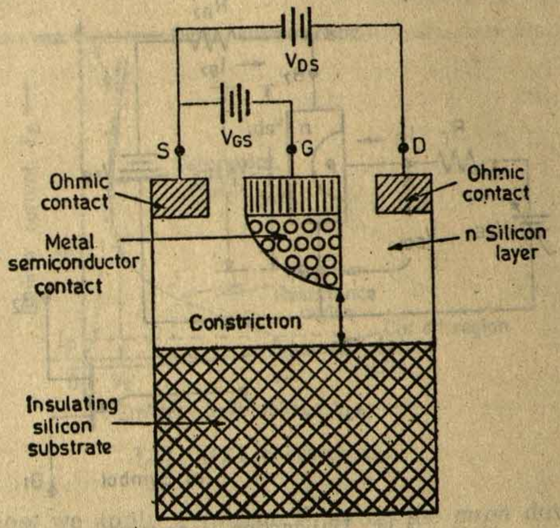


(b) Transfer characteristic

(c) Symbol

3.36 n-channel enhancement MOSFET

MESFET is another type of FET, different from MOSFET. It is actually a metal semiconductor field effect transistor. Its structure is shown in Fig. 3.37.



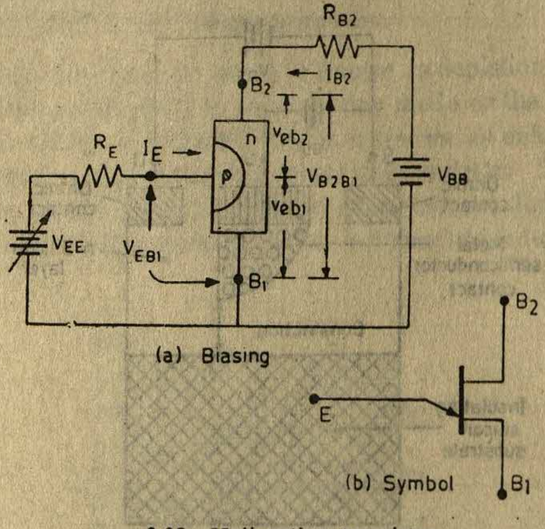
3.37 MESFET

There is an insulating silicon substrate over which a thin wafer of n-type silicon layer is deposited. The source and drain terminals are taken by developing ohmic contacts on the n-layer. A metal to semiconductor contact is made over the n-layer as shown. This is known as the gate terminal. As in the Schottky-barrier contacts, there is a depletion layer in the n-region due to the metallic gate contact. The conducting cross section is reduced due to this depletion layer. The width of the depletion layer and hence the cross section of the conducting region depends upon the gate voltage. The performance of this device is similar to that of JFET. They are easier to make because metal-semiconductor contacts can be made at lower temperatures.

3.2.4 UNIJUNCTION TRANSISTORS (UJT)

Unlike bipolar junction transistors and unipolar field effect transistors, a unijunction transistor has only one pn junction. It is a 3-terminal device with one emitter and two base terminals as shown in Fig. 3.38. A lightly doped n-type silicon bar acts as the base and the p type impurity is added to get a pn junction. The emitter terminal is taken out from the p-region and two base terminals B_1 and B_2 are taken out from the n-region as shown. This device has a negative resistance region and is therefore very useful in oscillator and switching circuits.

The n-type bar acts as a resistance having two parts, one above the E region i.e., towards B_2 and the other below the E-region i.e., towards B_1. The base B_2 is normally kept at a positive potential with respect to the base B_1 which is grounded. A voltage drop V_{B2B1} across the bar creates a field. Due to this field there is voltage drop V_{cb1} across the lower portion of the bar. A positive potential V_{EE} is applied to the emitter with respect to the base B_1. When V_{EB1} is smaller than



(a) Biasing

(b) Symbol

3.38 Unijunction transistor

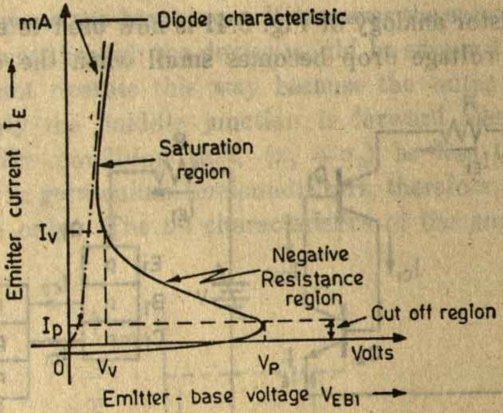
the voltage drop v_{eb1} in the lower portion of the bar, the *E-B* junction is reverse biased and only the saturation current flows in the *EB*1 circuit. When V_{EB1} is larger than v_{eb1} the junction gets forward biased and I_E flows. Due to this forward bias, holes are injected into the *n*-region and are collected by the base B_1. Therefore, the conductivity of the lower position of the bar increases i.e., its resistance decreases. This causes V_{EB1} to decrease when I_E increases. Thus, a negative resistance region is obtained as shown in Fig. 3.39 where I_E versus V_{EB1} are plotted.

At large emitter current I_E, the input characteristic approaches the *pn* diode characteristic asymptotically, shown dotted in the figure. The resistance changes from a negative to a positive one at the point $(V_v' I_v)$. Beyond I_v the resistance is positive. The cut-off ; the saturation and the negative resistance regions are marked in Fig. 3.39. The firing voltage V_p is linearly dependent on the voltage V_{BB} and is quite stable. UJT has important applications in sawtooth generator and multiviflrator circuits.

3.3 Four layer Devices

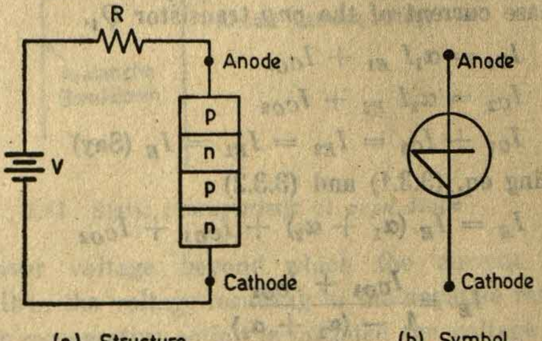
We have described so far diodes which are two layer or single junction devices and transistors which are three layer or two junction devices. We shall now discuss four layer *pnpn* devices which have three junctions as shown in Fig. 3.40. If we take 2 terminals out we get a *pnpn* diode. However, if we take 3 terminals out we get a silicon controlled rectifier (SCR), also known as thyristor ; with 4 terminals taken out we get the silicon controlled switch (SCS).

The operation of the four layer device can be easily understood by representing it in terms of two inter-connected *pnp* and *npn* transistors as shown



3.39 UTI characteristic

in Fig, 3,41. Suppose we apply a voltage V across the *pnpn* device, then we can easily see from Fig. 3.40 that the top and the bottom *np* junctions are forward biased but the middle *np* junction is reverse biased. Because of the presence of the reverse biased junction in series no current flows through the device. The only current permitted is the reverse saturation current of the reverse biased diode. This is the situation when V is small ; but if V is large then at some voltage $V = V_{BO}$ known as break over or firing voltage, the reverse biased *np* junction breaks down and the current rises abruptly. The voltage across the device drops to a very low value after the firing, because of the voltage drop across the resistance R due to the large current. Since the break down has occured the device is able to sustain large current even at the small voltage across it. Thus, the device has, two well defined states. There is an 'off' state when $V < V_{BO}$ and the current is



(a) Structure (b) Symbol

Fig. 3.40 Four layer device

low. There is an 'on' state when $V > V_{BO}$, the device is fired, and the current is large though the voltage drop is small. It can be brought back to the 'off' state only by removing the voltage V.

The two-transistor analogy of Fig. 3.41 is now used to explain the switching action wherein the voltage drop becomes small when the device fires and the current increases. The collector current of the *pnp* transistor Q_1 provides the base current to the *npn* transistor Q_2 and the collector current of the *npn* transistor Q_2 provides the base current of the *pnp* transistor Q_1.

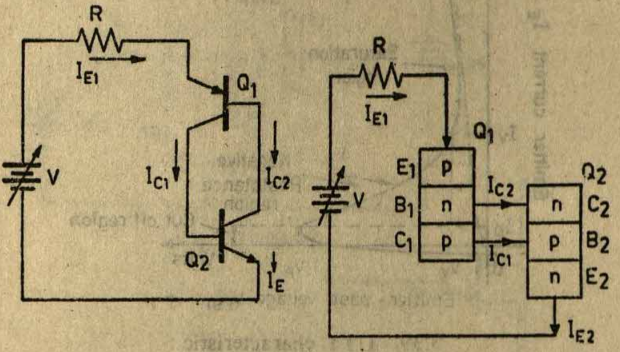


Fig. 3.41 Two transistor equivalence of 4-layer diode

We know that $I_{C1} = \alpha_1 I_{E1} + I_{CO1}$ (3.3.1)

and $I_{C2} = \alpha_2 I_{E2} + I_{CO2}$ (3.3.2)

Also $I_{C1} + I_{C2} = I_{E2} = I_{E1} = I_E$ (Say)

Therefore, combining eq. (3.3.1) and (3.3.2)

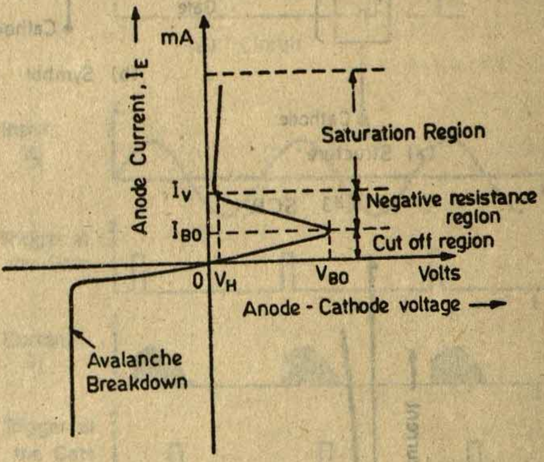
$$I_E = I_E(\alpha_1 + \alpha_2) + I_{CO1} + I_{CO2}$$

or

$$I_E = \frac{I_{CO1} + I_{CO2}}{1 - (\alpha_1 + \alpha_2)} \qquad (3.3.3)$$

Eq. (3.3.3) is a very important equation and tells us a lot about the device. If $(\alpha_1 + \alpha_2)$ approaches unity then I_E increases tremendously. In fact the device breaks over under this condition. For the current I to be small and the device to be in the off state $(\alpha_1 + \alpha_2)$ has to be very small. In silicon transistors, for small currents it is possible to have $(\alpha_1 + \alpha_2)$ less than one, that is, the individual αs are less than 0.5 when the voltage is small, the current and the αs are small and the equation (3.3.3) above is satisfied. As the voltage is increased, avalanche multiplication takes place and the current becomes larger thereby increasing the αs. When $(\alpha_1 + \alpha_2)$ approaches unity, breakover occurs. As the current increases following regenerative action sets in.

As I_{E1} increases I_{C1} increases. Since I_{C1} is the base current for Q_2, I_{C2} which is the base current of Q_1 increases. Thus the I_{C1} increases still more. Du to thise regenerative action the current increases in an unrestrained fashion driving both the transistors into saturation. In the saturated condition the αs are again small. Thus, $(\alpha_1 + \alpha_2)$ remains limited to one even after the current has increased beyond the breakover. If however the sum $(\alpha_1+\alpha_2)$ is greater than one, then the current through the device would be reversed. If V is reversed then the device does not operate this way because the outer two junctions are reverse biased and only the middle junction is forward biased inhibiting any regenerative action. The condition that, $(\alpha_1 + \alpha_2)$, be less than one at low currents is not feasible in germanium semiconductors, therefore, four layer devices are available in silicon only. The *v-i* characteristics of the *pnpn* diode is shown in Fig. 3.42.

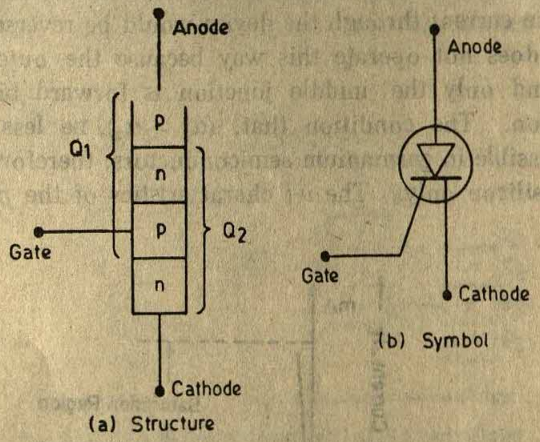


3.42 Static characteristic of *pnpn* diode

V_{BO} is the breakover voltage beyond which the current increases slowly accompanied by a fall in the voltage resulting in the negative resistance region of the device. Once the regenerative action is initiated the voltage drops to V_H and the current then rises rapidly as explained above.

The usefulness of the device increases if the breakover voltage V_{BO} can be varied. A gate terminal at the p-region next to the cathode is taken out for this purpose. The device is known as Silicon Controlled Rectifier (SCR) and is shown in Fig. 3.43. The introduction of a current into the gate terminal is equivalent to increasing the base current of Q_2 of Fig. 3.41. This would increase the collector currents I_{c1} and I_{c2} regeneratively even at lower anode to cathode voltage and the V_{EO} is reduced. The SCR characteristics with the gate current I_{C1} as a parameter are shown in Fig. 3.44.

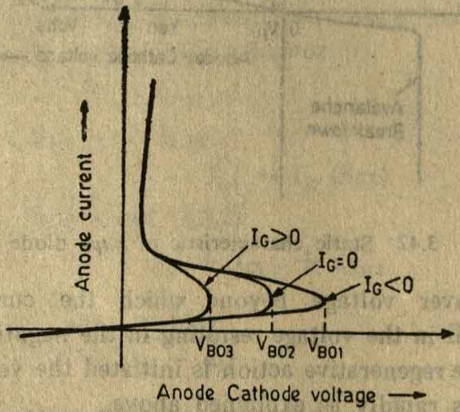
When the second gate terminal is connected to the *n*-region near the anode we get a silicon controlled switch (SCS). In SCS the operation can be controlled by currents through either or both the gates. In SCRs, once the device fires it can only be switched off by reducing the anode to cathode voltage. In SCS, the device can be turned off by applying a negative trigger on either or both the gates. The SCS is a low-power device compared to the SCR.



(a) Structure

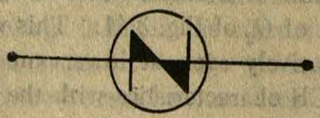
(b) Symbol

3.43 SCR



3.44 SCR characteristics

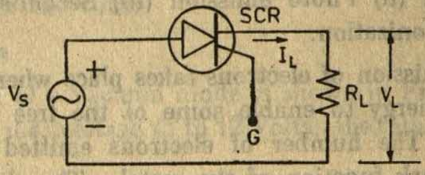
Two *pnpn* diodes connected back-to-back have 'ON' states in both directions. They are called bilateral diode switch and are shown in Fig. 3.45. Light activated SCR (LASCR) is another variation of the SCR where the device is turned on by light impinging on it. We know that when light impinges on a semiconductor,



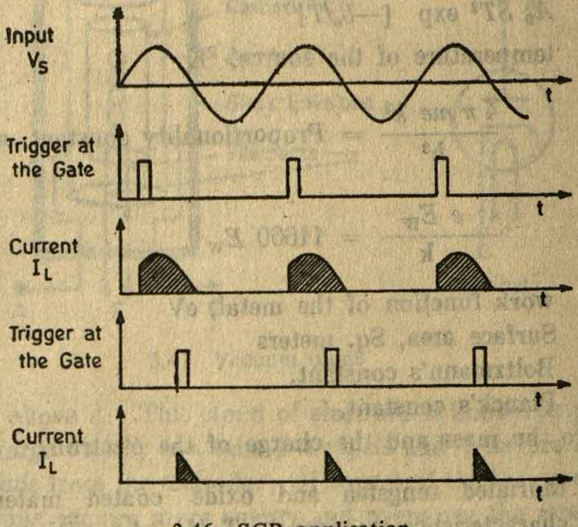
3.45 Bilateral diode switch

electron-hole pairs are generated. These excess carriers make $\alpha_1 + \alpha_2$ approach unity and help the device fire. Once the device fires, even if the light pulses are removed, it remains ON.

A simple application of an SCR in a circuit is shown in Fig. 3.46 (a) and the wave forms in Fig. 3.46 (b). We know that a diode rectifies an ac signal i.e., the current flows through the resistance for half the cycle. With the use of SCR, as in Fig. 3.46, we see that the angle of flow of current can be varied over 0° to 180° by applying the triggering pulses at the gate at various instants of time. Since the current flows for different durations as controlled by the application of the trigger, the average current and hence the average voltage actoss the load are different. Such methods are commonly employed in speed control of motors and in controlling illumination etc. The advantage of using SCRs over the resistance control circuits is that practically no power is lost in the control circuit.



(a) Circuit



3.46 SCR application

3.4 Vacuum Tubes

The vacuum tubes were the first active electronic devices used extensively. Even after the solid state devices mentioned in the earlier sections have been available extensively at low costs, vacuum tubes still find applications in many special circuits. The characteristics of vacuum devices such as the diodes, the triodes, the pentodes and the Cathode Ray tubes are discussed here briefly. All these vacuum tube devices are encapsulated in a glass or metal envelope which is evacuated approximately to 10^{-6} to 10^{-8} mm of Hg. Low pressure is essential in order to ensure that there is no ionization of the gas or air when the electrons move from cathode to anode. Low pressure also helps electron emission from cathode. The cathode and the anode are usually cylinderical in shape. The emission of electrons from the cathode is due to one of the following mechanisms (i) Thermionic emission (ii) Photo emission (iii) Secondary emission (iv) High field emission and (v) Ionization.

The thermionic emission of electrons takes place when the metal is supplied with enough thermal energy to enable some of the free electrons to leave the surface of the metal. The number of electrons emitted is a function of the temperature and the work function of the metal. The electron current is given by Richardson and Dushman as

$$I = A_0 S T^2 \exp\left[-b_0/T\right] \tag{3.4.1}$$

Where T = temperature of the source, °K

$$A_0 = \frac{4\pi m e k^2}{h^3} = \text{Proportionality constant, amp/m}^2\text{/deg}^2$$

$$b_0 = \frac{e E_W}{k} = 11600\, E_W$$

E_W = work function of the metal, eV
S = Surface area, Sq. meters
k = Boltzmann's constant,
h = Planck's constant,

and m and e are the mass and the charge of the electron.

Tungsten, thoriated tungsten and oxide coated materials are used as emitters. Their characteristics are given in Table 3.4.1. We see that the emitters

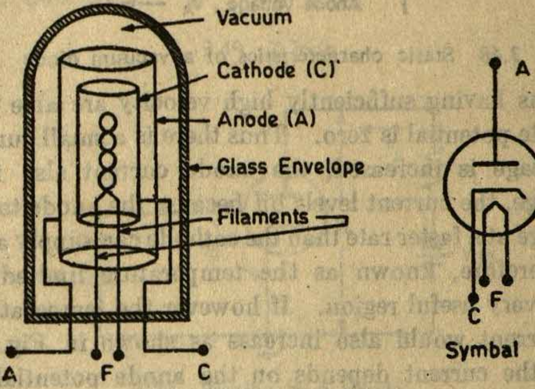
Table 3.4.1 Characteristics of Cathode Materials

Material	A_0	b_0	E_W (eV)	Emission efficiency mA/watt	Operating temp. (°K)
Tungsten	60.2×10^4	52,400	4.52	4-20	2500-2600
Thoriated Tungsten	3×10^4	30,500	2.6	50-100	1900-2000
Oxide coated.	0.01×10^4	11,600	1.0	100-1000	1000 1200

are required to be heated to a temperature ranging from 1000°K to 2600°K depending on the particular material chosen. Heating is usually done by passing an electric current through a filament. Sometimes the filament itself is made to work as an emitter and we have the directly heated cathode. In indirectly heated cathodes the cathode is separate from the heating filament. In addition to the cathode, the anode and the filaments, there are other-electrodes known as grids in the form of wires wound like a coil. These grids are used to control the flow of electrons through the vacuum in the tube.

3.4.1 VACUUM DIODE

The construction of a vacuum diode is shown in Fig. 3.47. As the filament is heated by an a.c. or d.c. voltage (5 to 12 Volts), the cathode emits electrons which form a cloud just above it. This cloud of electrons is known as the space charge. After a certain charge density is attained it repels and therefore stops any further emission of electrons from the cathode. Of course, if the temperature is increased further, the electrons acquire more energy and overcome the repelling field of the space charge resulting in an increased emission. Once again the space charge limits the emission of electrons beyond a certain charge density. Now, if a positive potential is applied to the anode, electrons from the space charge are depleted. More electrons are emitted from the cathode immediately to replenish the space charge. Thus, there is a continuous current flow in the cathode-anode circuit, The static characteristics of the diode is shown in Fig. 3.48.



3.47 Vacuum diode

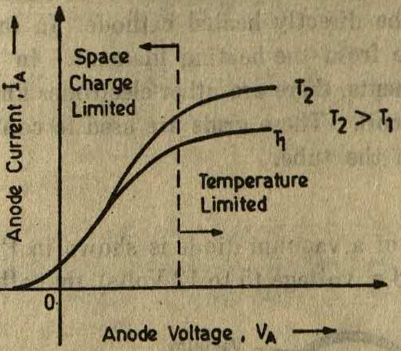
The relationship between anode voltage and the current density is given by Langmuir-Child law as

$$J = \frac{2.34 \times 10^{-6} \times E_b^{3/2}}{d^2} \qquad (3.4.2)$$

where J = anode current density, amp/m²

$V_A = E_b$ = anode potential, volts

d = anode-cathode separation in meters



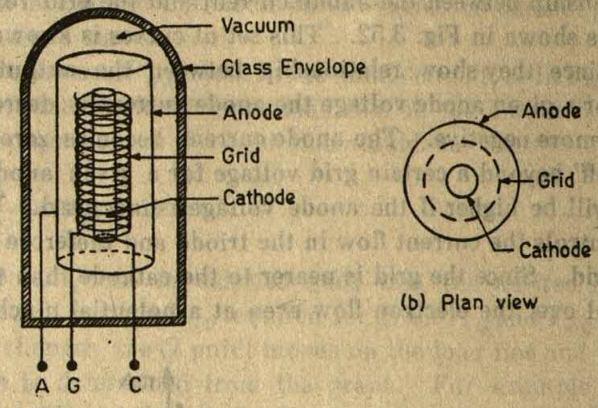
3.48 Static characteristics of a vacuum diode

Some electrons having sufficiently high velocity are able to reach the anode even when the anode potential is zero. Thus there is a small current when $V_A = 0$. As the anode voltage is increased, the anode current also increases. After a certain anode voltage, the current levels off because the anode takes away electrons from thes pace charge at a faster rate than the cathode can supply at that temperature. This region is, therefore, known as the temperature limited operation of the diode and is not a very useful region. If however the temperature of the cathode is increased the current would also increase as shown in Fig. 3.48. The region below this, where the current depends on the anode potential, is known as the space charge limited region.

If the polarity of the anode voltage is reversed then no current flows because the negative anode repels the electrons. Thus, the vacuum diode, like a semiconductor diode, is a unilateral device and is used as such in all applications. The range of operating voltages in vacuum diodes is much higher-of the order of tens of volts. The vacuum diodes are much bigger in size compared to the semiconductor diode and require heating voltage for their operation.

3.4.2 TRIODE

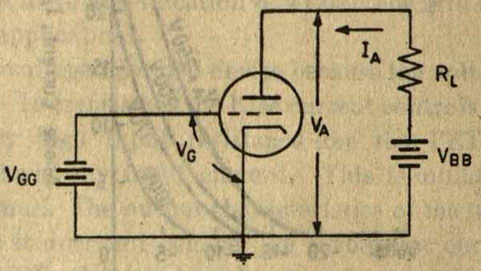
A triode consists of an additional mesh like structure between the anode and the cathode. The structure of the triode is shown in Fig. 3.49. When a positive potential is applied to the anode with respect to the cathode and no potential is applied to the grid, the triode works just like a diode—that is, the space charge is created near the cathode and the electrons flow to the anode due to the positive field. The *v-i* characteristic would be similar to that of the diode. Suppose we now apply a negative voltage on the grid with respect to the cathode as shown in Fig. 3.50. The negative potential on the grid creates a field that repels some of the electrons back to the cathode and a fewer electrons reach the



(a) Structure

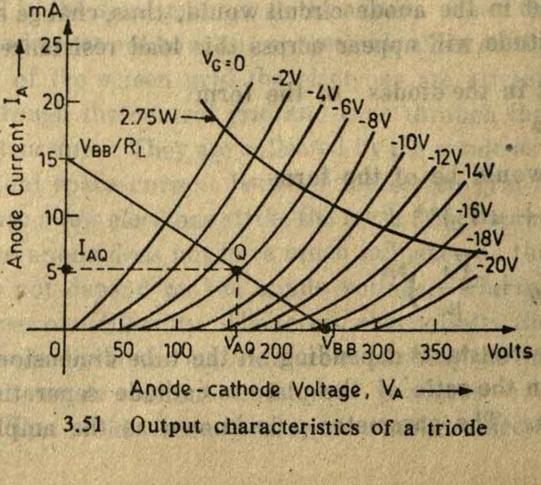
(b) Plan view

3.49 Triode



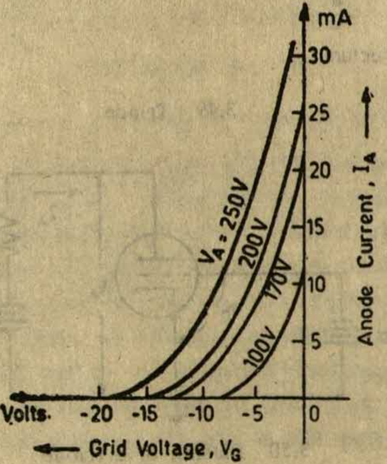
3.50 Biasing of a triode

anode now. The negative grid potential therefore reduces the anode current. We get the family of *v-i* curves for different grid voltages as shown in Fig. 3.51. These are known as the plate or anode or output static characteristics of the triode. Individual curves are the diode curves and are displaced because of the grid potential.



3.51 Output characteristics of a triode

The relationship between the anode current and the grid voltage for various anode voltages is shown in Fig. 3.52. This set of curves is known as the transfer characteristics since they show relationship between the output and the input parameters. For a given anode voltage the anode current is decreased as the grid voltage is made more negative. The anode current becomes zero or the tube is said to be 'cut-off' beyond a certain grid voltage for a given anode voltage. The anode current will be higher if the anode voltage is increased. We see that the grid actually controls the current flow in the triode and theferore it is also known as the control grid. Since the grid is nearer to the cathode than the anode, it has a greater control over the electron flow even at a potential much lower than the anode. A smaller voltage on the grid can control the anode current in the same way as a larger voltage on the anode. When a varying signal voltage is applied to the grid the anode current varies along with it. The voltage drop across a resistance connected in the anode circuit would, thus, change and the same signal with a large amplitude will appear across this load resistance.



3.52 Transfer characteristics of a triode

The anode current in the diodes of the form

$$I_A = k\,V_A^{3/2}\,.$$

For the triode it would be of the form

$$I_A = k\,(V_A + \mu\,V_G)^{3/2}$$

or $$I_A = k_1\left(V_G + \frac{V_A}{\mu}\right)^{3/2} \qquad (3.4.3)$$

where k and k_1 are constants depending on the tube dimensions and μ is a parameter dependent on the ratio of the plate-to-cathode separation to the grid-to-cathode separation. The parameter μ is known as the amplification factor of the tube and is a measure of the effectiveness of grid and plate in producing electric fields at the cathode surface.

With the resistance R_L present in the anode circuit, as in Fig. 3.50, the anode current can be found by drawing the load line on the output characteristic as in Fig. 3.51. The equation of the load line would be

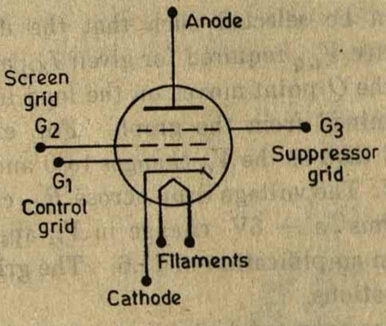
$$I_A = \frac{1}{R_L} (V_{BB} - V_A)$$

The operating point Q can be selected such that the desired I_{AQ} and V_{AQ} are obtained. The grid voltage V_{GQ} required for given I_{AQ} and V_{AQ} is found from the graph. As V_G changes, the Q point moves on the load line and the anode current and voltage can be determined from the graph. For example, if the operating point is at $V_{GQ} -5V$ and then as the V_G changes to 0 and-12V the anode voltages changes to 90V and 225V. The voltage drop across R_L changes to 160V and 25V from the initial 90V. Thus a + 6V change in V_G appears as ± (70V) change across R_L giving rise to an amplification of 11.6. The grid is never allowed to go positive in normal applications.

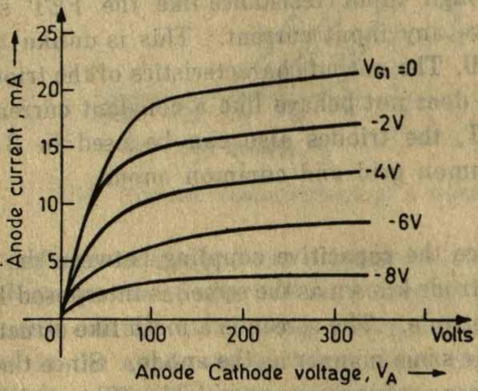
The triode is a voltage operated device because the voltage at the grid terminal controls the output. In transistors the base current controls the output parameters. The triode has a very high input resistance like the FET since both of them practically do not have any input current. This is unlike the transistor whose input resistance is small. The output characteristics of the triode are different from BJT and FET since it does not behave like a constant current source. Just like the BJT and the FET, the triodes also can be used in 3 configurations viz ; common cathode, common grid and common anode.

3.4.3 PENTODE

In order to reduce the capacitive coupling between the grid and the anode electrodes another electrode known as the screen is interposed between them. Such a device is known as tetrode. The screen is a mesh like structure and is kept at a positive potential in the same manner as the anode. Since the screen now shields the anode, the anode does not have any appreciable effect on the field at the cathode. Due to the field of the screen grid the electrons are attracted towards it. The electrons pass through the control grid and even through the screen grid because of its mesh like structure. They are collected by the anode as in the triode. Some division of the toal space current between the screen grid and the anode does takes-place because a few electrons strike the mesh directly and are collected by the screen. Since the anode does not have much influence on the field at the cathode the current does not depend on the anode voltage. The insertion of the screen grid, however poses one difficulty. The screen also collects the secondary electrons emitted by the anode due to the main electrons striking the anode with high energy This reduces the anode current and also produces a negative resistance characteristics. To avoid these problems another electrode, known as the suppressor grid, is interposed between the screen grid and the anode and is normally kept at the cathode potental. The secondary electrons are now returned back to the anode because of its higher voltage with respect to the suppressor grid. It further isolates the control grid and the anode. This device with five electrodes (3 grids, cathode and anode) and filaments is known as the Pentode whose characteristics and symbol are shown in Fig. 3.53. The pentode has output characteristics similar to BJT and FET and acts like a constant current source.



(a) Symbol



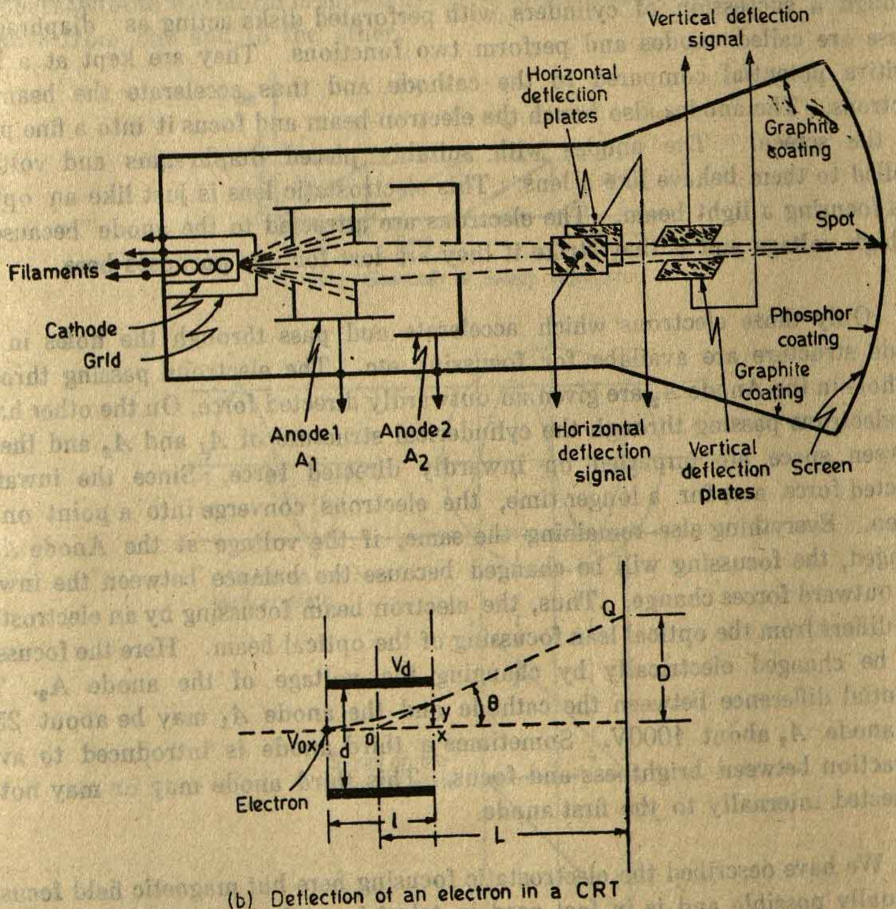
(b) Output characteristics

3.53 Pentode

3.5 Cathode Ray Tube (CRT)

Oscilloscopes occupy a very special place amongst the measuring and indicating instruments of today. The Cathode Ray Tube (CRT) is the heart of the oscilloscope and is used extensively for measurements in the laboratory and the industry. CRT converts electrical signals into visual signals and has therefore major applications as a transducer to project electrical signal visually. Viewing of pictures in television—black and white or colour is possible because of the CRT. It has another major application in the display of Radar Signals. Cathode ray is really another name of an electron ray or beam but the name Cathode ray is still used because of historical reasons.

The CRT has three fundamental functional parts. Firstly it has an electron gun to emit electrons, concentrate them into a beam and focus them on the screen. Secondly it has two sets of deflection plates, horizonal and vertical which deflect the beam and position it anywhere on the screen with the help of connected voltages. Lastly it has an evacuated glass tube with a flourescent screen which makes visible the impact of the invisible electron beam. The location of the electron beam can be seen from the other side as a lighted spot, Fig. 3.54 (a) shows a line diagram of a CRT.



(b) Deflection of an electron in a CRT

3.54 Cathode ray tube and deflection of beam

3.5.1 ELECTRON GUN

The filaments, cathode, grid and the accelerating anodes A_1 and A_2 in Fig 3.54 (a) form the electron gun. The electrons are emitted by a cylinderical

Cathode heated by spiralled filaments. The oxide coating is set down on the front head of the cylinder instead of the sides, as is the common practice in vacuum tubes. The grid is also a cylinder with a small hole facing the oxide coating. This electrode effectively controls the intensity of the electron emission just as in a conventional electron tube. By applying a large negative voltage to the grid in comparison with the cathode, the beam current is reduced and hence the brightness of the spot on the screen. The control voltage on the grid therefore provides a method of controlling or modulating the intensity of the beam and is referred to as Z-axis modulation.

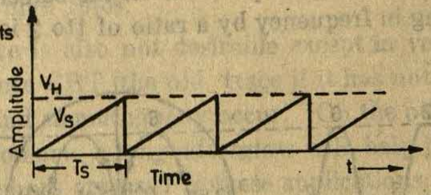
Coming out of the grid aperture, the diverging beam of electrons passes through a succession of cylinders with perforated disks acting as diaphragms. These are called anodes and perform two functions. They are kept at a high positive potential compared to the cathode and thus accelerate the beam of electrons. The anodes also bunch the electron beam and focus it into a fine point on the screen. The anodes with suitably placed diaphragms and voltages applied to them behave like a lens. This electrostatic lens is just like an optical lens focusing a light beam. The electrons are attracted to the anode because of its high voltage and if they strike it they are lost for our purposes here.

Only those electrons which accelerate and pass through the holes in the anode structure are availabe for focussing etc. The electrons passing through the hole in the Anode A_2 are given an outwardly directed force. On the other hand, the electrons passing through the cylinderical structure of A_1 and A_2 and the in-between space are imparted on inwardly directed force. Since the inwardly directed force acts for a longer time, the electrons converge into a point on the screen. Everything else remaining the same, if the voltage at the Anode A_2 is changed, the focussing will be changed because the balance between the inward and outward forces change. Thus, the electron beam focussing by an electrostatic lens differs from the optical lean focussing of the optical beam. Here the focussing can be changed electrically by changing the voltage of the anode A_2. The potential difference between the cathode and the anode A_1 may be about 250V and anode A_2 about 1000V. Sometimes a third anode is introduced to avoid interaction between brightness and focus. This third anode may or may not be connected internally to the first anode.

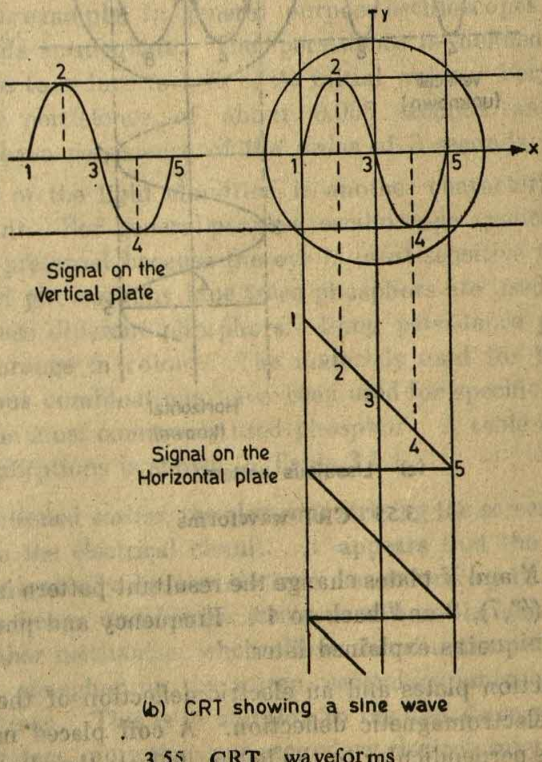
We have described the electrostatic focusing here but magnetic field focusing is equally possible and is in fact used in television tubes. It should also be remembered that electrons emitted by the cathode must finally go back to the anode after hitting the screen in order to close the electrical circuit. If no arrangements exist then the screen will slowly get negatively charged and further operation of the gun will be stopped. How the circuit gets closed and a return path provided is explained later.

3.5.2 Deflection System

There are two sets of deflection plates called the horizontal and the vertical. The horizontal deflection plates consists of two parallel plates placed together vertically. The plates are so positioned that the electron beam passes between them. When a voltage is impressed on the plates, the electron beam deflects along the x direction. Generally, a linearly increasing voltage, increasing with time, is applied to the horizontal or X-plates. The spot on the screen, therefore, will move liniearly with time from left to right if desired. Once the spot reaches the extreme right position it must be brought back to original left position quickly. The voltage waveform looks like a sawtooth and is also called a sawtooth or sweep waveform since it sweeps the electron beam from left to right and back again. An ideal sawtooth waveform is shown in Fig. 3.55(a). The spot will take T_s seconds to move from one end to the other.



(a) Sawtooth or Sweep waveform

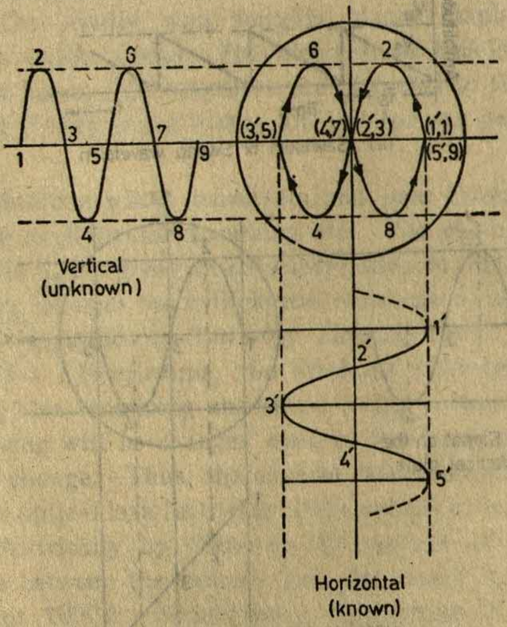


(b) CRT showing a sine wave

3.55 CRT waveforms

Similarly a second set of two plates placed horizontally across the path of the electron beam constitutes the vertical plates. If a voltage is applied to these electrodes the spot moves in the y-direction. These plates are also called the Y-plates of the CRT. By applying suitable voltages to the X and Y plates the spot can be moved to any position on the screen of the CRT.

Let us assume that a sinusoidal signal is applied to the vertical plates and a sweep signal is applied to the horizontal plates. The spot will move linearly with time in the x direction and will simultaneously be deflected by the sinusoidal signal in the y-direction. The resultant trace on the screen will therefore be the sinusoidal signal itself as shown in Fig. 3.55(b). Any waveform, therefore, may be seen on the screen of the CRT by a proper combinaton of the sweep and signal voltages applied. In case the signal applied to the horizontal plates is also a sine wave then we shall see the Lissajous patterns on the screen, Lissajous pattern of two sine waves differeing in frequency by a ratio of 1to 2 is shown in Fig. 3.55(c).



(c) Lissajous pattern

3.55 CRT waveforms

As the signals on the X and Y plates change the resultant pattern is traced as (1,1′), 2, (2′,3), 4, (3′,5) 6, (4′,7), 8 and back to 1′. Frequency and phase can be measured using this technique as explained later.

Instead of deflection plates and an electric deflection of the electron beam, television tubes use electromagnetic deflection. A coil placed near the neck of the tube, with its axis perpendicular to the beam, deflects the electron beam vertically. Larger amount of deflection can be obtained over shorter distances and hence the length of the tube may be small for a particular size of the screen. Magnetic deflection is not used in oscilloscopes because of the frequency limitations of the deflection system.

3.5.3 SCREEN

The screen of the CRT is coated with a thin layer of fluorescent material called phosphor. Various types of phosphors are available and are classified according to their 'colour' and 'persistence'. The persistence is necessary otherwise at high speeds the spot would not have enough time to impress the retina of the eye and no pattern would be perceived. The rapid succession of discrete points on the screen is seen as a continuous trace, thanks to the afterglow of the excited points of the phosphor. It appears as if the spot has a tail and a solid line would thus appear at high rates.

A high persistence is also not desirable except in very special applications. In a very high persistence CRT, the old trace if it has not disappeared will interfere with a new trace and smearing may occur. On the other hand while viewing a rapid transient phenomena a long afterglow will help perceive the waveform. High persistence phosphors are used in these applications. We come to the conclusion, therefore, that different type of phosphors are required for special applications. For example, in general purpose oscilloscopes a persisteaence of about 0.05 seconds is adequate. The persistence is defined as the time taken for the brightness to reduce to 1 % of its initial value. Very short persistence phosphors have a persistence of about 0.005 seconds and long persistence phosphors may have persistence of the order of 3 seconds.

The colour of the light emmitted is another characteristic of a phosphor which is important. For general purpose oscilloscope applications, a greenish-yellow colour is preferred because the eye is most sensitive to this colour. For fast or high speed photography blue trace phosphors are used. Black and white television tubes use different phosphors. Long persistence phosphors are generally yellow or orange in colour. The materials used for the phosphors vary widely and various combinations have been used for specific applications. Zinc orthosilicate is the most commonly used phosphor. A table of various phosphor numbers and applications is shown in Table 3.5.1.

As was mentioned earlier, the electrons striking the screen must have a return path to complete the electrical circuit. It appears that the screen will go on getting charged negatively by the electron beam striking it. This by itself will repel the electron beam and further electrons will not be able to reach it. There is, however, another mechanism whch allows this situation to be rectified. As the electrons hit the phosphor on the screen, secondary emission of electrons takes place from the screen. This is in addition to the fluorsence produced by it in the form of light. In fact, more than one secondary electron may be emitted for every electron in the beam hitting the screen. These secondary electrons are atracted and collected by a graphite coating placed over the interior of the glass envelope and connected to the second anode as shown in Fig. 3.54 (a).

Table 3.5.1 Cathode Ray Screens

Phosphor number	Colour	Persistence	Applications
P — 1	Green	Medium short	General purpose oscilloscopes
P — 2	Blue green	Long	Transients Seeing
P — 3	Greenish yellow	Medium short	General purpose oscilloscopes
P — 4	White	Short	Black — White TV
P — 5	Blue	Very short	Photographic oscilloscopes
P — 6	White	Short	TV
P — 7	Blue white then yellow	Very long	Radar screen
P — 12	Orange	Long	Radar Screen

3.5.4 DEFLECTION SENSITIVITY

An important characteristic of the CRT is the amount of d.c. or peak-to-peak a.c voltage required on the deflection plates to obtain 1 cm of spot deflection. It is called the deflection sensitivity and is expressed in volts/cm. The accelerated electron passes between the deflection plates and is deflected by the voltage applied to it. We shall assume that during the flight of an electron in-between the plates, the voltage on the plates does not change. In other words, the time taken by an electron to move through the plates is very small compared to the time period of the a.c signal applied to the plates and therefore the voltage appears to be constant to that electron. The deflection sensitivity depends upon the accelerating potential, the length and separation of the plates and the length of the tube.

An electron moving in an electric field is accelerated by it. The acceleration 'a' in any direction say x is given as

$$a_x = -\frac{e}{m} \cdot \varepsilon_x \qquad (3.5.1)$$

where e = charge of the electron

m = mass of the electron

ε_x = Electric fields intensity in the x direction.

The velocity v acquired by an electron, starting with zero initial velocity, is given as

$$v = \sqrt{\frac{2V_a.e}{m}} \tag{3.5.2}$$

where V_a = accelerating potential.

Let us now assume that an electron having a velocity v_{ox} enters a set of parallel plates of length l and distance of separation d as shown in Fig. 3.54(b). A voltage V_d is applied to the deflection plates. This will produce an electric field perpendicular to the motion of the electron. The electron will deflect by an amount y as shown. We can calculate y as follows. Since, the acceleration from eq. (3.5.1) is

$$a_y = -\frac{e}{m} . \epsilon_y$$

the velocity v_y is

$$v_y = -\frac{e}{m} . \epsilon_y . t \tag{3.5.3}$$

31

and displacement y is

$$y = -\frac{e}{m} . \epsilon_y \frac{t^2}{2} \tag{3.5.4}$$

The initial position is assumed to be at the origin. Now $t = \frac{x}{v_{ox}}$ therefore

$$y = -\left(\frac{e}{m}\right) \left(\frac{x^2}{2\, v_{ox}^2}\right) . \epsilon_y \tag{3.5.5}$$

which shows that the path is a parabola. The slope of the parabola at $x = l$ will be

$$\frac{dy}{dx} = -\frac{e}{m} . \frac{y}{v_{ox}^2} . l = \tan\theta \tag{3.5.5}$$

This also is the slope of the line OQ which is a tangent to the parabola at $x = l$. The point 'O' and the distance OX in Fig. 3.54(b) is therefore,

$$OX = \frac{y}{\tan\theta}$$

From eq. (3.5.6) and (3.5.5)

$$OX = \frac{l}{2} \tag{3.5.7}$$

Hence the point '*O*' is at the centre of the deflecting plates. The deflection D is thus

$$D = L.\tan\theta$$

$$\text{or}\quad D = L\left(\frac{e}{m}\right).\ \frac{\epsilon_y}{(v_{ox}^2)}\ .\ l$$

Substituting for $v_{ox} = v_x$
From eq. (3.5.2), we obtain

$$D = \frac{L.\,l}{2V_a}\ .\ \epsilon_y \qquad (3.5.8.)$$

The electric field intensity ϵ_y can be written simply as

$$\epsilon_y = \frac{V_d}{d}$$

Hence from eq. (3.5.8), we obtain

$$D = \frac{L.\,l.\,V_d}{2V_a.d} \qquad (3.5.9)$$

The eq. (3.5.9) gives the deflection on the screen produced by a voltage V_d applied to the plates of length l and distance of separation d. The electrons have an accelerating potential of V_a. The deflection sensitivity is expressed as volts/cm and hence

$$\frac{V_d}{D} = \frac{2V_a.d}{L.\,l} \qquad (3.5.10)$$

Eq. (3.5.10) gives the voltage V_d required to produce a deflection of D cm, where d, L, l are expressed in cms. Thus S_d the sensitivity for one cm deflection is

$$S_d = 2V_a\left(\frac{d}{l}\right)\ \frac{1}{L}\ \text{volts/cm} \qquad (3.5.11$$

Sensitivity values of 25 volts/cm are quite common. Sometimes sensitivity is also expressed as cm/volt. Either way, a higher accelerating potential will mean that a larger deflecting voltage will be necessary for the same deflection D as seen in eq. (3.5.10). To keep S_d low, 'd' may be decreased and 'l' increased. However with d small the electron beam will hit the plates for larger deflection as shown in Fig. 3.54(b). Similarly, the time the electron spends in-between the plates increases if l is increased and the assumption that V_d is constant is no more valid. The values of L, l, d, D and V_d are thus a matter of compromise in a particular CRT.

3.5.5. OSCILLOSCOPE

Oscilloscope is an extremely versatile and useful measuring equipment. It can measure frequency, time, phase, voltage, current etc and display waveforms for detailed analysis. Lissajous pattern demonstrated in Fig. 3.55(b) can be used to measure frequency. Here the unknown frequency is connected to the Y-plates and a known frequency is connected to the X-plates. By observing the pattern we can find the unknown frequency f_s as

f_s = unknown signal frequency on the Y plates

$$f_s = \frac{T_H}{T_V} \cdot f_x \tag{3.5.12}$$

Where T_H = the number of loops which touch the horizontal tangent line

T_V = the number of loops which touch the vertical tangent line

f_x = known frequency on the X plates.

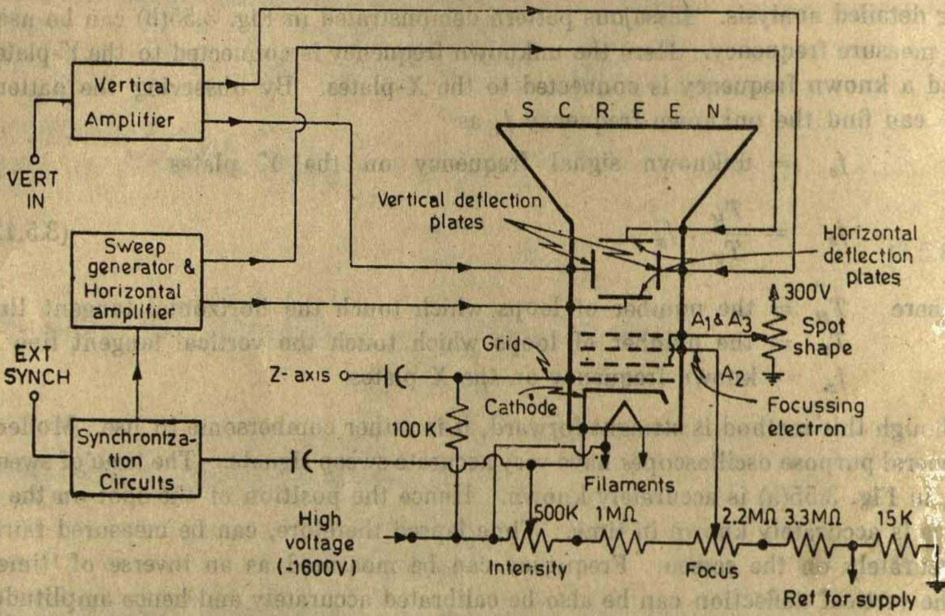
Though this method is straight forward, it is rather combersome to use. Modern general purpose oscilloscopes have very accurate sweep signals. The time of sweep T_s in Fig. 3.55(a) is accurately known. Hence the position of the spot on the x axis is accurately known in time. Time lapsed therefore, can be measured fairly accurately on the screen. Frequency can be measured as an inverse of 'time'. The vertical deflection can be also be calibrated accurately and hence amplitudes of signals can also be measured. Lissanjous pattern can also be used to measure phase.

The deflection sensitivity of the scope is so poor that the input signals have to be amplified considerably before they can be applied to the deflection plates. Block diagram of an oscilloscope is shown in Fig. 3.56. The horizontal and vertical amplifiers thus increase the level of the signals applied to the plates. It has the cathode connected to—1600 V supply and the anodes 1 and 3 are at a positive potential of say+150 V. The voltage at anode A_2, is the 'focus' control and can be varied over -120 V to -850 V. The anode voltage with respect to cathode is between 350 V to 750 V. The graphite coating inside the envelope is kept at the ground potential. Synchronization circuits are essential in order to adjust the sweep frequency to be an integral multiple or submultiple of the input signal. Then only the waveform displayed on the screen will be stationary.

There are many more features in modern oscilloscopes to make them more accurate and easy to operate. Digital oscilloscopes have even a "memory" where the signal is stored and can be viewed at will.

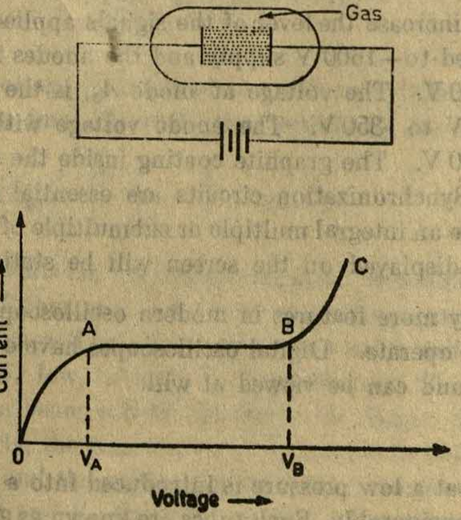
3.6 Gas Tubes

If an inert gas at a low pressure is introduced into a vacuum diode, its characteristic changes considerably. Such tubes are known as gas tubes and have many engineering applications in rectifiers, power control and voltage regulation. Mercury vapour, Helium, Neon, Argon, Krypton and Xenon are the inert gases used in these gas tubes. The gas tubes are basically of two types—hot cathode and cold cathode—depending on whether the cathode is heated or not.



3.56 Block diagram of a osilloscope

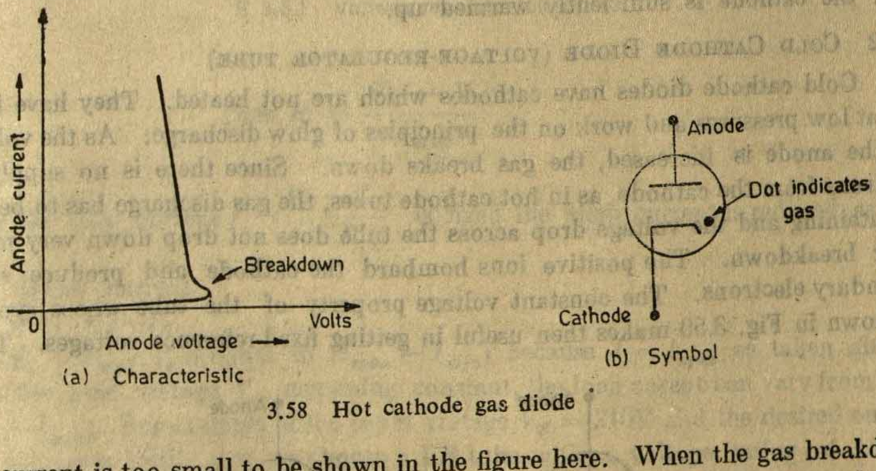
When a voltage is applied across two electrodes kept some distance apar in a gas, a volt-ampere characteristic shown in Fig. 3.57 is obtained. Due to th



3.57 v-i characteristic of a gaseous discharge presence of cosmic rays and radiation from radioactive substances, a few ions are always present in the gas. When a voltage is applied across the electrodes, the positive ions are attracted to the negative electrode and the negative ions or the electrons to the positive electrode. This gives rise to a current which increases with the increase in the voltage, as shown by the OA region of Fig. 3.57. The current levels off beyond a certain voltage when the positive ions are drawn to the electrodes as fast as they are generated by the ionization process. When the voltage is increased beyond V_B, the electrons acquire sufficient energy and collide with the gas molecules. The gas molecules are excited and get ionized liberating more electrons. Resultant positive ions and the electrons give rise to an increase in the current—the region BC in the figure. This region is known as the Townsend discharge region. When the voltage is sufficiently high to result in a self-maintaining gas discharge, the gas is said to be in 'breakdown'. When the discharge produces a soft luminousity in the gas, has low current density and has a voltage drop of the order of the minimum breakdown voltage of the gas it is said to be a glow discharge. The neon signs and voltage-regulator tubes are examples of glow discharge.

3.6.1 Hot Cathode Gas Diode

Hot cathode gas diodes have oxide-coated cathodes which are heated by filaments. An inert gas is introduced in the tube. The voltage current characteristic of the tube is shown in Fig. 3.58. Until the breakdown voltage is reached,



(a) Characteristic

(b) Symbol

3.58 Hot cathode gas diode

the current is too small to be shown in the figure here. When the gas breakdown occurs the increase in curent is unlimitted. An external resistance only can limit the current. At this current the voltage across the tube drops to the ionization potential of the gas used. The ionization energies of various gases is given in Table 3.6.1. The voltage drop across the tube is of the order of 10 to 20 volts and is practically constant over a large range of currents. The power loss in such tubes is quite small and therefore they are used in high power rectifiers instead of the vacuum diodes.

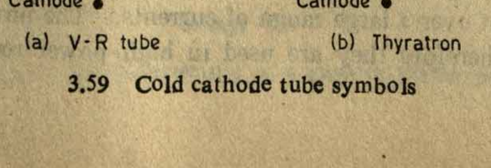
Table 3.6.1 Ionization Energy of Gases

Gas	Ionization energy (eV)	discharge colour
Neon	21.5	Orange
Argon	15.7	Blue
Xenon	12.1	Blue
Mercury	10.4	Blue Green
Sodium	5.1	Yellow

The positive ions which go towards the cathode may damage them by sputtering. Therefore the potential has to be kept sufficiently low (below 24 volts) so that their energy is not high enough to cause cathode sputtering. The cathode should be allowed to reach the desired temperature before the anode voltage is applied. At low temperatures, there will not be enough electrons and full ionization of the gas may not take place. Under such conditions, the tube drop would be higher. If the anode voltage is applied now, the positive ion bombardment may destroy the cathode. Therefore, the anode potential should be applied only after the cathode is sufficiently warmed up.

3.6.2 COLD CATHODE DIODE (VOLTAGE-REGULATOR TUBE)

Cold cathode diodes have cathodes which are not heated. They have inert gas at low pressures and work on the principles of glow discharge. As the voltage on the anode is increased, the gas breaks down. Since there is no supply of electrons from the cathode, as in hot cathode tubes, the gas discharge has to be self maintaining and the voltage drop across the tube does not drop down very much after breakdown. The positive ions bombard the cathode and produce some secondary electrons. The constant voltage property of the tube whose symbol is shown in Fig. 3.59 makes then useful in getting fixed reference voltages. They



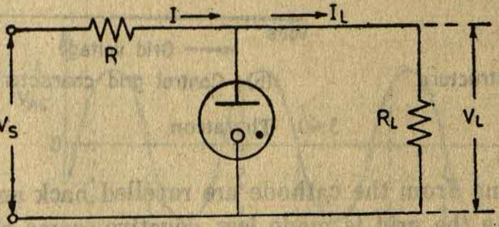
(a) V-R tube (b) Thyratron

3.59 Cold cathode tube symbols

are therefore known as voltage regulator tubes. The voltage drop is of the order of 75 volts. They are used to regulate voltage in the same manner as Zener diodes. Such cold cathode tubes are also used as pilot lamps and other indicating and night lamps.

Example 3.6.1

A cold cathode gas tube is capable of maintaining a discharge where the voltage across the diode remains constant while current varies over considerable limits. It is also used as a reference voltage. The circuit diagram in Fig. E. 3.6.1 shows the arrangement of a cold cathode gas diode used for voltage stabilisation and reference. Tube characteristics are normally such that the current ranges from I_{min} to I_{max}. The diode is used to provide a stable voltage V of 50 V. The resistance R is chosen such that if load resistance R_L is infinite (open circuited) the tube current I_A is limited to I_{max}.



E 3.6.1 Voltage regulator circuit

$$\text{Thus } R = \frac{V_S - V_L}{I_{max}}$$

Since the total current $I = \dfrac{V_S - L_L}{R}$ is fixed the diode current is reduced as the load draws current.

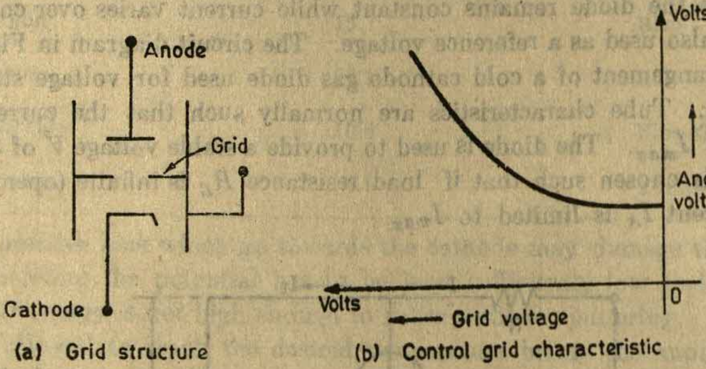
That is $I_L = I - I_A$

when $I_A = I_{min}$, I_L is equal to $(I_{max} - I_{min})$ because $I = I_{max}$ as taken above. Thus the load voltage V_L remaining constant, the load curent can vary from 0 to $(I_{max} - I_{min})$. For example, if the input voltage $V_S = 210\text{V}$ and the desired output load voltage is 150V, then we choose a *VR* tube with a voltage rating of 150 V. These tubes normally have $I_{min} = 5$ mA and $I_{max} = 30$ mA. The value of R would be 2 KΩ. The load current can vary from 0 to 25 mA.

The circuit also gives a stable voltage V_L across a fixed load R_L for an appreciable range of variation of supply voltage v_S. For example if $I_L = 10$ mA, the current I can vary from 15 to 40 mA since I_A varies from 5 to 30 mA. The input voltage v_S may vary from 180 V to 250 V and the output is still maintained at 150 V.

3.6.3 THYRATRON

A thyratron is a hot cathode gas triode whose symbol is shown in Fig. 3.59(b). The presence of the gas in the triode makes it unsuitable as a grid controlled amplifier. Rather, it makes it useful as a grid controlled rectifier like an SCR. Unlike vacuum triodes the grid in the thyratron completely encloses the anode and the cathode as shown in Fig. 3.60(a). When the grid is made very negative, the electrons from the cathode are repelled back and are unable to pass through the grid. As the grid is made less negative, some electrons are able to cross the grid and get accelerated by the positive anode. These electrons collide with the gas molecules and ionize them. The positive ions neutralize the negative field near the grid and thus help even more electrons to pass through it. The process continues and an arc discharge is set between the cathode and the anode. The current through the tube increases sharply and the voltage drop across it is considerably reduced. The thyratron is said to have fired. This firing takes place at a critical grid voltage which is different for different anode voltages. The control grid characteristic is shown in Fig. 3.60(b). Once the tube fires, the grid loses its control because a sheath of positive ions is formed around the grid after the ionization. The tube can be switched off only by removing the anode voltage. Due to this positive sheath around the grid, a grid current flows and has to be limited by an external resistance in the grid circuit. The current in the anode circuit would flow only when the anode is positive with respect to the cathode. Therefore, the thyratron can be used to produce controlled rectification like an SCR. The angle over which the conduction takes place can be changed from 0 to 180° by controlling the angle at which the tube is fired as shown in Fig. 3.61.



(a) Grid structure (b) Control grid characteristic

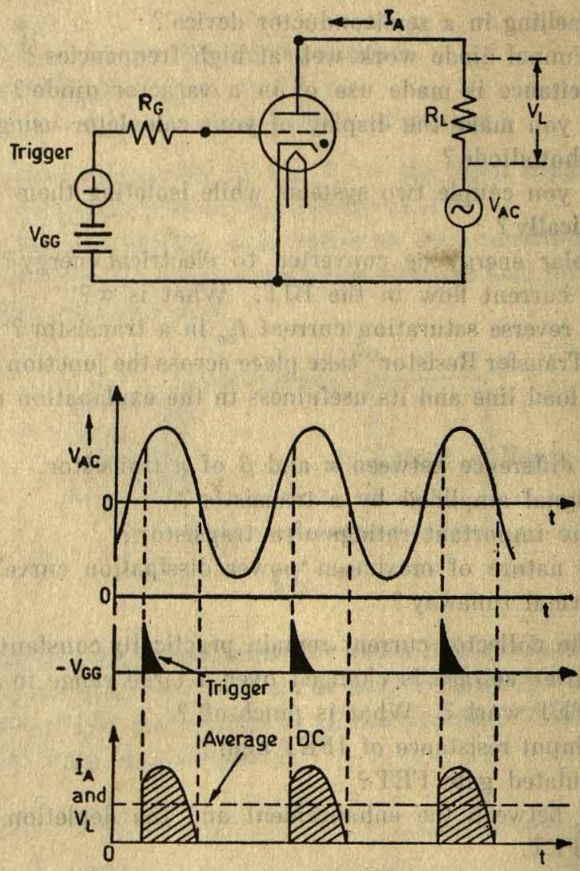
3.60 Thyratron

Review Questions

3.1 What is the unit and value of $\frac{kT}{q}$ at $T = 300°$ K ?

3.2 How does the current vary with voltage in a semiconductor diode ? Illustrate.

3.3 What is the significance of minority carriers in Semiconductor diodes ?



3.61 Controlled rectification using thyratron

3.4 What happens if the reverse voltage across the diode is increased ?

3.5 Enumerate the characteristics of an ideal rectifier diode.

3.6 What is a half wave rectifier ?

3.7 Sketch the current waveform in a practical half-wave rectifier.

3.8 Sketch the waveforms across the diode and the load in a half-wave rectifier.

3.9 How is diode used to charge a battery ?

3.10 How is the voltage waveform across the load modified by connecting a capacitor across it in half-wave rectifier ?

3.11 In a clamper circuit, sketch the waveforms across the diode and the capacitor.

3.12 Describe a limiter.

3.13 How does Schottky diode work ? What is its advantage ?

3.14 Differentiate between Zener and avalanche breakdowns.

3.15 How does Zener diode regulate the voltage ?

3.16 How does the conduction band move when a forward bias is applied across a junction ?

3.17 What is tunnelling in a semiconductor device ?

3.18 Why does Tunnel diode work well at high frequencies ?

3.19 Which capacitance is made use of in a varactor diode ?

3.20 How would you make the display of your calculator using LED ?

3.21 What is a photodiode ?

3.22 How would you couple two systems while isolating them both electrically and mechanically ?

3.23 How can solar energy be converted to electrical energy ?

3.24 Explain the current flow in the BJT. What is α ?

3.25 What is the reverse saturation current I_{co} in a transistor ?

3.26 How does "Transfer Resistor" take place across the junction in a transistor ?

3.27 Explain the load line and its usefulness in the explanation of the operating point.

3.28 Explain the difference between α and β of a transistor.

3.29 How is a signal amplified by a transistor ?

3.30 What are the important ratings of a transistor ?

3.31 What is the nature of maximum 'power dissipation curve'

3.32 What is thermal runaway ?

3.33 Why does the collector current remain practically constant even when the collector-emitter voltage is changed over a large range in a BJT ?

3.34 How does FET work ? What is pinch-off ?

3.35 Why is the input resistance of JFET high ?

3.36 What is insulated gate FET ?

3.37 Differentiate between the enhancement and the depletion modes of working in FET.

3.38 What is Enhancement MOSFET ?

3.39 Explain the working of the UJT.

3.40 How does four layer diode function ?

3.41 How do you achieve controlled rectification using SCR ?

3.42 How are electrons emitted from cathodes ?

3.43 Differentiate between the space charge and the temperature limit of a vacuum diode.

3.44 Why are the pentode characteristics different from the triode ?

3.45 Explain the function of the accelerating potential in a CRT.

3.46 How is frequency of a signal measured using CRO ?

3.47 Where are cold cathode gas tubes used ?

3.48 Why does the grid lose control of operation after firing in a thyratron ?

Problems

P. 3.1 A 6V lead acid battery shown in Fig. E 3.1.1 has to be changed using an a.c. supply of 10 sin 314 *t* volts. The limiting current of the diode is 2A. The r_s is estimated as 0.5 ohms. The required charging current is to be 1 amp.

(i) What should be the PIV of the diode ?

(ii) What must be the value of *R* ?

(ii) How will you know that the battery is charged ?

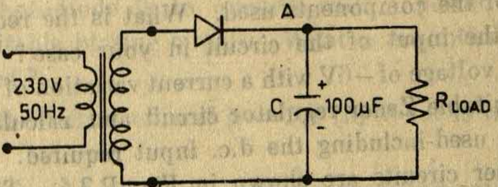
P. 3.2 In the half wave rectifier of Fig. P 3.1, the input supply is 230 V, 50 Hz.

(i) What is the peak value of the voltage at *A* ?

(ii) What is the d.c. voltage at *A* under no load conditions ?

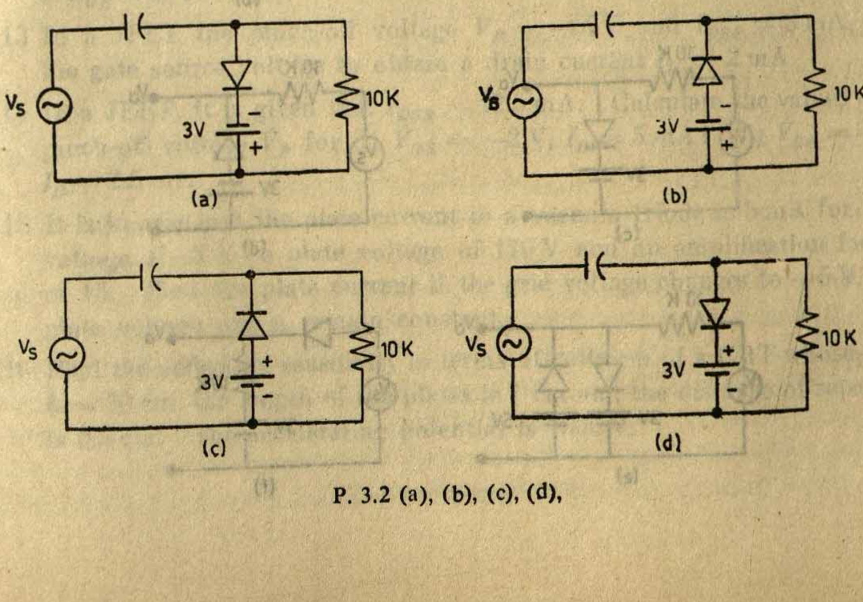
(iii) How much will the capacitor discharge when the load resistor is 1000 ohms.

(iv) Sketch the waveform at *A*.



P. 3.1

P. 3.3 Four circuits using diode, capacitor and a battery are shown in Fig. P 3.2. If the input signal is $v_S = 2 \sin wt$ and the battery voltage is 3 V, then sketch the output wave forms of all the circuits. Which of the combinations will work as a clamper ?

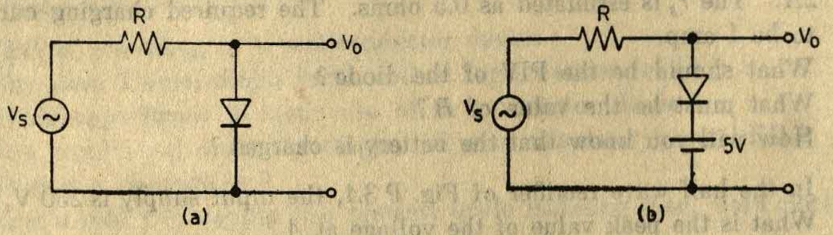


P. 3.2 (a), (b), (c), (d),

P. 3.4 Two limiter circuits are shown in Fig. P 3.3. Given that $v_S = 10 \sin \omega t$

(i) Sketch the output waveform v_o

(ii) Sketch the waveforms if the diodes are reversed.



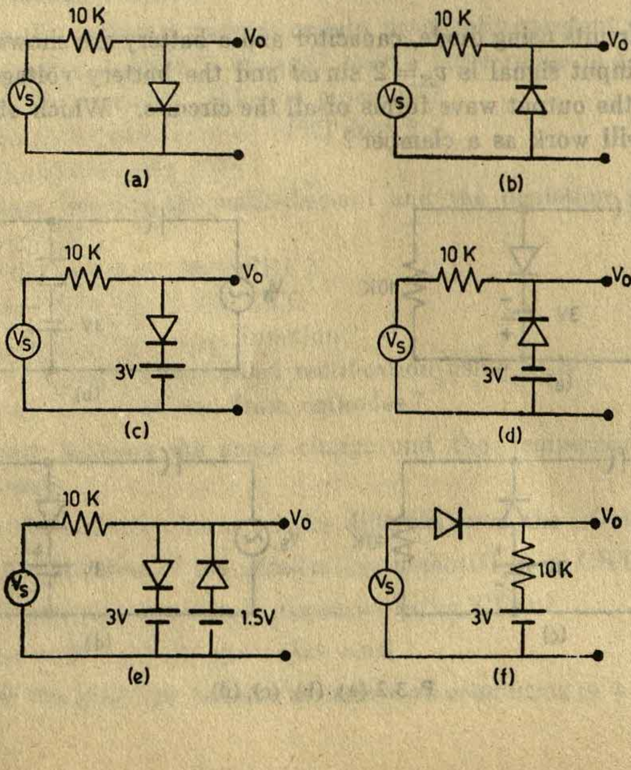
(a) (b)

P. 3.3

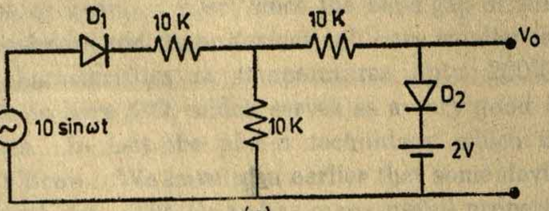
P. 3.5 It is required to obtain a constant voltage of 12 V with a current variation of 0-20 mA. Select a suitable Zener voltage regulator circuit and specify the values of the components used. What is the requirement of the d.c. voltage at the input of the circuit in your case?

P. 3.6 A regulated voltage of -6V with a current variation of 0-10 mA is required. Suggest a suitable Zener regulator circuit and calculate the values of the components used-including the d.c. input required.

P. 3.7 Seven clipper circuits are shown in Fig. P 3.4. The input is $v_S = 5$ Sin ωt. Draw the output waveform in each case



(a) (b) (c) (d) (e) (f)



(g)

P, 3.4

P. 3.8 In an LED, the material used is GaAs P with an $E_g = 1.9$ eV. What will be the wavelength of the emitted light? Give an approximate idea of the current that this LED will draw in the forward direction.

P. 3.9 In a photodiode, what is the order of the reverse current flowing in the diode. A photodiode is to operate with a power supply of + 30 V. Suggest a suitable biasing circuit. What is an optical coupler and where can it be used?

P. 3.10 (i) What is the value of α if $\beta = 200$ (ii) What is the value of β if α is 0.995.

P. 3.11 In a transistor, it is desired to set an operating point of $V_{CE} = 6$ V and $I_C = 2$mA. It is given that $\beta = 80$ and $V_{BB} = V_{CC} = 12\,V$. Calculate the values of R_C and R_B. What is the power dissipation in the transistor? For the same V_{CC} and R_C if the value of R_B is reduced to 2/3 rd its previous value, find the new operating point.

P. 3.12 In a transistor amplifier $V_{CC} = 15$ volts and $\beta = 150$ with $R_C = 5\,\text{K}\Omega$. Draw the load line on the $V_{CE}-I_C$ diagram and find the value of I_C for a $V_{CE} = 5$ V.

P. 3.13 In a JFET the pinch-off voltage $V_P = -4$ V and $I_{DSS} = 8$ mA, Find the gate source voltage to obtain a drain current I_D of 2 mA.

P. 3.14 In a JEET, it is given that $I_{DSS} = 12.5$ mA. Calculate the values of the pinch-off voltage V_P for (i) $V_{GS} = -2$ V, $I_D = 5$ mA; (ii) $V_{GS} = -3$ V, $I_D = 2.5$ mA

P. 3.15 It is known that the plate current in a vacuum triode is 5 mA for a grid voltage of -7 V, a plate voltage of 170 V and an amplification factor μ of 15. Find the plate current if the grid voltage changes to -5 V. The plate voltage and μ remain constant.

T. 3.16 Find the deflection sensitivity in terms of volts/cm of a CRT whose length $L = 30$ cm, the length of the plates is 1 cm and the distance of separation is 0.5 cm. The accelerating potential is 1500 V.

4

Technology of Devices

4.0 Introduction

In this chapter we shall discuss the fabrication of the semiconductor devices. The physical basis and the electrical characteristics of the electronic devices have been discussed in the preceding chapters. In fact the physics of the devices which led to their invention was known much earlier. The invention of the semiconductor devices had to wait the development and advancement of the relevant technology. In the past 3 decades of development of these devices not many new theories have been proposed but new devices with more stable characteristics have been made. The most remarkable progress in the field of electronics has been made in microminiaturization primarily due to the advancement in technology. Thus, it is important for us to discuss and describe the basic technology behind these devices. This will also enable us to appreciate and understand the integrated circuits, large scale integration and very large scale integration (VLSI) of electronic systems. The technology of vacuum tubes has not been discussed here.

4.1 Preparation of semiconductors

We have defined semiconductors as those materials which have covalent bonds and have a stable structure at absolute zero temperature with no electrons in the conduction band. But at room temperature some of the covalent bonds break and electrons in the conduction band and holes in the valence band are available for conduction. The impurities of the semiconductors greatly affect their properties. Thus, it is essential to start with a semiconductor in pure crystalline form and add impurities in a controlled manner to get the desired *n* or *p* type of semiconductor. The semiconductors of interest are *Ge*, *Si* and *GaAs*. Though *Ge* is rarely available in nature, it was quite easy to purify and prepare it in the early days of semiconductor technology. Thus, first few years of the semiconductor device development saw the use of *Ge*. Later, as the technology for purifying silicon improved, it became the desirable semiconductor for most of the devices. Once the difficulties of purifying silicon have been overcome, it has many advantages over *Ge*. Silicon is available plentifully everywhere on the earth in the form of Silica or quartz. Also, since the band gap of silicon is more than germanium, the transistors and other devices will have smaller reverse current and will have better characteristics at temperatures upto 200°C. Further, with silicon it is possible to have SiO_2 which serves as a very good insulating surface in fabricating devices. In fact the planar technology which is very important to-day is based on silicon. We have seen earlier that some devices like SCR can not even be made with *Ge*. The *GaAs* has many useful properties and is finding greater applications in semiconductor devices day by day, particularly at microwaves frequencies. Because of the complex technology involved in *GaAs* devices, we do not discuss them here. We shall confine our attention to *Si* and *Ge* only.

4.1.1 GERMANIUM PREPARATION

Germanium occurs in zinc ores, flue dust and germanite ore. The percentage of germanium in these ores is very small. The germanite ore has many impurities such as copper, iron and zinc. Germanium dioxide is obtained from the germanium ore by chemical treatment. The germanium dioxide is reduced by heating it in a pure graphite boat in presence of pure hydrogen. This results in poly-crystalline ingots of germanium.

Further specialized purification of germanium is essential in order to obtain electronic grade crystals. Single crystals are grown. Purification of germanium is done either by directional crystallization or zone melting. In directional crystallization the germanium is melted and withdrawn from the heated zone slowly. The withdrawn portion starts to solidify gradually. It is known that the impurities try to concentrate in the liquid phase and, thus, as the melted germanium gradually solidifies, the liquid portion collects all the impurities. Finally, towards the end all the impurities are concentrated at one side where germanium has not yet solidified. After solidification, this end containing the impurities is removed. In the zone melting and refining technique, germanium ingot is taken in the form of a bar and is placed in an induction heating coil which would heat and melt the bar over a zone. The bar is pulled through the coil and, thus, some portion of it solidifies earlier than the other. The portion which solidifies later has more impurities as explained earlier. The whole bar is passed through the induction coil five to ten times. The last portion of the bar is cut-off.

Single crystal of germanium is grown by taking a seed crystal, dipping it into the purified molten germanium and pulling it out gradually while rotating it simultaneously. The *n* or *p* type of semiconductor crystal can be obtained by adding appropriate type of impurity to the molten germanium. It is very important to control the rate of crystal growth. Slices and pellets used in making devices are cut from the single crystal ingot by a diamond saw. These slices are lapped and polished to get plane, parallel and smooth surface. They are then etched chemically to remove any contaminants and oxides from the surface.

4.1.2 SILICON PREPARATION

Since molten silicon has high chemical reactivity its purification is rather more difficult. Silicon is obtained from the silicon dioxide which reacts with carbon at high temperatures to result in silicon and carbon monoxide. This commercial grade silicon is purified by chemical processes. It is treated with mixtures of hydrofluoric, sulphuric and hydrochloric acids. Further purification is done by treating it with dry HCL at a temperature of 300°C. The resultant product is trichlorosilane which is purified by distillation. This product is then reduced with hydrogen to give silicon. After chemical purification of silicon described above, it is subjected to metallurgical refining and crystal drawing. Like germanium silicon also is melted in quartz containers in vacuum. The vacuum helps in removing volatile impurities. However, the molten silicon reacts with the quartz container and dissolves some impurities like Boron from the quartz. Repeated melting and pulling refines and gives single crystals of silicon.

Another technique, known as floating zone refining, where no container is used, has been developed for purification of silicon. In this technique, the silicon ingot is fixed between two rod terminals as shown in Fig. 4.1. The whole thing is kept inside a working chamber. A small portion of the ingot is heated and melted by induction heating. When silicon melts the upper rod is pressed to compress the molten zone. The upper and the lower portions are rotated in opposite direction for good agitation and uniform distribution of impurities. The molten zone is moved up and down relative to the induction coil. This technique gives electronic grade of silicon. Slices or pellets are cut from the ingot and are lapped, polished and etched like germanium. Proper type of impurities are added in the melt when single crystals are drawn to give p-type or n-type semiconductors.

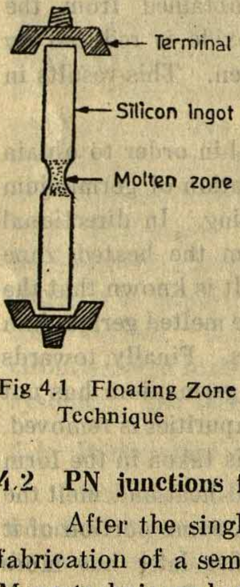


Fig 4.1 Floating Zone Technique

4.2 PN junctions formation

After the single crystals with electronic grade purity have been grown, the fabrication of a semiconductor device primarily consists of making PN junctions. Many techniques have been developed to grow junctions. Each of these techniques is quite elaborate and has some plus points in comparison to the other techniques. The device characteristics depend upon (1) the semiconductor material (2) the doping, that is, addition of external impurities and (3) size, shape and geometry. Therefore, these processes are critical and require a strict control. Junction growing being a metallurgical process requires a precise control of time and temperature. During and after the fabrication of a device various measurements have to be made to ascertain that the desired characteristic have been achieved. All these datails are beyond the scope of this book. We shall only briefly describe a few important techniques of device fabrication.

There are three popular methods of making junction diodes viz. (1) grown junction (2) alloyed junction and (3) diffused junction. The grown-junction diode is made while pulling the crystal from the metal. By adding a particular type of impurity, say Indium, to the melt, we get *p*-type crystal. After a desired length of the *p*-type crystal is obtained we add donor impurity, say Arsenic, to the melt in sufficient quantity to neutralize the acceptor impurity and give *n*-type crystal. After a desired length of the *n*-tpye crystal is grown, it may be cut to give a grown *pn* junction as shown in Fig. 4.2. In fact, the process of adding *p* and *n*-type impurities may be alternated and a large number of junctions grown. They are cut into separate *pn* junctions. Metallic contacts are deposited on them and they are encapsulated after bringing out leads to result in diodes. The grown junction technique was used to make the first junctions but is not used now because the various parameters cannot be controlled here precisely.

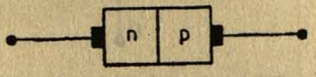
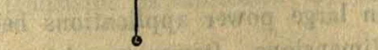


Fig. 4.2 Grown junction

The alloyed junctions are easy to make. An *n*-type silicon wafer (slice) of say 1 cm diameter and 0.4 mm thickness after lapping, polishing and etching is taken. A dot of aluminium of say 0·3 mm thickness is pressed on the wafer and the whole combination is heated to about 580°C. The aluminium would melt into silicon to give an alloy. Silicon re-crystallizes on cooling. The recrystallized silicon volume is *p*-type because aluminium acts as an acceptor impurity. Thus a *pn* junction is formed. In the alloyed junctions, the impurity concentration changes abruptly from *n* to *p*-type, the junction is in fact very narrow. In a grown junction the transition is gradual. Indium is used as acceptor when *n*-type germanium wafer is used. An alloyed junction is shown in Fig. 4.3.



Fabrication of devices by the technique of diffusion has become very popular because precise control can be exercised over various parameters in the manufacturing process. In this technique, a slab of semiconductor doped with a particular type of impurity is heated to a high termperature in the presence of an impurity of opposite type in gaseous form. The atoms of the impurity in the gaseous form migrate into the slab. For example, a *p*-type silicon slab may be exposed to, say, phosphorous in the gaseous form. The heating is done in the presence of an inert gas upto temperatures ranging from about 200°C below the melting point of silicon to the melting point. Phosphorous diffuses into the wafer and neutralizes the acceptor impurities and produces a layer of *n*-type of silicon. Thus a large and uniform *pn* junction can be formed as shown in Fig. 4.4.

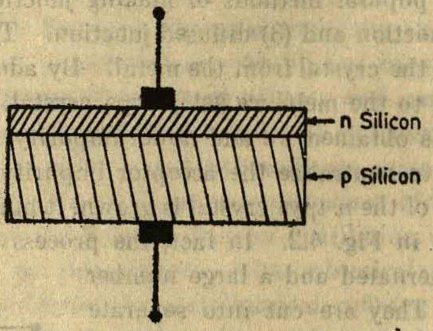


Fig. 4.4 Diffused junction

The impurity concentration is highest at the surface and decreases inwards. Many types of diffusion furnaces are available commercially for the purpose.

4.3 Fabrication of Transistors

A large number of techniques of fabricating transistors are available. We shall, however, confine ourselves to only a few type of transistors such as alloy-junction, grown-junction and diffused-junction transistors. Even though the first transistor made was a point contact transistor it is not used now-a-days. Just as in diodes, the fabrication technique has a great influence on the transistor characteristics and therefore reguires a great deal of detailed understanding of the underlying process. We shall again focus our attention only to the basics of the fabrication process.

We recall that a transistor has a base region through which the minority carriers are required to diffuse to the collector region without recombining in the base region. Recombination cannot be completely prevented but can be kept very small by making the base region (width) very small. All transistors thus are made with very small base widths such as 1 to 100 microns. Other dimensions of the active part of the transistor are also quite small, say about 300 microns. Such small dimensions create some problems. First is the difficulty of handling such a device both during and after manufacture. They have, therefore, to be supported by substrates of larger dimensions. Secondly the heat required to be dissipated in large power applications becomes large and the device has to have larger dimensions. Power transistors have collector junctions which are as large as 5000 microns. Of course, in very large power devices, heat sinks are provided with the collectors to dissipate the excessive heat.

The alloy junction transistor as shown in Fig. 4.5 is made by alloying two Indium pellets on two opposite sides of an n-type germanium wafer. Indium, an acceptor impurity, is dissolved into the germanium giving p-regions on both the sides. We thus get *pnp* structure. Collector, Emitter and Base contacts are

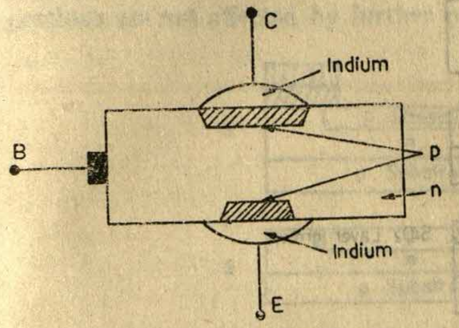


Fig. 4.5 Alloy junction transistor

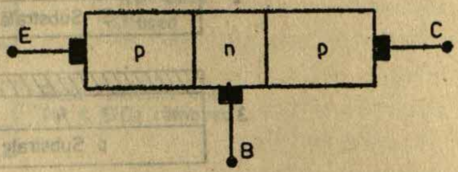


Fig. 4.6 Grown junction transistor

made in the respective regions and terminals brought out to result in a *pnp* transistor.

The grown junction transistor, shown in Fig. 4.6, is fabricated during crystal growing. By adding suitable impurities to the melt two junctions are drawn close by to make a *pnp* or *npn* transistor.

Diffusion technique of making transistors is becoming increasingly popular because it offers precise control on geometry and results in better transistor characteristics and improved performance. Different junctions are grown by the diffusion of impurities into a semiconductor wafer. The diffusion technique has led to the development of a very powerful technique of making not only transistors but even Integrated Circuits. This technique known as Silicon Planar Technology is described in detail in the next section.

4.4 Silicon planar technology

Silicon has become a very popular semiconductor because (i) its temperature range extends upto 200°C due to its larger band gap, (ii) it is available in abundance in nature and (iii) silicon dioxide (SiO_2) is a good insulator and can be used as mask in preparation of devices. SiO_2 can simply be deposited on silicon by heating. The use of mask prevents diffusion of impurities where we do not want them. Thus, wherever diffusion of impurities is required the selected region on the silicon chip is left unexposed. This provides a lot of flexibility and control in device fabrication. Let us see how an *npn* transistor is fabricated by this technology.

A *p*-type silicon wafer is taken to act as a substrate, as shown in Fig. 4.7. A thin layer of *n*-type silicon of required resistivity is epitaxially grown on the *p* silicon substrate. Epitaxial layer is grown by thermal decomposition of silicon bearing compounds such as Silane, Silicon tetrachloride and trichlorosilane. It is possible to provide single crystal layers of uniform resistivity over the semiconductor substrate. The resistivity of the epitaxial layer can be chosen independently of the substrate.

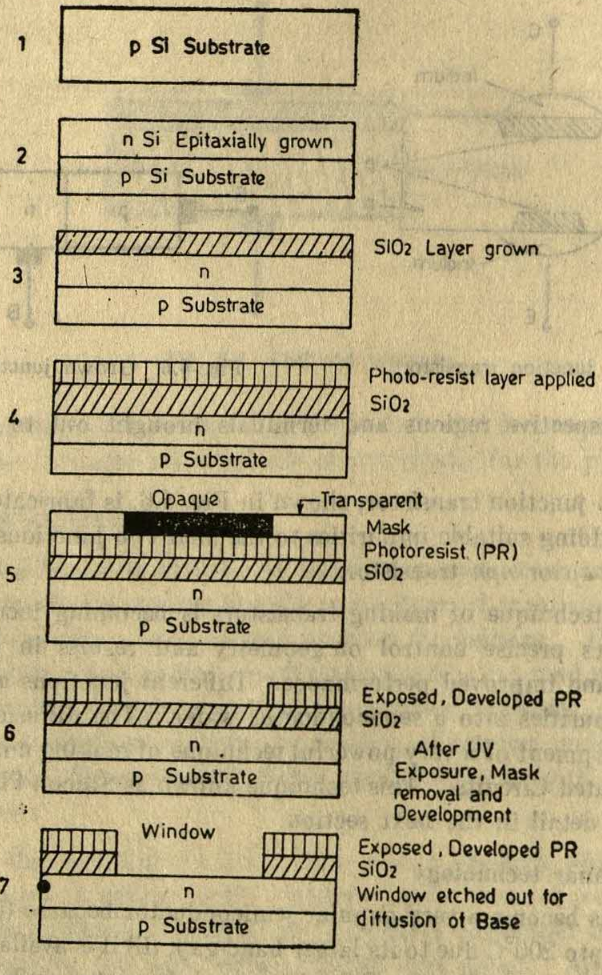


Fig. 4.7 Steps of Silicon Planar Technology for making *NPN* Transistor

A film of photoresist is applied over the silicon dioxide layer formed over the epitaxial layer. The property of this photoresist is that it gets polymerised when exposed to ultraviolet light. Thus a mask is now prepared in which the portions which are not required to be doped are kept transparent and the portions where doping is required are made non-transparent to ultraviolet light. Usually the pattern is drawn on large scale and then reduced by photographic techniques. The mask is then placed over the photoresist and the ultraviolet light is allowed to fall over it. The ultraviolet light polymerises the photoresist wherever there are openings in the mask. The non-transparent portions do not allow the ultraviolet light to pass through and, therefore, the photoresist below these portions are unexposed. After the ultra violet exposure the mask is removed and the photoresist from the unexposed portions is dissolved by developing the wafer like a photographic film. The wafer is then fixed in a solution so that the exposed portions are not affected by further processing. We now have a wafer in some

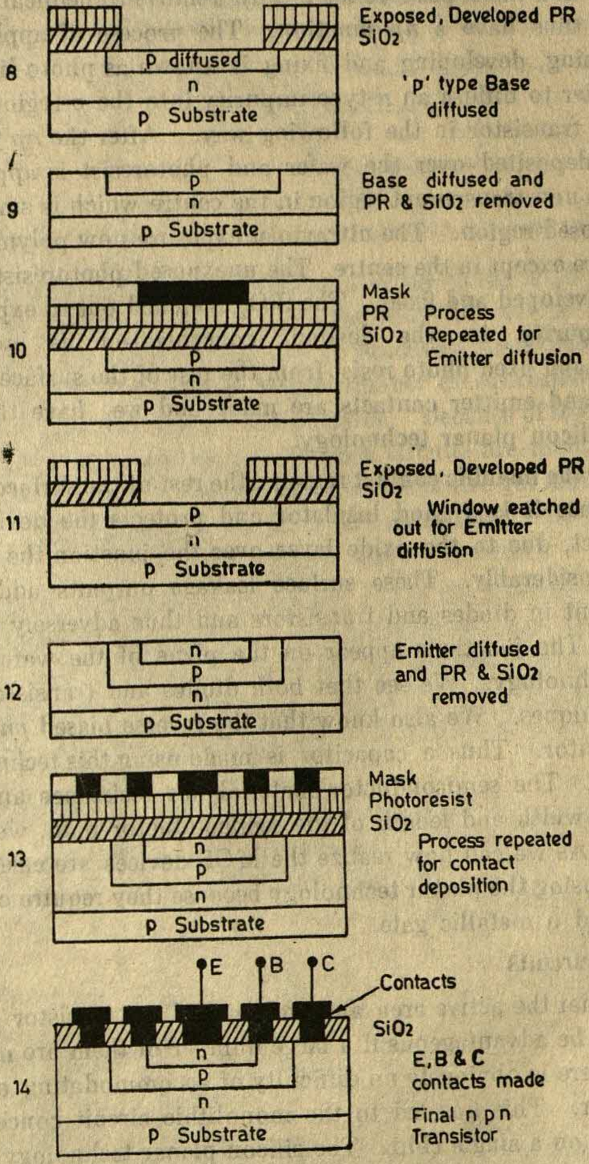


Fig. 4.7 (Continued) Steps of Silicon Planar Technology for making NPN transistor

portions of which the oxide layer is directly available and in the rest of the portion it is covered by the polymerized, developed and fixed photoresist.

By etching the chip in hydrofluoric acid the oxide layer from the unexposed portions is removed. This makes the *n*-type silicon surface available for doping with a *p*-type impurity. By diffusion technique, the *p*-type impurity is now diffused in the selected region. This makes the base region of the transistor. The developed and fixed photoresist is now removed chemically from the other portions. We thus have a *np* junction. The process of applying photoresist, masking, exposing, developing and fixing is known as photo-lithography. It is repeated in order to diffuse an *n*-type impurity into the *p*-region and thus giving rise to the *npn* transistor in the following way. After the *np* junction is ready, SiO_2 is again deposited over the wafer and photoresist is applied. A mask is prepared with a non-transparent region in the centre which is smaller in size than the previous closed region. The ultraviolet exposure now polymerises the photoresist everywhere except in the centre. The unexposed photoresist is dissolved and the wafer is developed and fixed. The SiO_2 is etched out to expose the *p*-region. An *n*-type impurity in the desired concentration is now diffused in. The developed and fixed photo resist from the rest of the surface is removed. The collector, base and emitter contacts are made and we have the *npn* transistor made by the silicon planar technology.

Except for the metallic contact regions, the rest of the surface is again covered with SiO_2 because it is a good insulator and protects the device from external hazards. In fact, due to the oxide layer over the junction the surface currents are reduced considerably. These surface leakage currents add to the reverse saturation current in diodes and transistors and thus adversely affect the device characteristics The junctions appear on the plane of the wafer and hence the name planar technology. We see that both diodes and transistors can be made using these techniques. We also know that the reverse biased *pn* junction can be used as a capacitor. Thus a capacitor is made using this technique by actually making a diode. The semiconductor material has resistance and, therefore, by choosing proper width and length of the semiconductor path, we get resistors of desired values. As we can now realize the MOS devices are easier to make than the BJT devices using the planar technology because they require only a deposition of SiO_2 layer and a metallic gate.

4.5 Integrated circuits

It is clear that the active area and volume of a transistor are really very small. It would be advantageous if a large number of them are made on a single silicon chip. There is obviously no difficulty of accommodating a large number on a single wafer. This has led to the monolithic circuit concept where many circuits are made on a single chip. The silicon planar technology as discussed in the previous section makes this concept a reality. In fact, by proper masking many devices can be made simultaneously. The diodes, capacitance and resistances can also be made by this technique. Thus complex electronic circuits having transistors, diodes, capacitors and resistors are made on a single chip known as the Integrated Circuit. Two transistors are shown in Fig. 4.8 in the same substrate. The active and passive components in the Integrated Circuit are connected within

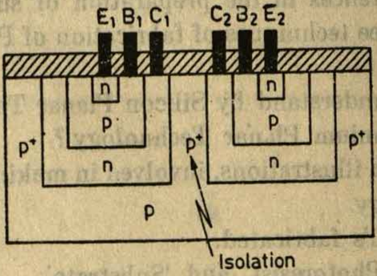


Fig. 4.8 Two transistors on the same substrate with junction type isolation

the chip. A large silicon IC has a dimension of the order of 10 mm whereas the silicon wafer is of dimension 10 cm. So the same IC can be made repeatedly on the same wafer. Also many wafers can be processed simultaneously to produce a large number of IC's and a much larger number of equivalent devices. Since the masks are used again, the process is repeatable. Because of the interconnections inside, the reliability and performance of such circuits are much better than the discrete devices and circuits. The size and the weight also get reduced considerably which is a prime requirement in all fields of applications. In the size of single discrete transistor we now have a complete circuit assembly.

In ICs the collector terminal is brought out at the top because the collector is completely covered by the substrate. An isolation as shown in Fig. 4.8 between the collector and the substrate is provided by reverse biasing the *pn* junction between the substrate and the collector. This technique is also used to provide isolation between devices in the same chip. Dielectric isolation by SiO_2 is also sometimes provided between devices.

By the planar technology both linear and Digital IC's using BJT or MOSFET and passive components such as diffused resistors and capacitors are being made. There are other ICs other than the monolithic silicon ones. They are the thin film and the hybrid ICs. Thin film ICs have an insulating substrate such as glass, ceramic or sapphire over which MOSFETs and thin film resistors and MOS capacitors are fabricated. Hybrid ICs have active devices fabricated on Silicon and the passive components and interconnections are on thin/thick film. Sometimes discrete devices are also connected to hybrid circuits.

The microminiaturization in electronics is progressing with no apparent end. The monolithic ICs had to start with about 3000 components on 1 cm^2 silicon wafer. We now, have, with improvement in technology, large scale Integration (LSI) and very large scale Integration (VLSI). A VLSI chip has more than 100000 components in an area of 1 cm^2.

Review Questions

4.1 What are the advantages of using silicon over germanium in semiconductor devices ?

4.2 What are the differences in the preparation of silicon and germanium ?

4.3 Describe briefly three techniques of fabrication of PN junctions and compare them.

4.4 Explain what you understand by Silicon Planar Technology. Why is there nothing like Germanium Planar Technology ?

4.5 Enlist the steps, with illustrations, involved in making a silicon *npn* transistor by planar technology.

4.6 Explain how are IC's fabricated.

4.7 Explain 'Etching' 'Photoresist' and 'Substrate'.

5

Terminal Characteristics of Electronic Circuits

5.0 Introduction

An electric circuit is an interconnection of various circuit elements such as resistances, capacitances, inductances and transformers and electrical sources such as voltage and current in such a manner that each element or source is in one or more closed paths for the currents to flow. In electronic circuits, electronic devices such as tubes and transistors are all connected as circuit elements. Electric circuits are analysed, that is the voltage across an element and the current through it are found by circuit laws such as the Ohm's law and the Kirchoff's voltage and current laws. Application of these laws to circuits have led to the two standard techniques known as Nodal and Mesh methods for finding voltages and currents in circuits. The same techniques will be applicable to the analysis of electronic circuits also, provided we are able to represent the electronic devices in terms of the conventional elements like voltage and current sources, resistances, capacitances etc. in an equivalent way. By equivalence, we mean that the voltage-current characterstic across a pair of terminals of the electronic device would be maintained in the equivalent representation. Most of the conventional circuit elements have linear voltage current relationship in the useful range of operation. The electronic devices, however, do not have such a linear relation as apparent from their characteristics described in the previous chapters. Nevertheless, over small regions of voltage and current the characteristics are approximated by linear relationships. It should be emphasized here that the non-linear characteristics of devices is not a drawback. In fact their overall non-linearity is more useful. For example, the diode is able to rectify because its characteristic is not uniformly linear throughout the range, that, is both in the first and the third quadrants.

The electronic devices have characteristics which can be linearized piecewise and they can be operated over the desired range of linearity or non-linearity by biasing them properly. In this chapter our aim is to define some important parameters of the devices so that their equivalent circuits can be drawn. Once we are able to do this satisfactorily we can consider the electronic device and other circuit elements to be enclosed in a box with some terminals available outside. We are then concerned about the behaviour of the circuit at these terminals only. We talk of cause and effect or input and output in terms of the voltage and the current when one of the two is taken as the cause and the other as the effect. Most of the circuit elements have two terminals only and, in general, when they are interconnected the circuits and systems will have four terminals (or two ports)—two for the input (one port) and two for the output (one port). We thus have four quantities, voltages and currents at both the ports, in terms of which the effect and cause or the output-input relationship is required to be determined. For the purposes of reference, one out of the four terminals may be made common and we thus get 3 terminal circuits.

The relations existing between output and input voltages, output and input currents, output voltage and input current, output current and input voltage, output voltage and output current or between input voltage and input current in a 3 (or 4) terminal or a 2 port circuit is of interest to us. However complex a circuit may be, in most cases 2 ports appropriately chosen are enough to analyse the behaviour of the circuit. We shall therefore confine our attention to 2 port circuits and find the various relationships as stated above. An understanding of the physical principles, the electrical characteristics and the technology of the devices, as developed in the previous chapters, would be helpful in representing the device in the circuit form. We shall study the whole circuit finally as a black box with only the input and the output terminals as the terminals of interest.

In a two port electronic circuit or for that matter any other circuit, where we deal with the relations between the variables at the output and the input port we call the resulting relationship as the transfer parameter of the circuit or the device. Similarly, when the relations between variables at the same port are under consideration we call them the input or the output driving point, parameters as the case may be. All of the three parameters viz, the input, output and the transfer can have dimensions of impedance or admittance. The transfer parameters may, however, have dimensionless ratios also. When we talk of the terminal characteristics of the devices or the circuits, we mean the evaluation and study of these parameters. We also wish to study the frequency response of circuit because the circuits and the systems are supposed to work over a wide range of frequencies. We therefore like to know the values of the various parameters over the whole range of frequencies of interest. Frequency response obviously, therefore, indicates how a particular parameter responds to different input frequencies. We would also like to know the dynamic range of the circuit. The dynamic range is the range of the signal amplitude or power level, either at the input or the output terminals, over which the circuit performs satisfactorily i.e., has desirable behaviour.

5.1 Driving point and transfer parameters

An electronic device or a circuit is represented by a black box with 2 ports as shown in Fig. 5.1

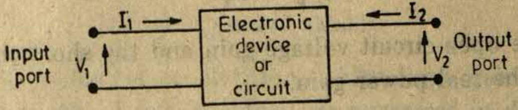


Fig. 5.1 Black box representation of Electronic circuit.

In terms of the terminal variables V_1, I_1 and V_2, I_2 we now define various driving point and transfer parameters and discuss their significance. For the sake of convenience and uniqueness, the parameters are defined under conditions of the ports being either short circuited or open circuited. Whenever current is the variable the respective terminals are shorted and the current is referred to as the short circuit current. Any other termination, other than shorting would not be unique and, therefore, the parameter would change depending upon the termination. Similarly, whenever the variable under consideration is voltage, we keep the respective terminals open and refer to it as the open circuit voltage. In some cases the parameters may also be defined for a given termination.

5.1.1 TRANSFER PARAMETERS

In electronic circuits one of the most popular transfer parameter is the voltage gain G_v defined as the ratio of the open-circuit output voltage V_2 to the open-circuit input voltage V_1.

$$\text{Voltage gain, } G_v = \frac{V_2}{V_1} \tag{5.1.1}$$

The voltage gain G_v is of primary importance in all types of amplifiers. Another transfer parameter is the current gain G_i defined as the ratio of the output short-circuit current I_2 to the input short-circuit current I_1

$$\text{Current gain } G_i = \frac{I_2}{I_1} \tag{5.1.2}$$

The current gain parameter G_i is used extensively in bipolar transistors because their basic operation depends upon current flow. Since in vacuum tubes and FETs there is no input current practically the current gain is not usually used as a parameter of any importance. It has been explained earlier that it is neither the voltage nor the current gain in isolation which makes an amplifier. All amplifiers must have power gains G_p, defined as the ratio of the output power P_2 to the input power P_1, larger than unity. Input and output powers are usually measured across a resistance or a load. Then the power gain is given by

$$G_p = \frac{P_2}{P_1} = \left. G_v \right]_{\text{load}} \times \left. G_i \right]_{\text{load}}$$

$$< G_v \times G_i \qquad (5.1.3)$$

The product of the open-circuit voltage gain and the short circuit current gain of eq. (5.1.3) is not the real power gain.

Now, either G_v or G_i may be less than unity in a particular amplifier but we get an amplification so long as the product is greater than unity. In common base amplifier for example, the current gain is less than unity but the voltage gain is much more than unity and we get overall power gain. In common collector amplifier, the voltage gain is less than unity but current gain is much greater than unity and once again a power gain is achieved. In common emitter amplifiers both the voltage and the current gains are greater than unity and so the power gain is obviously greater than unity. A signal is amplified only when its power and hence energy is increased. We should remember that amplification does not violate the law of the conservation of energy. If fact the amplifier converts d.c. energy into the signal energy. All amplifiers consisting of active devices require d.c. voltage and current for their operation. The d.c. voltage and the current are controlled by the input signal in such a manner that at the output of the amplifier the same signal appears with a larger energy taken from the D.C. supply.

A word of caution is necessary here. The power gain and the ability of an electronic circuit to give out large powers are two different things. All electronic amplifiers have power gain greater than unity but all of them do not have capability to give large power outputs. When the power output is small, we call the amplifier as voltage or current amplifier depending on which gain is larger and more useful in a particular situation. When the power output is large, we call the amplifier as a power amplifier.

The three ratios G_v, G_i, and G_p are dimensionless quantities and are usually expressed in dB (deci Bel) defined as

$$[G_p]_{dB} = 10 \log G_p$$

$$= 10 \log_{10} \frac{P_2}{P_1} \qquad (5.1.4a)$$

$$[G_v \text{ or } G_i]_{dB} = 20 \log_{10} [G_v \text{ or } G_i] \qquad (5.1.4b)$$

The advantage of using this unit is that when many circuits are connected in tandem or cascade, without affecting each other, as shown in Fig. 5.2, then the overall gain G in dB is simply the sum of individual gains in dB. Thus

$$G = G_1 G_2 G_3$$

$$\text{or} \quad G_{dB} = G_{1\,dB} + G_{2\,dB} + G_{3\,dB}$$

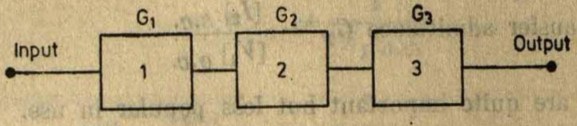


Fig 5.2 Cascaded circuits

and multiplication is converted to addition. Also large gains can be expressed by small and manageable numbers if they are expressed in dB. Table 5.1 gives conversion of voltage, current and power gain from ratio to dB and vice versa.

Table 5.1 Gain Ratio and dB

dB	Voltage or current gain Ratio	Power gain Ratio	Voltage or current gain Ratio	Voltage or current gain dB	Power gain dB
1	1.220	1.259	1	0	0
2	1.259	1.585	2	6.021	3.010
3	1.413	1.995	3	9.542	4.771
4	1.585	2.612	4	12.041	6.021
5	1.778	3.162	5	13.979	6.990
6	1.995	3.981	6	15.563	7.782
7	2.239	5.012	7	16.902	8.451
8	2.512	6.310	8	18.062	9.031
9	2.818	7.943	9	19.085	9.542
10	3.162	10.00	10	20.000	10.000
11	5.548	12.590	15	23.522	11.761
12	3.981	15.850	20	26.021	13.010
13	4.467	19.953	30	29.542	14.771
14	5.012	25.119	40	32.041	16.021
15	5.623	31.622	50	33.980	16.990
16	6.310	39.811	60	35.563	17.782
17	7.080	50.119	70	36.902	18.451
18	7.943	63.096	80	38.062	19.031
19	8.913	79.433	90	39.085	19.542
20	10.00	100.00	100	40.00	20.00
30	31.62	1000.00	200	46.021	23.010
40	100.00	10^4	500	53.980	26.990
50	316.2	10^5	1000	60.000	30.00
60	1000.00	10^6			
70	3162.27	10^7			
80	10^4	10^8			
90	3.16×10^4	10^9			
100	10^5	10^{10}			

Other transfer parameters are transfer impedances and transfer admittances defined as follows ;

$$\text{Transfer Impedance } G_Z = \frac{[V_2]_{o.c.}}{[I_1]_{s.c.}} \qquad (5.1.5)$$

$$\text{Transfer admittance } G_Y = \frac{[I_2]\ s.c.}{[V_1]\ o.c.} \tag{5.1.6}$$

These parameters are quite important but less popular in use.

So far we have taken the ratios of output variables to the input variables. The reason is that most of the electronic circuits are unilateral and the output quantities are dependent on the input qantities which are themselves independent variables. These ratios are truely known as forward parameters and have moderate values. The reverse parameters, that is, the ratios of the input to the output variables are also taken and these are quite small. They are in fact non-zero because of the non-ideality of the device, leakage currents and parasitic effects. Thus reverse gains are

$$G_{Vr} = \left[\frac{V_1}{V_2}\right]_{o.c.} \tag{5.1.7a}$$

$$G_{Ir} = \left[\frac{I_1}{I_2}\right]_{s.c.} \tag{5.1.7b}$$

The reverse impedance and admittance are

$$G_{Zr} = \frac{[V_1]_{o.c.}}{[I_2]_{s.c.}} \tag{5.1.8a}$$

$$G_{Yr} = \frac{[I_1]_{s.c.}}{[V_2]_{o.c.}} \tag{5.1.8b}$$

5.1.2 DRIVING POINT PARAMETERS

The most important driving point parameters are the input and the output impedance of the elecronic circuits. They are defined as driving point input impedance, z_I

and
$$Z_I = \frac{V_1}{I_1} = \frac{1}{Y_I} \tag{5.1.9}$$

driving point output impedance, z_O

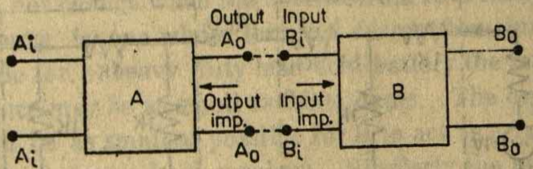
$$Z_O = \frac{V_2}{I_2} = \frac{1}{Y_0} \tag{5.1.10}$$

Whenever the parameters on one port are being calculated the other port has a specified termination. Usually, when the impedance at one port is considered the other port is open circuited, and when the admittance is considered the other port is short circuited. It should be noted that

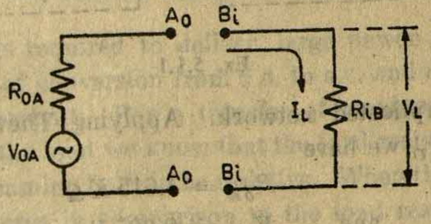
$$[Y_I]\ s.c. \neq \frac{1}{[Z_I]o.c.}$$

$$\text{and} \quad [Y_0]\ s.c. \neq \frac{1}{[Z_o]o.c.}$$

We shall now discuss the significance of the input and output impedances of a circuit. The input impedance is the effective impedance the electronic circuit under consideration will offer at its input port to any source or circuit connected to it. If the input impedance of the circuit is small then it may draw current from the source or the circuit to which it is connected and affect its working. On the other hand, if the input impedance is high the circuit under consideration does not draw any significant amount of current at its input port. Consider the two circuits *A* and *B* shown in Fig. 5.3(a) being connected together. It will be important to know the amount of current the circuit *B* will take at its input port from the circuit *A* and whether *A* can deliver that current at its output port.



(a) Inter connection of A and B



(b) Equivalent connection

Fig. 5.3 Connection of two circuits

The output impedance of a circuit is the effective impedance across the output terminals where some other circuit or load will be connected. The output impedance of the circuit *A* gives an idea of how much A will be affected by connecting the circuit *B* at its output as shown in Fig. 5.3(a). The circuit *A* is represented at its output terminals A_O-A_O by an equivalent output impedance R_{oA} and voltage source V_{oA}. This can be done by applying Thevenin's theorem to the left of the terminals A_OA_O. The circuit *B* can be represented at its input port by an equivalent input resistance R_{iB}. The current I_L through R_{iB} and the voltage V_L across it are given as

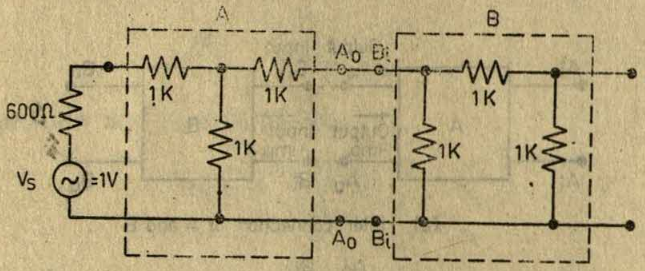
$$I_L = \frac{V_{oA}}{R_{oA}+R_{iB}} \tag{5.1.11}$$

$$V_L = I_L \times R_{iB} = \frac{R_{iB}}{R_{oA}+R_{iB}} \cdot V_{oA} \tag{5.1.12}$$

Using eq. 5.1.11 we can calculate I_L since V_{oA}, R_{iB} and R_{oA} are known. We should now ascertain that the circuit A is capable of giving out the current I_L. The voltage V_L is not equal to V_{oA} as seen from eq. 5.1.12. Both I_L and V_L depend on the output and input impedances R_{oA} and R_{iB}. If it is desired to have V_L approximately equal to V_{oA}, then either $R_{oA} \approx 0$ or $R_{iB} \gg R_{oA}$.

Example 5.1.1

Two circuits A and B are connected together as shown in Ex. 5.1.1. The circuits inside the boxes are represented in T and π form, the most general equivalent representation of any complicated network. Applying Thevenin's theorem to the left of terminal A_0—A_0 we have



Ex. 5.1.1

$$R_{oA} = 1.615\,K\Omega$$

$$\text{and} \quad V_{oA} = 0.385\,V$$

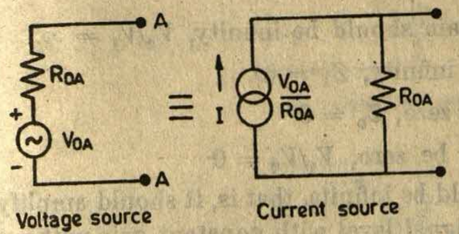
Similarly R_{iB} is found as $0.667\,K$.

$$\text{Hence } I_L = 0.169\,\text{mA}$$

$$\text{and } V_L = 0.113\,\text{volts.}$$

We thus find that the current drawn from A changes as R_{iB} changes and the terminal behaviour of A may change in this process. Similarly different output resistance R_{oA} would cause different voltages to be impressed on the circuit B and thus may affect the terminal behaviour of B. To evaluate this interaction, it is important to know the input and output impedances or resistances of the circuits.

A source can be represented in the form of an open circuit voltage V_{oA} and a series resistance R_{oA}. The circuit of A above, for example, can be considered as an equivalent source. We call this a voltage source representation. We can also represent it by a current source form that is by a current source $I = \left(\frac{V_{oA}}{R_{oA}}\right)$ in parallel with a resistance R_{oA} as shown in Fig. 5.4.



Voltage source Current source

Fig. 5.4 Voltage and current sources

So far as the terminals $A-A$ are concerned, the two representations are exactly equivalent. For an ideal voltage source, the output resistance $R_{oA} = 0$.. Then the terminal voltage $A-A$ does not drop when another circuit in the form of a load or a next stage is connected. For an ideal current source, the output resistance $R_{oA} = \infty$. In such a situation the total source current goes to the load or the next stage without being shunted in the internal resistance R_{oA}. We can now define the ideal voltage source as one whose terminal voltage does not change when the current from it is changing. Similarly the ideal current source is one whose terminal current remains constant at all voltages. For example for a heavy duty lead-acid battery the internal resistance or the source resistance may be as small as 0.004 ohms. The output impedence of an amplifier should be as small as possible for it to act as a voltage source to deliver power to a load (say a loud speaker). Similarly the output impedance of the amplfier should be very large for it to act as a current source.

When an amplifier is required to deliver large power to a load then the questions of its efficiency of conversion from d.c. to a.c. and the maximum power transfer become very important. For a transfer of maximum power from the source or the amplifier to the load we know that the load resistance must be equal to the source resistance assuming both to be resistive. When the output impedance of the amplifier is quite large in comparison to the load resistance, some impedance matching device such as a transformer is used so that maximum power transfer can be affected. The question of maximum power transfer also becomes very important when the signal power is very small as in case of some transducers where no loss of signal can be tolerated. However, if the source impedance is very small as compared to the load resistance then it is not necessary to match the resistances. We thus find that in electronic circuits the input and output impedances play a very important part.

5.2 Ideal amplifier

We have explained what an amplifier is. It can be represented as a^{14} terminal electronic circuit and its terminal behaviour in terms of the driving point and transfer parameters can be determined by analysis or measurement. At this point a natural curiosity arises in our minds. What is an ideal amplifier or in other words what should be the terminal parameters of an amplifier ? The answer to this question is quite simple in the light of the discussions so far in the previous sections and chapters. The ideal amplifier should have the following characteristics.

(1) Its voltage gain or the current gain should be infinity, $V_2/V_1 = \infty$.

(2) The input impedance should be infinity, $Z_1 = \infty$.

(3) The output impedance should be zero, $Z_o = 0$.

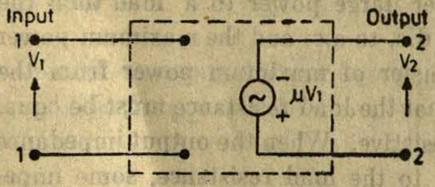
(4) The reverse transmission should be zero, $V_1/V_2 = 0$·

(5) The signal handling capacity should be infinite, that is, it should amplify the smallest to largest possible signal level with constant gain without producing any distortion. and

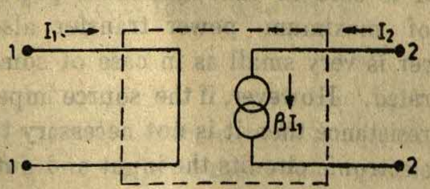
(6) The bandwidth should be infinite, that is, it should equally amplify all frequencies from zero to infinity.

Obviously all these characteristics cannot be realized in practical amplifiers. We aim to design amplifiers which approach these characteristics and analyse practical amplifiers to check how far we have achieved them.

We have seen that an amplifier can be thought of as a controlled source which converts the D.C. energy from the power supply to the a.c. energy controlled by the input signal. From this view point an equivalent circuit of an ideal amplifier can be drawn as shown in Fig. 5.5. Both the controlled voltage and current source equivalent circuits have been shown. In the voltage source circuit the input V_1 is amplified μ times and appears as controlled voltage source of μV_1 in the output circuit. Similarly in the current source circuit, the input current I_1 is amplified β times and produces a controlled current source βI_1 in the output circuit. Both the output and the input circuits are isolated in the reverse direction. As has been mentioned earlier. Such ideal amplifiers are not practically realizable and therefore we have to introduce some approximations. The important approximations are the finite input and non-zero output impedances. The practical amplifier will have an equivalent circuit like that shown in Fig. 5.6. Both the circuits of Fig. 5.6 can be combined into a convenient single circuit as shown in Fig. 5.7.



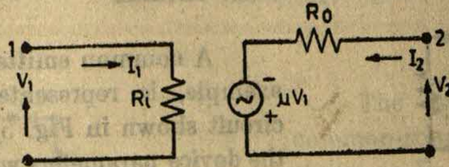
(a) Controlled voltage source



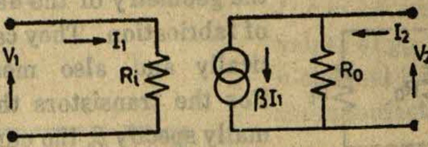
(b) Controlled current source

Fig. 5.5 Equivalent circuits of Ideal Amplifier

In all the equivalent circuits R_i represents the input resistance and R_o the output resistance. In the controlled voltage source equivalent circuit of Fig.



(a) Controlled voltage source



(b) Controlled current source

Fig. 5.6 Practical amplifier equivalent circuits

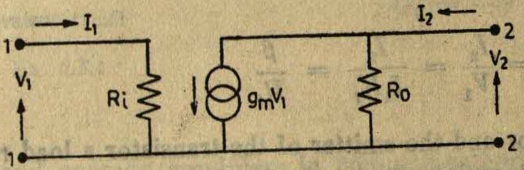


Fig. 5.7 Practical amplifier equivalent circuit

5.6(a) μ represents the voltage amplification factor. In controlled current source circuit of Fig. 5.6(b) β represents the current amplification factor. Both μ and β are the transfer parameters and are dimensionless. The g_m as in Fig. 5.7 on the other hand is the transconductance (transfer conductance) and has the dimension of mhos.

The g_m is given by

$$g_m = \frac{[I_2]_{sc}}{[V_1]_{oc}} \tag{5.2.1}$$

5.2.1 EQUIVALENT CIRCUIT OF ACTIVE DEVICE

The equivalent circuits described above represent the actual circuit at its four terminals of input and output. The circuits themselves are visualsed as a black box and inside the black box there may be a simple or a complex amplifier. The amplifiers may be using BJT, FET, triode or pentode as the basic active device producing amplification. The devices themselves can also be represented by an equivalent circuit and the equivalent circuit again looks like the one shown in Fig. 5.7. As long as the reverse transmission is assumed to be zero the equivalent

$I_P = 10$ mA are given as

$$g_m = 5.5 \times 10^{-3}\,℧$$
$$R_O = 10.9\ \text{K}\,\Omega$$

$$\text{Then } G_V = g_m \frac{R_O \times R_L}{R_O + R_L}$$

R_O and R_L are comparable in triodes.

For a typical pentode at a plate current of 9.0 mA, the values of g_m and R_O are

$$g_m = 4 \times 10^{-3}\,℧$$
$$R_O = 750\ \text{K}$$

Therefore gain $G_V = -g_m R_L$

since $R_O \gg R_L$

If $R_L = 10$ K Ω, then gain $= -40$.

We see that the same type of equivalent circuit as given in Fig. 5.7 is good for all the devices. Only the values of parameters R_i, R_O and g_m change from device to device. These parameters are specified by the manufacturers in various forms and can also be derived from the static characteristics discussed in the previous chapter. Thus the slope of the output *v-i* characteristics $\frac{\partial i}{\partial v}$, at a given point gives $\frac{1}{R_O}$ at that point. Similarly the slope $\frac{\partial i}{\partial v}$ of the input *v-i* characteristics gives $\frac{1}{R_i}$. Since in the tubes and the FETs the input current is very small, R_i is infinite.

The slope $\frac{\partial i_{out}}{\partial i_{in}}$ of the transfer characteristic of the BJT would give β from which g_m can be easily calculated. Since the output current versus input current characteristics for the BJT is a straight line it is not usually drawn and β is simply specified. However for the vacuum tubes and the FETs the output current versus input voltage transfer characteristics $\frac{\partial i_{out}}{\partial v_{input}}$ give the transconductance g_m of the device. The representation of Fig. 5.7 is not unique for the devices and circuits. Based on the ideas of the four-terminal network theory different equivalent circuits have been proposed. Some of these have also been used extensively in the literature and in practice. We shall describe in the next section two of the popular equivalent circuits.

5.3 Hybrid and T-parameters of transistors

Many manufacturers give the hybrid or the *h* parameters for the transistors because they are easy to measure and give the input impedance, output admittance and the current gain directly. Another set of parameters known as *T* parameters find use in transistors because they are based on the physical model of the transistor and are simpler to use in approximate analysis of the transistor circuits. Both these equivalent circuits are discussed here.

Considering the transistor to be a black box with two input and two output terminals, we can model its behaviour by knowing the terminal quantities V_1, V_2, I_1 and I_2. We can represent any two of the 4 quantities as the independent variables and the other two as the dependent variables. Since the transistor is a current controlled device basically, we take I_1 and V_2 as the independent variables and represent V_1 and I_2 as

$$V_1 = h_{11}\, I_1 + h_{12}\, V_2 \qquad (5.3.1)$$

$$I_2 = h_{21}\, I_1 + h_{12}\, V_2 \qquad (5.3.2)$$

Alternatively the above equations can be written in the matrix form as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Coefficients h_{11}, h_{12}, h_{21} and h_{22} are known as the hybrid parameters. Using eq. (5.3.1) and (5.3.2), the *h* parameters can be determined easily. If for instance $V_2 = 0$, that is the output terminals are short circuited, then

$$V_1 = h_{11}\, I_1 \qquad \text{and } I_2 = h_{21}\, I_1$$

Therefore

$$h_{11} = \left.\frac{V_1}{I_1}\right]_{V_2 = 0} \qquad (5.3.3)$$

and

$$h_{21} = \left.\frac{I_2}{I_1}\right]_{V_2 = 0} \qquad (5.3.4)$$

Similarly, if $I_1 = 0$, or the input terminals are open circuited, then

$$V_1 = h_{12}\, V_2 \quad \text{and} \quad I_2 = h_{21}\, I_1$$

Thus

$$h_{12} = \left.\frac{V_1}{V_2}\right]_{I_1 = 0} \qquad (5.3.5)$$

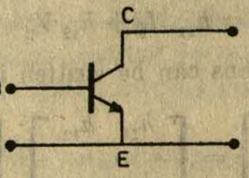
and

$$h_{22} = \left.\frac{I_2}{V_2}\right]_{I_1 = 0} \qquad (5.3.6)$$

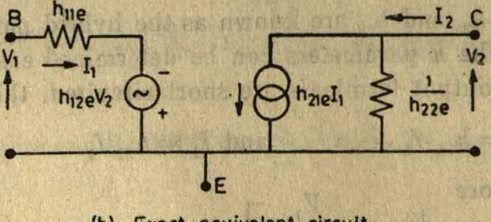
We see from eq. (5.3.3) and (5.3.6) that h_{11} is an input impedance and h_{22} is an output admittance. The eqs. (5.3.4) and (5.3.5) show that h_{12} is the reverse voltage gain and h_{21} is the forward current gain. As we can see, these parameters are a mix of impedance and admittance and voltage ratio and current ratio. They are therefore called the hybrid parameters. Sometimes the hybrid parameters are also designated as

$h_{11} = h_i$ (Input impedance)
$h_{12} = h_r$ (Reverse voltage feedback ratio)
$h_{21} = h_f$ (Forward current transfer ratio)
$h_{22} = h_o$ (output admittance).

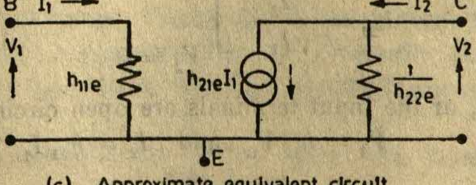
Considering the CE configuration and adding a subscript to the h-parameters we can represent the two equations in the form of an equivalent circuit as shown in Fig. 5.9. As assumed the reverse transmission can be neglected and thus $h_{12} \approx 0$. We can now connect other external components to this circuit and analyse it by usual circuit techniques. The parameters h_{11e}, h_{21e} and h_{22e} can be measured,



(a) The transistor



(b) Exact equivalent. circuit



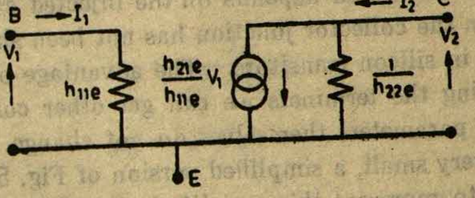
(c) Approximate equivalent circuit with $h_{12e} = 0$

Fig. 5.9 h-parameter CE equivalent circuit as has been mentioned earlier, and are also specified by the manufacturer. The parameters for the CC and CB configuration can similarly be defined and measured. The conversion from one set of parameters of, say, CE to other parameters of CB and CC can be worked out and are given in Table 5.2 below.

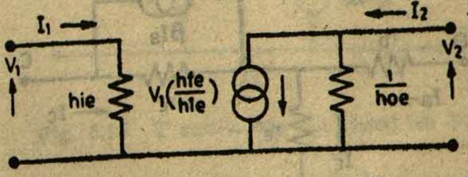
Table 5.2

Common Collector (approximate)	Common Base (approximate)
$h_{ic} = h_{ie}.$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
$h_{rc} = 1$	$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$
$h_{fc} = -(1+h_{fe})$	$h_{fb} = -\frac{h_{fe}}{1+h_{fe}}$
$h_{oc} = h_{oe}$	$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

The current controlled current source in Fig. 5.9 can be replaced by a voltage controlled current source as shown in Fig. 5. 10 by simply noting that I_1 is also given as $\frac{V_1}{h_{11e}}$. Comparing the circuits of Figs. 5.10, 5.7 and 5.8 we find



(a) In terms of general notation



(b) In terms of functional notations

Fig. 5.10 Equivalent ckt. of CE Transistor with voltage controlled current source

that R_i = input impedance
$$= h_{11e} = h_{ie} \qquad (5.3.7a)$$

$$g_m = \text{transconductance} = \frac{h_{21e}}{h_{11e}} = \frac{h_{fe}}{h_{ie}} \qquad (5.3.7b)$$

$$\text{and } R_o = \text{output impedance} = \frac{1}{h_{22e}} = \frac{1}{h_{oe}} \qquad (5.3.7c)$$

We can also see that

$$h_{21e} = h_{fe} = \beta = \text{current gain of the transistor.} \qquad (5.3.7d)$$

5.3.1 T-PARAMETERS

We shall now describe an equivalent circuit of the transistor based on its physical structure. This equivalent circuit as shown in Fig. 5.11, is in terms of the internal resistances of the device. It is generally known as the *T* equivalent circuit of the transistor because the 3 arms form a *T*. The emitter-base junction is forward biased and acts like a diode with a resistance r_e given by

$$r_e = \frac{Tk}{q} \cdot \frac{1}{I_E} = \frac{25 \times 10^{-3}}{I_E} \qquad (5.3.8)$$

The ohmic resitsance between the base terminal and the active region somewhere in the base region of the transistor is represented by r_b and is known as the base spreading resistance. The value of this resistance is somewhere between 50 to 100Ω in practical transistors. The reverse biased collector offers a resistance r_c which is usually very high (of the order of Megaohms). The current souce represents the collector current which depends on the injected carrier at the emitter. The leakage current in the collector junction has not been shown, since it is very small, particularly so in silicon transitors. The advantage of *T* the model is that by simply interchanging the terminals we can get other configurations such as CB and CC, and the parameters themselves do not change. Since r_c is usually quite large and r_b is very small, a simplified version of Fig. 5.11 is shown in Fig. 5.12. If we now try to represent this simplified circuit in the form of Fig. 5.8,

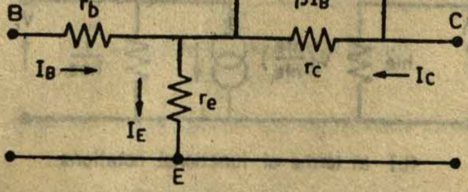


Fig. 5.11 T-equivalent circuit of the CE transistor

we shall get the circuit of Fig. 5.13. Here the base to emitter voltage V_{BE} is given by

$$\begin{aligned} V_{BE} &= r_e \cdot I_E \\ &= r_e \cdot (I_B + \beta I_B) \\ &= r_e (1 + \beta) . I_B \end{aligned}$$

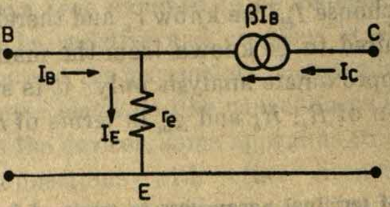


Fig. 5.12 Simplified T model of CE transistor

Hence, we get the circuit of Fig. 5.13. The collector current is given as βI_B

which is equal to $$\frac{\beta V_{BE}}{(1+\beta) r_e} = g_m . V_{BE}$$

Therefore, $$g_m = \frac{\beta}{(1+\beta)\, r_e}$$

Since β is much greater then unity $g_m \cong \frac{1}{r_e}$ (5.3.9)

From eq. (5.3.8) we obtain

$$g_m = \frac{I_E}{25 \times 10^{-3}}$$

or $$g_m = 40\, I_E \qquad (5.3.10)$$

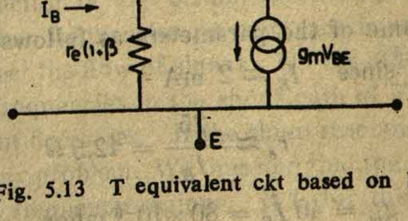


Fig. 5.13 T equivalent ckt based on V_{BE}

We can now express the parameters of the circuit shown in Fig. 5.8 in terms of the T-parameters.

$$R_i = (1 + \beta)\, r_e \qquad (5.3.11)$$

$$g_m = \frac{1}{r_e} \tag{5.3.12}$$

and
$$R_o = r_c \tag{5.3.13}$$

One great advantage of the T model is that it has brought out a parmeter r_e which is dependent of I_E (or I_C since $\alpha \approx 1$) as given by eq. (5.3.8). Because of this, once we know I_E or choose I_E, we know r_e and therefore we know R_i and g_m. Only β or h_{fe} is required to be known from the manufacturer's data sheet. Though this gives us an approximate analysis only it is sufficient in most practical situations. The relation of R_i, R_o and g_m in terms of h and T parameters are summarised in Table 5.3

Table 5.3 Summary of terminal parameters in terms of h and T parameters of common emitter transistor

		h-parameter	T parameter
Current gain		$h_{fe} = h_{21e}$	$\beta = \dfrac{\alpha}{1-\alpha}$
Input Resistance	R_i	$h_{ie} = h_{11e}$	$(1+\beta)\, r_e \approx \dfrac{25 \times 10^{-3}}{I_E}\beta$
Transconductance	g_m	$\dfrac{h_{fe}}{h_{ie}}$	$\dfrac{\beta}{(1+\beta)\, r_e} \simeq 40\, I_E$
Output Resistance	R_o	$\dfrac{1}{h_{oe}} = \dfrac{1}{h_{22e}}$	r_c

Example 5.3.1

In an *npn* silicon transistor, the collector current is 2mA and β at this current is 80. We should remember that β varies with the collector current and from unit to unit. In fact the β may vary over a large range like 60-240 from one piece to another.

We can calculate some of the parameters as follows

$$\text{since} \quad I_E \approx 2 \text{ mA}$$

$$r_e \approx \frac{25}{I_E} = 12.5\,\Omega$$

also
$$g_m = 40\, I_E = 80 \times 10^{-3} \text{ mhos}$$

$$h_{ie} = R_i = (1+\beta)\, r_e = 1.00 \text{ K}$$

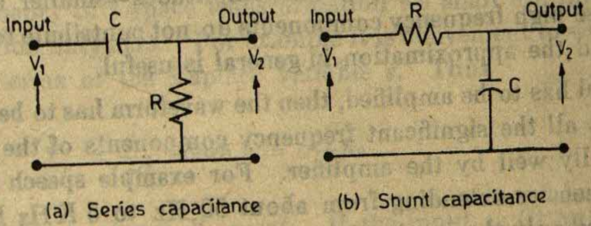
The slope of the output characteristics is 125 K. Hence

$$r_c = 125 \text{ K}$$

$$h_{oe} = \frac{1}{r_c} = 8\ \mu\ \text{mhos.}$$

5.4 Frequency dependence of terminal characteristics

We have so far discussed the terminal behaviour of circuits and devices in terms of the input and output resistances and voltage and current gains. These terminal parameters have been assumed to be frequency independent, that is, they have been assumed to be resistive and constant at all frequencies. In practice this is not the situation and the parameters change with frequency. The reason is the presence of reactive elements like capacitances in the circuit. Some capacitances are inherent in the devices, some appear as stray and parasitic shunt capacitances because of connections with other circuits and some are externally connected purposely for various requirements. They cause the output and input inpedances and the voltage and the current gains to change with frequency. They either appear in the series path of the signal as shown in Fig. 5.14 (a) or shunt the output and the input terminals as shown in Fig. 5.14(b).



(a) Series capacitance (b) Shunt capacitance

Fig. 5.14 Capacitances in circuits

We know that the reactance of a capacitor $X_c = \frac{1}{\omega C}$ is very high at low frequencies and decreases at high frequencies. When the reactance increases in the series path at low frequencies and becomes comparable or higher than the resistance R, it prevents the signal from flowing onwards and thus decreases the output. The series capacitor in Fig. 5.14(a) therefore becomes effective only at low frequencies. At higher frequencies its reactance is very small in comparison to R and it does not effect the flow of signal. On the other hand when the reactance decreases at higher frequencies in the shunt path of Fig. 5.14(b) the signal is bypassed and the output decreases. If the shunt reactance is large in comparison to R it does not cause any problem. We thus find that the different capacitors become effective in different frequency regions. It is for this reason that we divide the operation and analysis of the circuits in three regions—low frequency, middle frequency and high frequency. The middle frequency region is that where the series and the shunt capacitors are not effective and the circuit is considered only resistive. In the high frequency region the shunt capacitors only are effective and the series one can be neglected. In the low frequency region the series capacitor only is considered and the shunt ones are neglected. The circuit in Fig. 5.14(a) is known as the high pass filter and the circuit in Fig. 5.14(b) is the low pass filter.

We see that almost all devices and circuits have either a series, a shunt or a combination of both capacitors modifying the terminal behaviour at different frequencies. Now the signals to be amplified by these circuits are complex themselves and consist of a large number of frequency components. The signal frequencies extend over a band and the difference between the highest and the lowest frequency component, f_H and f_L, is designated as the bandwidth W of the signal.

Thus $$W = f_H - f_L$$

The bandwidth W is mostly governed by f_H since $f_H \gg f_L$. The rate of the change of amplitude of the signal from one instant of time to another governs the highest frequency component f_H present. If the change is abrupt or fast then f_H is very high and W is large. Theoretically f_H may be infinity but in practice we ignore high frequency components having small amplitudes—smaller by a factor of 10^3 or more. These high frequency components do not contribute really to the waveform much and the approximation in general is useful.

If a signal has to be amplified, then the waveform has to be preserved. This will mean that all the significant frequency components of the signal should be amplified equally well by the amplifier. For example speech signals occupy a band of frequencies extending from about 50 Hz to 5 KHz but for telephone purposes we use only the band of frequencies from 300 Hz to 3.4 KHz. It was found that this band is sufficient for the communication of speech information. High fidelity (Hi-Fi) music on the other hand occupies a band of 20 Hz to 20 KHz. A good quality Hi-Fi amplifier, therefore has to amplify all the signal frequencies in this band equally well without any distorition. The bandwidth of the colour TV picture signals is 0 to 7 MHz. Some of the industrial signals may have small bandwidths limited to few hertz only.

So far we have been accustomed to describing the signals in the time domain i.e., variation of amplitude with time, Fig. 3.21. However, we notice from the discussion above that the signals occupy a certain band of frequencies and the amplifiers have to work over that band. The amplifiers, therefore, have to have two characteristics. One is the ability to reproduce the dynamic variations of the signal in amplitude-time domain and this has been designated as the dynamic range of the amplifier. The second is the ability to reproduce the band of frequencies of interest in the signal. Dynamic range is normally limited by the linearity of the devices and the noise level of the devices and the circuits. It is the ability to reproduce the band of frequencies which is of the more interest here and all the analysis and design of electronic circuits is mainly concerned with this.

We have shown that both the circuits and signals are limited in frequency range and a better insight into the electronic circuits is obtained if we use the frequency domain description. It will be essential to describe the signal in the frequency domain in order that we can study the affect of the amplifier on the signals. There is another angle to the problem here which forces us to change over to the frequency domain for the analysis and the design. All the real life signals are complex in nature. They are nonrepetitive and are random. In other words it is impossible to write an analytical expression for the signal as a functionof time. For example, there are infinite number of waveforms for a speech signal but all the signals occupy a given bandwidth of say 300 Hz—3.4 KHz. If the amplifier does not pass all the frequencies properly we can immediately see its effect. Thus, it is seen that a frequency domain description of the signal and the circuits is very convenient for the analysis and design of systems.

One of the most popular techniques to convert the time domain description to a frequency domain one is the use of Laplace transorm. Rules for transforming a time function to a frequency function and vice versa are all defined. Instead of going into the theory of Lapace transrormation we shall use this concept of domain transformation only here. For example it is convenient to write the capacitor reactance in terms of the Laplace variable s. Thus

$$X_c = \frac{1}{sC} \text{ where } s = \sigma + j\omega$$

Similarly the inductive reactance $X_L = sL$. If the input $v_1(t)$ and the output $v_2(t)$ are also considered in terms of their Laplace Transforms V_1(s) and V_2(s), Then the ratio of V_2(s)/V_1(s) is known as the transfer function $H(s)$ of the circuit or the system. Thus

$$H(s) = \frac{V_2(s)}{V_1(s)} \tag{5.4.1}$$

Once we know the transfer function $H(s)$ we can calculate the output $V_2(s)$ for any input signal $V_1(s)$ by multiplying $H(s)$ with $V_2(s)$. The output quantity as a function of time $v_2(t)$ is obtained by taking the inverse Laplace transform of $V_2(s)$. Thus, we finally go back to the time domain. Among many other advantages of such a technque of solving the problem, the mathematical manipulations in terms of s become very simple and convenient. For instance, the transfer function of the circuit in Fig. 5.14 (b) can be written as follows

$$V_2(s) = \frac{V_1(s)}{R + \frac{1}{sC}} \times \frac{1}{sC}$$

$$\text{or} \quad \frac{V_2(s)}{V_1(s)} = H(s) = \frac{1}{1+sCR}$$

$$\text{or} \quad H(s) = \frac{1/CR}{s+\dfrac{1}{CR}} \tag{5.4.2}$$

We notice that if we make $s = -\dfrac{1}{CR}$ (physically not possible) we find from eq. (5.4.2) that $H(s)$ is infinite. Such a frequency where the transfer function is infinie is known as the 'pole' of the transfer function. Thus $s = -\dfrac{1}{CR}$ is the pole of $H(s)$. The product CR is known as the time constant of the circuit. Similarly if for some value of s the value of $H(s)$ becomes zero then that frequency is known as the 'zero' of the transfer function. We shall now analyse the two circuits of Fig. 5.14 and deterine their frequency characteristics.

5.4.1 Low Pass Filter

A simple low pass filter is shown in Fig 5.14 (b). It has a transfer function given by eq. (5.4.2). We are interested in finding how the output changes as the input frequency is changed. In the transfer function of Eq. (5.4.2) we replace s by jw to obtain

$$H(j\omega) = \frac{1/CR}{j\omega+\dfrac{1}{CR}}$$

We can determine the magnitude $|H(j\omega)|$ and phase $\underline{|H(j\omega)} = (j\omega)$ of this complex function. Putting for convenience $\dfrac{1}{CR} = \omega_1$ we obtain

$$H(jw) = \frac{\omega_1}{j\omega+\omega_1}$$

Thus

$$|H(j\omega)| = \frac{1}{\sqrt{1+(\omega/\omega_1)^2}} \tag{5.4.3}$$

and

$$\theta(j\omega) = \tan^{-1}\left(-\frac{\omega}{\omega_1}\right) \tag{5.4.4}$$

The frequency and phase responses of eq. (5.4.3) and (5.4.4) are plotted in Fig. 5.15(a) and (b) respectively.

If the input voltage is kept constant then it is seen from the figure that the magnitude response and hence the output voltage is constant upto a certain frequency. Beyond this frequency the ouput decreases with the increasing frequency. At a frequency $w = w_1$, we see that

$$|H(jw)| = \frac{1}{\sqrt{2}} = 0.707$$

$$\text{or} \quad V_2(jw) = 0.707\, V_1(jw)$$

$$\text{or} \quad V_2^2(jw) = 0.5\, V_1^2(jw)$$

This shows that the output power $\frac{V^2}{R} = V^2 \text{ if } R = 1$ is halved at $w = w_1$.

This frequency $w_1 = \frac{1}{RC}$ is known as the 3dB frequency because the output power drops by 3 dB. In terms of voltage the output voltage reduces to 0.707 times its value at zero frequency. This frequency is also known as the out-off or corner frequency. The output lags in phase the input by 45° at this frequency. We can express $|H(jw)|$ in dB as

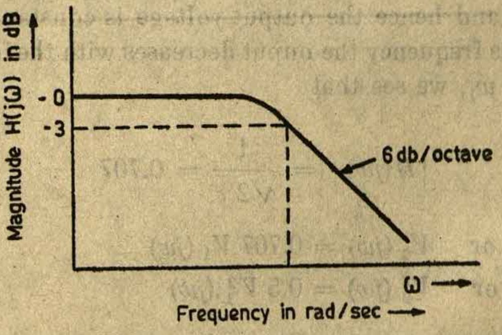
$$|H(jw)|_{dB} = 20 \log \frac{1}{\left[1 + \left(\frac{\omega}{\omega_1}\right)^2\right]^{1/2}} \tag{5.4.5}$$

$$= 10 \log \left[1 + \left(\frac{\omega}{\omega_1}\right)^2\right]^{-1}$$

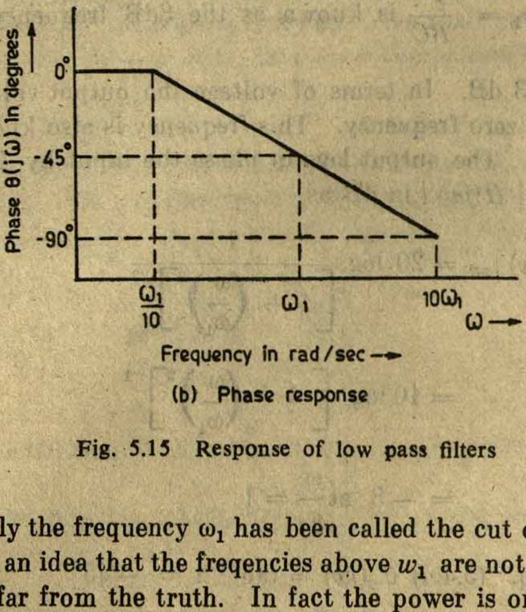
$$= -3 \quad \text{at} \frac{\omega}{\omega_1} = 1$$

Similarly from eq. (5.4.4) $\theta\,(jw) = \tan^{-1} 1 = -45°$

For large values of w when $\frac{\omega}{\omega_1} \gg 1$ the eq. (5.4.5) shows that the magnitude of the transfer function changes by 6dB if the frequency is doubled. This will mean that the slope of the response curve in Fig· 5.15(a) will be 6dB/octave change of frequency. This change is also expressed as 20dB/decade if the frequency is changed 10 times. Similarly the phase change at frequencies greater than $10w_1$ is approximately -90 degrees. It can be assumed that for frequencies smaller than $\omega_1/10$ the phase change is negligible. The phase curve, therefore can be approximated by the straight lines shown in Fig. 5.15(b).



(a) Magnitude response



(b) Phase response

Fig. 5.15 Response of low pass filters

Conventionally the frequency ω_1 has been called the cut off frequency and it brings to our mind an idea that the freqencies above w_1 are not passed through the network. This is far from the truth. In fact the power is only reduced to half or the voltage is requced to .707 times its value in the passband. Significant output is obtained at frequencies which are 10 times w_1. Even with all these limitations the terminology of a cut off frequency is very convenient to use in dealing with the frequency respnonse of networks because it gives a quantitative idea.

The circuit of Fig. 5.14(b) is called low pass obviously because it passes the low frequencies only. It is called a single order filter because the order of s in the transfer function is 1.

5.4.2 HIGH PASS FILTER

We shall next consider the high pass filter shown in Fig. 5.14(a). The transfer function $H(s)$ is given by

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{R}{R + \dfrac{1}{sC}}$$

or

$$H(s) = \frac{s}{s + \dfrac{1}{RC}}$$

or

$$H(s) = \frac{s}{s + \omega_1}, \text{ where } \frac{1}{RC} = \omega_1 \tag{5.4.6}$$

We notice that the transfer function of a high pass filter has a 'zero' and a 'pole'. The 'zero' is at $s = 0$ or the origin and the pole is at $s = -\omega_1$.

Replacing s by $j\omega$,

$$H(j\omega) = \frac{j\omega}{j\omega + \omega_1}$$

Therefore

$$| H(j\omega) | = \frac{1}{\sqrt{1 + \left(\dfrac{\omega_1}{\omega}\right)^2}} \tag{5.4.7}$$

The phase function $\theta\ (j\omega)$ is

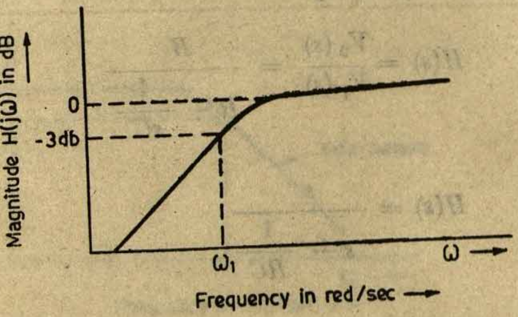
$$\theta\ (jw) = \tan^{-1}\left(\frac{\omega_1}{\omega}\right)$$

and

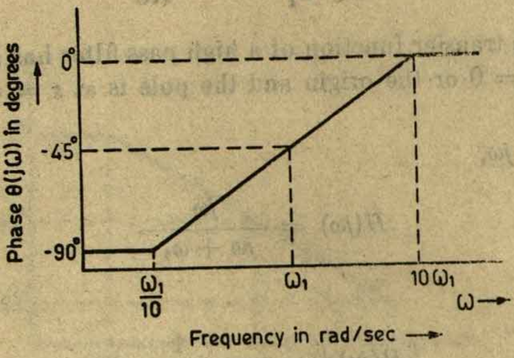
$$| H(j\omega) |_{dB} = -10 \log \left[1 + \left(\frac{\omega_1}{\omega}\right)^2\right]$$

The frequency and phase functions are plotted in Figs. 5.16(a) and (b). Here we find that as the frequency is increased the output increases upto a certain frequency and then it becomes constant.

It is a first order RC high pass filter. At $w_1 = w$, the output power falls by 3dB (voltage becomes 0.707 times) and at frequencfes much lower than this, the slope is once again 6 dB/octave. The cut-off or corner frequency is $w_1 = 1/RC$. The phase is 45° at $w = w_1$ and is 90° at $\frac{1}{10}\,w_1$ and 0° at $10w_1$ approximately as shown in Fig. 5.16. 5.16(b.



(a) Magnitude response



(b) Phase response

Fig. 5.16 High pass filter response

Normally an electronic amplifier would have both series and shunt capacitors and the frequency response will be a combination of the low pass and the high pass responses, as shown in Fig. 5.17. The two corner frequencies are known as

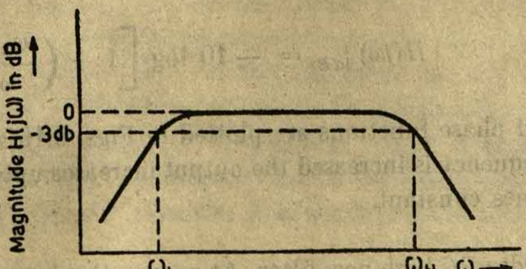


Fig. 5.17 Frequency response of amplifier.

upper and lower cut-off freqencies W_H and W_L. The region between W_H and W_L is known as the mid band and $W_H - W_L = W$ is the pass band or the bandwidth of the amplifier. Signals inside this band would be amplified without any frequency distortion.

Review questions

5.1 Show the non-linearity which a device has and is used for rectification.

5.2 What is a two port network ?

5.3 Explain what is meant by transfer parameters ? What are their possible dimensions ?

5.4 What do you understand by driving point parameters ?

5.5 Define deci Bel and explain its utility. Convert voltage and power ratios from 1 to 10 (integers only) into dB. Also convert 1 to 10 dB (only integers) into power and voltage ratios.

5.6 Explain short and open circuited parameters.

5.7 Enumerate the features of an ideal amplifier.

5.8 Draw equivalent circuits of a practical amplifier using (i) voltage controlled voltage source (ii) voltage controlled current source (iii) current controlled current source and (iv) current controlled voltage source. What are the dimensions of the coefficients ?

5.9 Define hybrid parameters for CE, CC and CB transistors.

5.10 Define T parameters of a transistor.

5.11 Draw a T-equivalent circuit of a CC transistor.

5.12 Explain how does a series capacitor affect the frequency response of a circuit.

5.13 What are sources of shunt capacitances in an electronic circuit ? How do they limit the amplifier performance ?

5.14 What do you understand by the bandwidth of an amplifier ?

5.15 What are poles and zeros of a transfer function ?

5.16 What do you understand by 3-dB cut-off frequency of a circuit ?

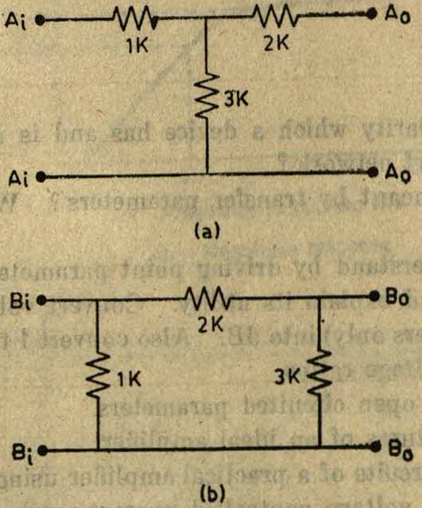
5.17 Draw typical maganitude and phase responses of an amplifier having both lower and upper cut-off frequencies.

Problems

P. 5.1 Prove that $G_p \neq G_v \times G_i$.

P. 5.2 Calculate the input and output impedances of the circuits shown in Fig. P 5.2a and P 5.2b.

P. 5.3 An ideal voltage source of magnitude 10 V is connected at the input terminals A_i A_i of the circuit in Fig. P 5.2a. Calcutlate the Thevenin's equivalent voltage source across A_o A_o.
How would the voltage across $A_o A_o$ get modified if the circuit in Fig. P 5.2b is connected in tandem with that in Fig. P 5.2a ?



(a)

(b)

Fig. P5.2

P. 5.4 Find the interrelations among the parameters of practical amplifier equivalent cicuits with (i) voltage controlled voltage source (ii) voltage controlled current source and (iii) current controlled current source.

P. 5.5 A practical amplifier with $R_i = 2\text{K}\ \Omega$, $R_o = 50\ \text{K}\ \Omega$ and $\beta = 60$ has a load resistance $R_L = 10\ K\ \Omega$. Calculate the values of β, μ, G_v and G_i.

P. 5.6 The common emitter h-parameters of a transisistor are given as

$$h_{11} = 1\ \text{K}\ \Omega \qquad h_{12} = 50 \times 10^{-6}$$

$$h_{21} = 40 \qquad h_{22} = 10^{-4}\ \mu v$$

Calculate the common base and the common collector h parameters. Also calculate R_i, R_o and g_m for the common emitter configuration.

P. 5.7 The T parameters of a transistor at $I_c = 1$ mA are given as $r_b \approx 0$, $r_c = 10\ \text{K}\ \Omega$ and $\alpha = 0.975$ Calculate R_i , R_o and g_m.

P. 5.8 Draw CB and CC equivalent circuits in terms of T—parameters.

P. 5.9 Plot the magnitude and phase responses of (i) a low pass and (ii) a high RC filters with $R = 1\ \text{K}\ \Omega$ and $C = 0.1\ \mu\text{F}$. Calculate the time constants and the cut-off (corner) frequencies of the filters. Calculate the frequencies at which the relative phase shift becomes 90°.

6

Single Stage Amplifiers

6.0 Introduction

Practical single stage amplifiers using tubes and transistors are described in this chapter. We know that a device is made to operate by applying appropriate D.C. voltages at its terminals and by allowing appropriate currents through them. Proper operating points and ranges are chosen from the characteristics of the devices. The transistor or the tube is said to be biased when the chosen currents and voltages are applied at its terminals. Techniques of biasing the devices are discussed in this chapter. The device with the proper biasing network and arrangements to couple the input signals and take the output across loads makes a practical amplifier. These amplifiers have been analysed here and their terminal characteristics have been determined. The discussion is limited to single stage amplifiers which use a single device.

As mentioned earlier, by making one terminal of the transistor common between the output and the input, three amplifier configurations viz CE, CB and CC in case of BJTS and CS, CG and CD in case of FETs are obtained. Since the biasing aims at making the device operate in the proper region it basically is the same for all the three configurations. However, the terminal characteristics of the three configurations differ from each other. In addition to the three different configurations, the amplifiers are divided into different classes called A, B and C depending on the choice of the operating point of the device. This can be best understood by considering a typical transfer characteristics, shown in Fig. 6.1, which gives the output current versus an input parameter that can be a voltage or a current depending upon the device. The input signal changes the voltage or the current parameter on the x-axis of the transfer characteristics and thus produces a change of current at the output. Let us assume that the input parameter is voltage and that its value is less than zero. Hence, as the voltage is reduced the current decreases and finally becomes zero when the device is said to be cut-off.

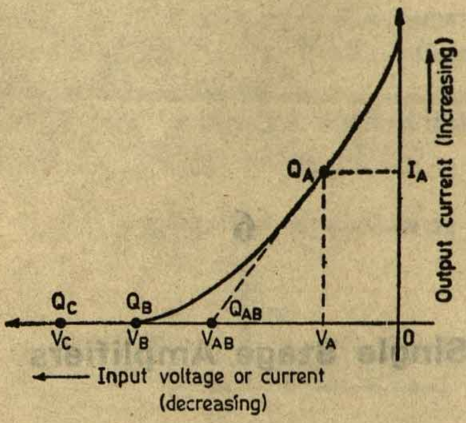


Fig. 6.1 Transfer Characteristic

We shall assume a quiescent operating point Q_A where the input voltage is V_A and the output current is I_A. As the voltage is varied around V_A, the current changes around I_A. As long as the variation of the voltage is small so that the current does not become zero at any time, the operation is linear and such an amplifier is called a class A amplifier. If the operating point is chosen at Q_B then, normally, with no input signal the quiescent current is zero. During the positive swing of the signal the device conducts and output current flows. For the negative excursion, on the other hand, there is no current flow and the device is cut-off. Then, corresponding to a full cycle of the input signal, the output conduction takes place for only half the cycle, as shown in Fig. 6.2. This is known as the class B operation.

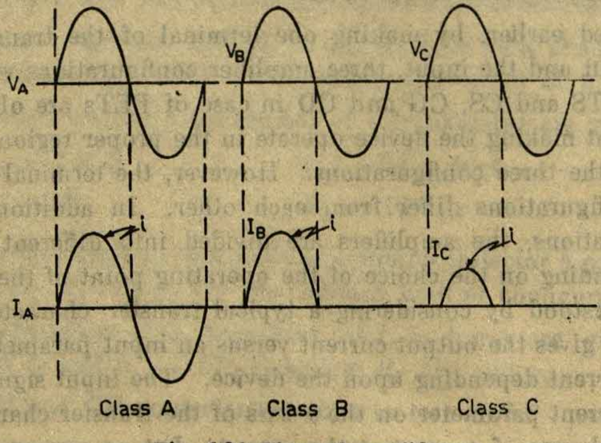


Fig. 6.2 Class of amplifiers

In class C operation the device is biased much to the left of V_B-say at V_C. There is obviously no quiescent operating current and even during the positive excursion, the output current flows only when the input signal amplitude is sufficiently large to cross the point V_B. Thus, the output current flows during less than half the cycle as shown in the figure. It is obvious that only in class A operation the input signal waveform will be directly reproduced at the output. In other classes of operation the output waveform is distorted. The distortion will occur even in class A operation if the transfer curve is not linear throughout the range of the input signal variation. Thus class A small signal amplifiers whose operation is confined to the linear portion of the characteristics are quite common and useful. Class B and class C amplifiers, even though they distort the signals at the first instance, find special applications particularly when large power levels are involved. At large power levels the efficiency of conversion of DC power from the power supply to AC power in the load becomes a primary concern. The total D.C. input power is not available to the load in the shape of signal power because of the dissipation in the device. The efficiency η is defined as

$$\eta = \frac{P_{Load}}{P_{DC}} = \frac{P_{Load}}{P_{Load} + P_D}$$

where P_{Load} = Signal power in the load
$P_{DC} = V_{DC} \cdot I_{DC}$ = Power from the DC supply
P_D = Power dissipation in the device.

We have seen that in class B and C operation, current flows for half or less than half a cycle and thus the average power dissipation would be low thereby increasing the efficiency. It is also desirable in many situations that, in the absence of signal, no current should flow in order to keep the power consumption from the battery low. This is possible in class B and C conditions. The resulting distortion of signal has to be corrected by some other means.

The transfer characteristics are usually non-linear (gradually changing) near the cut-off region. They may be linearized by using an extended cut-off point Q_{AB} as shown in Fig. 6.1. This is known as class AB region and is sometimes preferred over class B region. In this book we shall not be discussing either AB, B or class C amplifiers and our main concern will be class A amplifiers.

6.1 CE Amplifiers

Among the bipolar junction transistors the common emitter amplifier is most commonly used because it provides both voltage and current gains which is larger than unity. We shall first discuss the biasing of this amplifier in the active region in order to obtain class A operation. Its analysis will be taken up later to help determine the voltage and current gains, the input and output impedances and finally the frequency response.

6.1.1 BIASING OF A CE AMPLIFIER

We recall the output characteristics of an *npn* transistor that is shown once again in Fig. 6.3 The operating point is fixed in such a way that the transistor

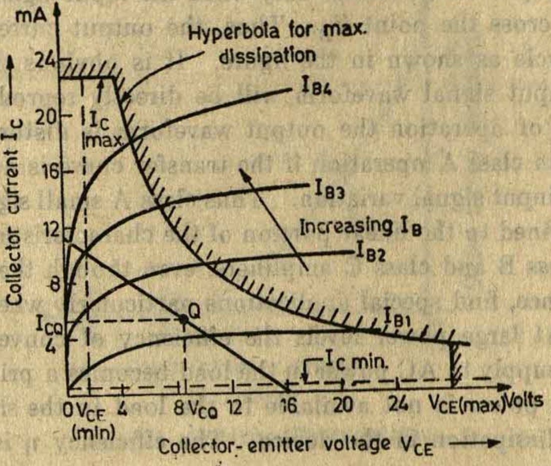


Fig. 6.3 Output characteristics showing biasing of BJT

always operates within the prescribed limits of voltages and currents etc. For example, the manufacturer of the transistor specifies the maximum current $I_{C\,max}$, max voltage V_{CC}, minimum I_C and V_{CE} and maximum collector power dissipation $P_{C\,max}$. The curve for the collector power dissipation is a hyperbola on the $V_{CE} - I_C$ axis as shown in Fig. 6.3. The operating point must never cross this curve. In fact, for most of the class A amplifiers it is kept well below this limit. For a given V_{CC}, an operating point could be chosen as $V_{CE} = \dfrac{V_{CC} - V_{C\,min}}{2}$ and $I_C = \dfrac{I_{C\,max} - I_{C\,min}}{2}$. This choice may not be very desirable and Q may be fixed from other considerations. Once the V_{CE} and I_C have been chosen, the base current I_B is also fixed.

A simple arrangement to obtain the chosen Q point is shown in Fig. 6.4 (a). The circuit uses two power supplies V_{BB} and V_{CC}. Let us see how the desired I_C, V_{CE} and I_B are obtained. For the time being we shall neglect the effect of I_{CO}, the reverse-biased collector saturation current, and the emitter—base diode resistance. The values of β, I_{CO}, $P_{C\,max}$, $I_{C\,max}$ etc. are specified by the manufacturer. Now the collector current I_C is

$$I_C = \beta\, I_B + (1 + \beta)\, I_{CO}$$

and

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \tag{6.1.1}$$

where V_{BE} = base—emitter diode cut-in voltage and is 0.6 to 0.7 volts for Si and 0.2 to 0.3 volts for Ge.

Thus, by controlling either R_B or V_{BB} or both the desired I_B can be set. This fixes up the desired I_C since β is known. Next we consider the collector circuit where

$$V_{CC} = I_C \cdot R_C + V_{CE} \tag{6.1.2}$$

$$V_{CE} = V_{CC} - I_C \cdot R_C \tag{6.1.3}$$

The collector to emitter voltage drop V_{CE} is set by the proper choice of V_{CC} and R_C. Larger V_{CC} gives a greater output swing but the maximum value of V_{CC} is limited to the breakdown voltage of the device. The collector resistance has been shown to be the load resistance across which the output is taken in earlier discussions. It is in fact a biasing resistance because it fixes the V_{CE} but we also take the output across it.

Example 6.1.1

In a transistor biasing circuit, it is desired to have the operating point at $V_{CE} = 6\text{V}$, $I_C = 4$ mA with $V_{BB} = V_{CC} = 15\text{V}$. The β of the *npn*-silicon transistor is given as 80. Calculate the values of R_B and R_C.

$$\text{Since} \quad I_C = 4 \text{ mA}$$

$$\text{we have } I_B = \frac{4}{80} = 0.05 \text{ mA}$$

Let V_{BE} the cut-in voltage of the transistor $= 0.65\text{V}$

$$\text{Hence} \quad R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{15 - 0.65}{0.05} = 287\text{K}\Omega \approx 300\text{K}\Omega$$

$$\text{and} \quad R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{15 - 6}{4} = 2.25 \text{ K}\Omega$$

We have been able to bias the CE amplifier but unfortunately this operating point does not remain stable. The operating point shifts by itself for reasons explained below and sometimes the shift takes the device to the extremes of the operating region and even distroy it . The transistor is a device where the minority carriers, which control the operation, depend very much on the ambient temperature. The cut-in-voltage V_{BE} also depends on the temperature. It decreases at the rate of approximately 2.5 $_m V/°C$ with the increasing temperature. With a decrease in the value of V_{BE}, the effective base-emitter voltage increases and hence I_B also increases. This will in turn increase I_C directly. Similarly the I_{CO} increases with an increase in temperature. In fact, this current doubles approximately for every 10°C rise in temperature. Even though we have neglected this current in the beginning it creates a problem as the temperature increases. I_{CO} is added to I_C and changes the V_{CE} since the drop across R_C is changed. Thus, the variation in temperature changes the operating point.

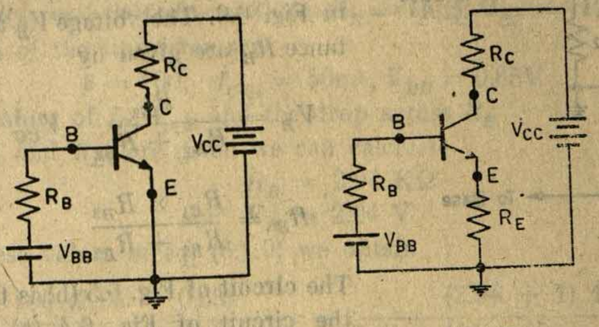
Variation in the value of β is another reason why the operating point stability is not guaranteed. First of all the value of β is temperature dependent and secondly it changes from device to device. All transistors having the same type number do not have the same β. Thus, if one transistor is replaced by another, then the biasing circuit has to be redesigned since the β of the new device will normally be different. The β specified by the manufacturers is a typical value only. The variation may be as large as one to four. The temperature and β variations etc. lead to changes in the operating point and ultimately the power dissipation which may increase. The device temperature will thus be increased affecting the operating point further. If the process becomes regenerative it may destroy the device by excessive heating and is known as thermal runaway.

Typical parameters of an npn silicon transistors are given in Table 6.1 below.

Table 6.1 A Silicon *npn* transistor BC 107

Collector- Emitter voltage. ($V_{BE} = 0$)	V_{CES} max	50 V
Collector- Emitter voltage (open base)	V_{CEO} max	45 V
Collector current (peak value)	I_C max	200 mA
Total power dissipation upto $T_{ambient} = 25°C$		300 mW
Junction temperature T_j	max	175°C
Small signal h_{fe} at $T_j = 25°C$ ($I_C = 0.2$ mA, $V_{CE} = 5$ volts, $f = 1$ KHZ)		$\left\{\begin{matrix} h_{fe} > 125 \\ h_{fe} < 500 \end{matrix}\right\}$
Transition frequency at $I_C = 10$ mA, $V_{CE} = 5V$ (at $f = 35$ MHz)	....	typical 300 MHz
Noise figure at $r_s = 2$ KΩ ($I_C = 200$ µA, $V_{CE} = 5$ V)	....	$\left\{\begin{matrix} \text{typical 1.4 db} \\ - \text{4 db)} \end{matrix}\right\}$
At $T_j = 150°C$, $V_{CB} = 20$ V, $I_E = 0$ $I_{CBO} = (1 + \beta) I_{CO}$	....	15 µA
At $I_C = 2$ mA, $V_{CE} = 5$ volt V_0 is	....	typical 620 µV
At $I_C = 10$ mA, $V_{CE} = 5$ volt, V_{BE} is	......	770 mV
h parameters : (typical values)	$I_C = 2$ mA, $V_{CE} = 5$ Volt $h_{ie} = 2.7$ kΩ $h_{ie} = 1.5 \times 10^{-4}$ $h_{fe} = 220$ $h_{oe} = 30\ \mu ℧$	

To prevent thermal runaway and to keep the operating point largely insensitive to temperature and β variations, it is important to incorporate some corrective measures in the biasing circuit. One such circuit is shown in Fig. 6.4 (b), where a resistance R_E has been inserted in the emitter circuit. Let us see how R_E helps in the stabilization of the operating point. The emitter current I_E flows through R_E and gives rise to a voltage drop V_E. If I_E is large then V_E also is large. We shall assume that the voltage at the base is fixed. Suppose now that due to an increase in the temperature the cut-in voltage V_{BE} decreases and the I_{CO} increases. The net result would be an increase in I_C and hence I_E and a decrease in V_{CE}. However, as the I_C starts increasing, V_E also starts increasing and the difference V_{BE} decreases. This would reduce I_B and hence I_C would be reduced in turn. Thus V_{CE} will be nearer to its previous value. This can be seen quantitatively by calculating I_B for the circuit in Fig. 6.4 (b).



(a) Simple circuit (b) With R_E

Fig. 6.4 Biasing of transistors

$$I_B = \frac{V_{BB} - (V_{BE} + V_E)}{R_B} \tag{6.1.4}$$

Comparing with eq. (6.1.1) we see that the I_B now depends on V_E also. Thus an increase in I_C causes V_E to increase which reduces I_B and keeps I_C at or near its original value. Similar process goes on in the opposite direction when the temperature decreases and the net I_C decreases. As we can see, the V_E would then drop which in turn would increase I_B and finally I_C. Even when β changes due to the temperature or due to a change of the device, the I_C may increase or decrease but the R_E would tend to keep I_C constant. Thus R_E is used to stabilize the operating point.

The schemes of biasing suggested in Figs. 6.4(a) and (b) require two power supplies V_{CC} and V_{BB} of the same polarity. We can dispense with one power supply and obtain the base voltage from the collector power supply itself. One simple method of doing so is shown in Figs. 6.5.

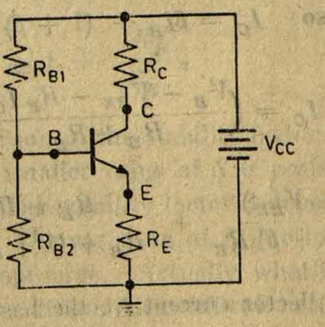


Fig. 6.5 Single supply biasing of transistor.

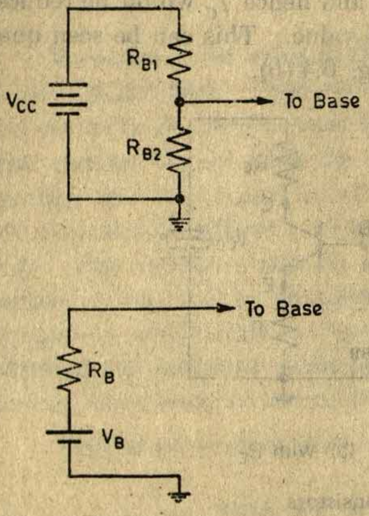


Fig. 6.6 Thévenins equivalent circuit.

The voltage divider R_{B1}, R_{B2} and the supply V_{CC} can be represented by an equivalent circuit using Thevenin's theorem as shown in Fig. 6.6. The voltage V_B and the the resistance R_B are given by

$$V_B = \frac{R_{B2}}{R_{B1} + R_{B2}} \cdot V_{CC} \tag{6.1.5}$$

$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}} \tag{6.1.6}$$

The circuit of Fig. 6.5 (b) is thus reduced to the circuit of Fig. 6.4 (b). The base and collector currents can be calculated by eq. (6.1.4) as

$$I_B = \frac{V_B - V_{BE} - R_E\,(I_B + I_C)}{R_B} \tag{6.1.7}$$

$$\text{Since} \quad V_E = R_E\,(I_B + I_C)$$

Rewriting eq. (6.1.7) by arranging terms we have

$$\left(1 + \frac{R_E}{R_B}\right) I_B = \frac{V_B - V_{BE} - R_E I_C}{R_B}$$

$$\text{or} \quad I_B = \frac{V_B - V_{BE} - R_E I_C}{R_B + R_E} \tag{6.1.8}$$

$$\text{Also} \quad I_C = \beta I_B + (1 + \beta)\, I_{CO}$$

$$\text{or } I_C = \left(\frac{V_B - V_{BE} - R_E I_C}{R_B + R_E}\right) + (1 + \beta)\, I_{CO}$$

$$\text{or } I_C = \frac{(V_B - V_{BE})}{R_B + (1 + \beta)\, R_E} + \frac{R_B + R_E}{R_B + (1 + \beta)\, R_E}\,(1 + \beta)\, I_{CO} \tag{6.1.9}$$

We can now find the collector current I_C, the base current I_B and the collector emitter voltage V_{CE} in terms of the circuit parameters and the manufacturer's data.

Example 6.1.2

An npn transistor is connected as shown in Fig. 6.5. The values of $R_{B1} = 12K\Omega$, $R_{B2} = 3.9K\Omega$ $R_C = 3K\Omega$, $R_E = 1K\Omega$, $V_{CC} = 12$ V.
The parameters of the transistor are

$$\beta = 100, \quad I_{CO}, = 50\text{nA}, V_{BE} = 0.65\text{V}$$

Calculate the values of I_C, V_{CE} and the drop across R_E

Since R_{B1} and R_{B2} are given we can calculate

$$R_B = 2.94 \text{ K}\Omega$$

$$\text{and } V_B = 2.94 \text{ V}$$

substituting these values in eq. (6.1.9) we obtain

$$I_C = \frac{100\ (2.94 - 0.65)}{2.94 \times 10^3 + 101 \times 1 \times 10^3} + \frac{(2.94 + 1)\ 10^3}{2.94 \times 10^3 + 101 \times 1 \times 10^3} \times 101 \times 50 \times 10^{-9}$$

$$= 2.20 \times 10^{-3} + 0.191 \times 10^{-6}$$

$$\text{or } I_C \approx 2.20 \times 10^{-3}$$

$$\text{Hence } V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - 2.2 \times 10^{-3} \times 3 \times 10 \times 10^{+3}$$

$$= 5.4 \text{ volts}$$

$$V_{R_E} \text{ and } = 2.2 \times 10^{-3} \times 1 \times 10^3 = 2.2 \text{ volts.}$$

The variation of I_C due to the changes in I_{CO} is quantitatively denoted by a stability factor S defined as

$$S = \frac{\Delta I_C}{\Delta I_{CO}} \tag{6.1.10}$$

From eqn. (6.1.9) the stability factor S of the circuit in Fig. 6.5 is

$$S = \frac{(1 + \beta)\ (R_B + R_E)}{R_B + (1 + \beta)\ R_E} \tag{6.1.11}$$

If it is assumed that $(1 + \beta)\ R_E >> R_B$, then

$$S \approx 1 + \frac{R_B}{R_E}. \tag{6.1.12}$$

We notice from the definition of the stability factor in eq. (6.1.10) that it is always greater then unity. A smaller value of S is preferred since the variation of I_C will then be minimum. The stability factor S depends to a large extent on R_E, as seen from eq. (6.1.12). The variation of I_C due to a change in I_{CO} can be reduced considerably if R_E is kept large. Actually, what is required is that R_B/R_E ratio should be kept small — a condition that is difficult to satisfy in many situations.

It is now quite simple to design the biasing circuit of the CE amplifier and meet the requirements of a given operating point. The operating point is chosen as discussed earlier. The resistance R_E and equivalent resistance R_B are chosen to meet the stability requirements. Choice of R_E is also governed by the choice of V_{CC} because of the drop $I_E R_E$ across R_E. Finally R_C is calculated by considering the drop V_{CE} required for the operating point.

We can obtain $$R_{B1} = \left[\frac{V_{CC}}{V_B}\right] R_B \qquad (6.1.13)$$

and $$R_{B2} = \frac{R_{B1}}{\left[\frac{V_{CC}}{V_B} - 1\right]} \qquad (6.1.14)$$

Example 6.1.3

In a transistor circuit using *npn* silicon transistor, it is desired to have $I_C = 5$ mA and $V_{CE} = 5$ volts. A stability factor $S = 3.0$ is required. Calculate the values of R_C, R_E, R_{B1} and R_{B2}. Calcuiate the shift in the operating point if the temperature increases by 60°. The relevant parameters of the transistor at the ambient temperature are $\beta = 150$, $V_{BE} = 0.7$V, $I_{CO} = 20$ nA; suggest a suitable value of V_{CC}.

From eq. (6.1.12) we have, for $S = 3$,

$$R_B = 2\ R_E$$

At this stage none of the specifications given can uniquely fix the value of R_E. A trial and error solution is therefore attempted.

Let us assume that $R_E = 1\ \text{K}\Omega$

then $R_B = 2\ \text{K}\Omega$

Fom the eq. (6.1.9)

$$5 \times 10^{-3} = \frac{150\ (V_B - 0.7)}{2\times10^3+150\times10^3} + \frac{3\times10^3}{2\times10^3+151\times10^3} .151\times20\times10^{-9}$$

$$= 0.98\times10^{3}(V_B -- 0.7) + 0.059\times10^{-6}$$

or $V_B = 5.8$ volts

with a $V_{CE} = 5$ volts, we can select $V_{CC} = 15$ volts.

From eq. (6.1.13) and (6.1.14) we can calculate

$$R_{B1} = \frac{15}{5.8} \times 2\times10^3 = 5.17\times10^3 \approx 5.1\text{K}\Omega$$

$$R_{B2} = \frac{5.10\times10^3}{\frac{15}{5.8} - 1} = 3.215\times10^3 = 3.3\text{K}\Omega$$

$$R_C = (15-10.8)/5\times10^{-3} = 0.84\text{K}\Omega$$

The temperature changes by 60°C. Since the I_{CO} doubles for every 10°C change of temperature the I_{CO} will rise to $20 \times 2^6 = 640$ nA Hence

$\Delta I_C = S.\,\Delta I_{CO} = 3 \times 640$ nA $= 1.92$ μA. This is a very small change in I_C. However the V_{BE} decreases as the temperature rises. From eq. (6.1.9) differentiating

$$\Delta I_C = \frac{-\beta}{R_B + (1+\beta) R_E} \Delta V_{BE}$$

$$\text{Now} \quad \Delta V_{BE} = -60 \times 2.5 \text{ mV}$$
$$= -150 \text{ mV}$$

$$\text{hence} \quad I_C = \frac{150 \times 150 \times 10^{-3}}{153 \times 10^3}$$

or $\Delta I_C = 0.147$ mA — a change of about 3%

The drop across R_C is only 4.2 volts. A slightly higher V_{CC}, higher than 15V, may be better.

Example 6.1.4

In the example 6.1.3 above, assume that β may change from 80—240 from one unit to another. Calculate the change of I_C over the whole range.

Since I_{CO} is very small, the effect of I_{CO} can be neglected. From eq. (6.1.9)

$$I_{C1} = \frac{\beta_1 (V_B - V_{BE})}{R_B + (1+\beta_1) R_E}$$

$$\text{or} \quad I_{C1} = 4.92 \text{ mA where } \beta_1 = 80$$

$$I_{C2} = \frac{\beta_2 (V_B - V_{BE})}{R_B + (1+\beta_2) R_E}$$

$$= 5.037 \text{ mA for } \beta_2 = 240.$$

$$\text{Hence } I_{C2} - I_{C1} = (5.03 - 4.92) \text{ mA}$$

$$\text{or} \quad I_{C2} - I_{C1} = 0.117 \text{ mA — a change of only about 2.4\%}$$

In these two examples if we had chosen $R_E = 330\ \Omega$, the values of the resistances and other parameters are

$$R_B = 660\ \Omega$$
$$V_B = 2.383 \text{ V}$$
$$R_{B1} = 4.15 \text{ K}\Omega$$
$$R_{B2} = 0.784 \text{ K}\Omega$$
$$R_C = 1.52 \text{ K}\Omega$$
$$\Delta I_C \Big|_{I_{CO}} = 1.92\ \mu\text{A}$$

$$\Delta I_C \Big|_{V_{BE}} = 0.445 \text{ mA, a change of about } 9\%$$

$$\Delta I_C \Big|_{\beta} = 0.12 \text{ mA, a change of about } 2.4\%$$

The change in I_C due to a change in temperature is much more severe when the value of R_E is smaller. As a matter a choice the R_E should be chosen as the largest value which can be accomodated consistent with the V_{CC} and the drop across R_C. A value of S between 3 to 8 is a good value to start with.

6.1.2 CAPACITIVE COUPLING AND ANALYSIS OF CE AMPLIFIERS

We shall now consider the requirement of how to couple the signal to the amplifier and taken an output from it. The signal to be amplified can be thought of as appearing across two terminals with a d.c. path and having an internal (or output) resistance of r_s and open circuit voltage V_S. When these two terminals are directly connected to the amplifier input terminals, the biasing of the amplifier would be disturbed. A d.c. current would flow through the source and the d.c. potential of the base terminal will change disturbing the operating point. Similarly on the output side, when the usual resistive load, is connected to the collector, a d.c. current would flow through the load changing the d.c. potential of the collector. It is known that d.c. does not flow through either capacitors or transformers. Therefore they are used to couple the source and the load to the amplifier. Transformers are cumbersome and bulky and therefore are avoided for the coupling purposes alone. They are however used in special circumstances where tuned circuits are involved, isolation (balanced output) is required or impedence matching is essential. Capacitive coupling as shown in Fig. 6.7 is quite common. The source V_S is coupled to the input of the amplifier by a capacitor C_1 and the load R_L is connected to the amplifier output by a capacitor C_2. Now at least the d.c. condition are not disturbed. These

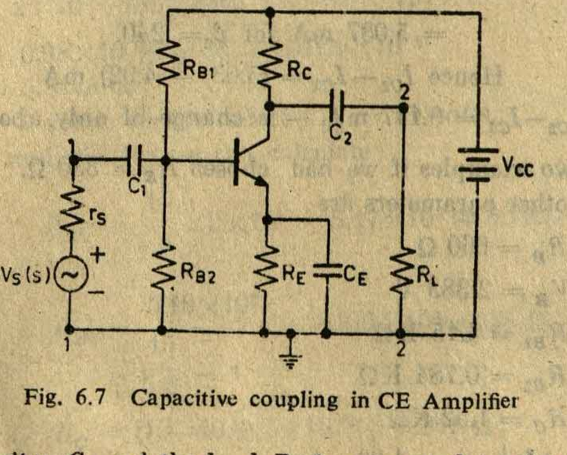


Fig. 6.7 Capacitive coupling in CE Amplifier

capacitors have very large reactances at very low (near zero) frequencies and therefore such d.c. signals, or actually very low frequency signals, will not be amplified by this arrangement because they are not coupled to it. To amplify very low frequency signals both capacitors and transformers are avoided. The biasing is so done that both at the input and the output terminals of the amplifier a zero d.c. voltage is set. This can be done by using positive and negative supplies instead of a single supply. Such a practice is followed in operational amplifiers.

The emitter resistance R_E has been connected to stabilize the biasing but it affects the signal amplification also. Let us see how. When a signal $V_S\ (t)$ is applied at the base terminal, a base current $I_B\ (t)$ would flow. Due to the presence of R_E the $I_B\ (t)$ would be smaller than the value it had when R_E was not connected. Thus $I_C\ (t)$ would be small and the output would be small. Alternatively, we can say that when a signal $V_s\ (t)$ is applied a collector current would flow which would cause a voltage drop $V_E\ (t)$ across R_E. This voltage would oppose the input voltage $V_S\ (t)$ and thus the net voltage appearing between the base and the emitter junction would be small. Assuming the gain to be constant, the output would be small. Thus, the presence of R_E decreases the amplification. Since R_E is used for stabilizing the d.c. current., the a.c. voltage drop across it can be made small or (zero) if the impedance in the emitter path is made small (zero). This can be done by connecting a capacitor C_E in parallel with the resistance R_E as shown in Fig. 6.7. The impedance of the parallel R_E—C_E combination is

$$Z_E\ (s) = \frac{R_E \cdot \dfrac{1}{sC_E}}{R_E + \dfrac{1}{sC_E}} = \frac{R_E}{sR_EC_E+1}$$

$$\text{or} \quad Z_E\ (s) = \frac{\dfrac{1}{sC_E}}{s + \dfrac{1}{R_EC_E}} \tag{6.1.15}$$

The voltage $V_E\ (s)$ across the emitter is given by

$$V_E\ (s) = Z_E\ (s)\ .\ I_E\ (s)$$

$$\text{or} \quad V_E\ (s) = \frac{\dfrac{1}{C_E}}{S + \dfrac{1}{R_EC_E}}\ .\ I_E\ (s) \tag{6.1.16}$$

For d.c., $s = 0$ and the equation (6.1.16) simplifies to $V_E = I_E . R_E$ which is the required bias voltage. For a.c. signal

$$V_E(s) = \frac{\frac{1}{C_E}}{s + \frac{1}{R_E C_E}} \cdot I_E(s), \text{ which would be very small}$$

if C_E is sufficiently large.

Example 6.1.5

In the circuit of Fig. 6.7 it is given that the current $I_E = 5$ mA and $R_B = 1\text{K}\Omega$. Find the value of C_E which will have the effect of a short circuit at 50 Hz.

If we consider short circuit as having a value which is $\frac{1}{100}$th of the previous value, then the reactance of C_E should be $\frac{1}{100}$th of R_E. That is

$$\frac{1}{\omega C_E} \leqslant \frac{1000}{100}\,\Omega$$

$$\text{or} \quad (1/\omega C_E) \leqslant 10\,\Omega$$

$$\text{or} \quad 1/(2\pi \times 50 \times C_E) \leqslant 10\,\Omega$$

$$\text{or} \quad C_E) \geqslant 318\,\mu\text{F}$$

From eq. 6.1.16

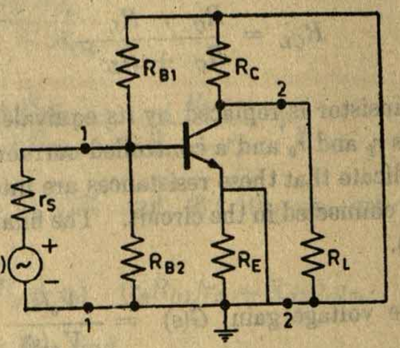
$$V_E(s) = \frac{\frac{1}{318 \times 10^{-6}}}{s + 3.145} \cdot I_E(s)$$

$$= \frac{3.145 \times 10^3}{s + 3.145} \cdot I_B.(s)$$

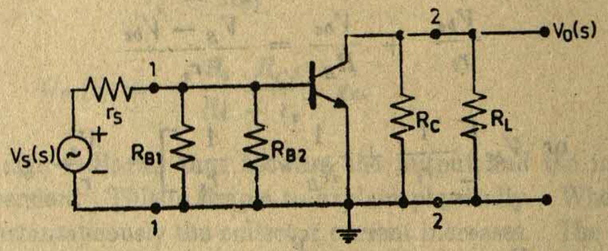
For a.c. signals, the emitter is considered to be grounded and is thus common between the input and output terminals. The coupling capacitors C_1 and C_2 are chosen such that they offer practically no impedance at the signal frequencies of interest. Such an amplifier is commonly known as the *RC* coupled amplifier. Once the amplifier has been biased and an a.c. signal is applied at its input then for analysis purposes we can draw its a.c. equivalent circuit, as shown in Fig. 6.8 The capacitors C_1, C_2 and C_E are assumed to be short circuit at the frequencies of interest. The power supply (or the battery) V_{CC} is assumed to have no internal resistance as far as a.c. signal is concerned and is shorted. Biasing resistances R_{B1} and R_{B2} appear in parallel and are replaced by a single resistance

$$R_B = \frac{R_{B1} \cdot R_{B2}}{R_{B1} + R_{B2}}.$$

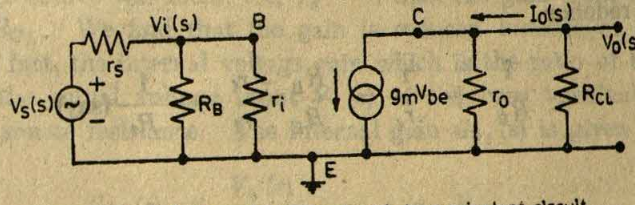
The collector resistance R_C and the load resistance R_L are in parallel and are replaced by a single equivalent resistance



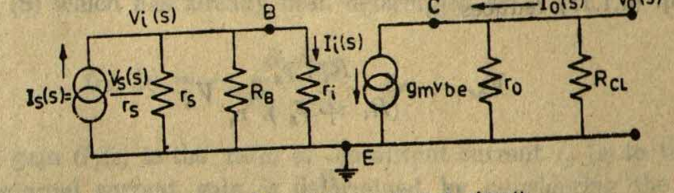
(a) a.c. equivalent



(b) Circuit redrawn



(c) Transistor replaced by equivalent circuit



(d) Complete equivalent circuit

Fig. 6.8 Equivalent circuit of CE amplifier.

$$R_{CL} = \frac{R_C \cdot R_L}{R_C + R_L} .$$

The device i.e. the transistor is replaced by its equivalent circuit in terms of input and output resistances r_i and r_0 and a controlled current source $g_m V_{be}$. The small letters for r_i, r_0, r_s indicate that these resistances are internal equivalent resistances and are not physically connected in the circuit. The final equivalent circuit is shown in Fig. 6.8 (c) and (d).

We now find the voltage gain $G(s) = \frac{V_0(s)}{V_S(s)}$ of the amplifier. First V_{be} is calculated in Fig. 6.8 (c) by applying Kirchoff's current Law (KCL) at the node B,

$$\frac{V_{be}}{r_i} + \frac{V_{be}}{R_B} = \frac{V_S - V_{be}}{r_s}$$

$$\text{or } V_{be}\left[\frac{1}{r_i} + \frac{1}{R_B} + \frac{1}{r_s}\right] = \frac{V_s}{r_s}$$

$$\text{or } V_{be} = \frac{V_s}{r_s\left[\frac{1}{r_s} + \frac{1}{R_B} + \frac{1}{r_s}\right]} \qquad (6.1.17)$$

Now, we can redefine

$$\frac{1}{R_B} + \frac{1}{r_i} = \frac{R_B + r_i}{R_B \cdot r_i} = \frac{1}{R_i} \text{ (say)}$$

Hence

$$\frac{1}{R_B} + \frac{1}{r_i} + \frac{1}{r_s} = \frac{1}{R_i} + \frac{1}{r_s} = \frac{R_i + r_s}{R_i \cdot r_s}$$

Therefore, eq. (6.1.17) reduces to

$$V_{be} = \frac{R_i \cdot r_s}{(R_i + r_s) \cdot r_s} V_S$$

$$\text{or } V_{be} = \frac{R_i}{R_i + r_s} V_S \qquad (6.1.18)$$

It is interesting to note that if the voltage source was ideal, then $r_s = 0$ and $V_{be} = V_S$.

Now $V_o(s) = - g_m \cdot V_{be} \dfrac{r_0 . R_{CL}}{r_0 + R_{CL}}$

or $$V_O(s) = -- g_m \cdot \frac{r_0 R_{CL}}{r_0 + R_{CL}} \times \frac{R_t}{R_t + r_s} V_S \tag{6.1.19}$$

Therefore, combining eqs. (6.1.18) and (6.1.19) we get the voltage gain G_V (S) as

$$G_V(s) = - R_t / (R_t + r_s) \cdot (r_0 R_{CL} / r_0 + R_{CL}) . g_m \tag{6.1.20}$$

Normally the resistance $r_0 \gg R_{CL}$ and

$$\frac{r_0 \cdot R_{CL}}{r_0 + R_{CL}} \approx R_{CL}$$

Then $$G_V(s) = -- \frac{R_t \cdot R_{CL}}{R_t + r_s} \cdot g_m \tag{6.1.21}$$

The negative sign indicates that between the output and the input signals there is a phase inversion. This is simple to explain physically. When the input voltage increases, instantaneously the collector current increases. The drop across R_C and R_{CL} increases, and the output voltage decreases instantaneously indicating a phase difference of 180°.

If the voltage source was ideal, *viz*, $r_s = 0$, then the gain from eq. (6.1.21) is simply $- g_m . R_{CL}$. We find that the gain is reduced because of the source resistance r_s. In fact, the internal voltage gain which is the ratio of the voltage output $V_0(s)$ to the actual voltage input V_t (s) at the base terminal does not depend upon the source resistance. The internal gain G_{Vt} (s) is given by

$$G_{Vt}(s) = \frac{V_0(s)}{V_t(s)} = - g_m . R_{CL} \tag{6.1.22}$$

In contrast to the internal gain, the gain with respect to the source is called the external gain G_{ve} (S) which has already been determined as

$$G_{Ve}(s) = - \frac{R_t R_{CL}}{R_t + r_s} \cdot g_m \tag{6.1.23}$$

The current gain $G_I(s)$ is the ratio of the output current $I_0(s)$ to the input current. The internal current gain is determined by considering the current through r_t alone whereas the external current gain is found by considering the source current $I_S(s)$. The equivalent circuit convenient for this calculation is shown in Fig. 6.8 (d).

Combining r_s and R_B and designating it as $r_s{}'$ we have

$$I_i\ (s) = \frac{V_{be}}{r_i} \tag{6.1.24}$$

and in terms of the source current

$$I_i\,(s) = I_s\,(s) \cdot \frac{r_s{}'}{r_i + r_s{}'} \tag{6.1.25}$$

Let us assume that $r_0 \gg R_{CL}$ hence

$$I_0\,(s) = g_m\, V_{be}$$

Therefore, from eq. (6.1.24) and (6.1.25) we get

$$G_{Ii}\,(s) = \frac{I_0(s)}{I_i\,(s)} = g_m\ r_i \tag{6.1.26}$$

and
$$G_{Ie}\,(s) = \frac{I_0\ (s)}{I_S\,(s)} = \frac{g_m r_i r'_s}{r_i + r'_s} \tag{6.1.27}$$

or
$$G_{Ie}\,(s) = g_m \cdot r_i \,\|\, R_B \,\|\, r_s$$

The input resistance h_{11} of the transistor alone in the CE configuration is r_i and depends on r_e and β. The input resistance of the amplifier as a whole is taken at the terminal (1,1), Fig. 6.8(b) where the source is connected. At this point the input resistance is the parallel combination of the transistor input resistance r_i and the biasing resistance R_B. Thus

$$R_i = \frac{r_i\ R_B}{r_i + R_B} \tag{6.1.28}$$

The output resistance of the transistor alone is r_0 which is usually very high. The output resistance R_0 of the amplifier is taken at the terminal (2.2) Fig. 6.8.(b) where the load is connected. There it is the parallel combination of the output resistance r_0 of the transistor and the collector bias resistance R_C. Therefore the output resistance R_0 is given by

$$R_0 = \frac{r_0 . R_C}{r_0 + R_C} \approxeq R_C \text{ since } r_0 \gg R_C \tag{6.1.29}$$

Example 6.1.6

A CE amplifier using an *npn* transistor of $\beta = 120$ has an $I_C = 5\text{mA}$, the $R_E = R_C = 1\text{K}\Omega$ and $R_B = 2\text{K}\Omega$. This amplifier is being driven by (*i*) a voltage source of $r_s = 600\Omega$ and (ii) a current source of 10 KΩ. Calculate the internal and external voltage and current gains, the input impedance and the output impedance. It is given that $R_L = 600\ \Omega$, and $r_0 = 100\ \mathrm{K}\Omega$

We have $$r_e \approx \frac{25}{I_C(\mathrm{mA})} = 5\ \Omega\ ;\ g_m = \frac{1}{r_e} = 200 \times 10^{-3}\ \mathrm{mhos}$$

Hence $r_i = r_{b'e} \cong (1+\beta)r_e \approx 120 \times 5 = 600\ \Omega$

(i) For the voltage source $r_s = 600\ \Omega$ from eq. (6.1.22)

$$\begin{aligned} G_{Vi}(s) &= -g_m R_{CL} \\ &= -200 \times 10^{-3} . \frac{1 \times 10^3 \times 600}{1600} \\ &= -75 \end{aligned}$$

From eq. (6.1.23), the external voltage gain

$$G_{Ve}(s) = -g_m \frac{R_i \times R_{CL}}{R_i + r_s}$$

now $R_i = 600\ \Omega \parallel 2\mathrm{K}\ \Omega$

$= 461.5\ \Omega \approx 462\ \Omega$

$$\text{hence } G_{Ve}(s) = -200 \times 10^{-3} \frac{0.462 \times 375 \times 10^6}{.462 \times 10^3 + .6 \times 10^3}$$

$$= -32.6$$

From eq. (6.1.26)

$$\begin{aligned} G_{Ii}(s) &= g_m r_i = 200 \times 10^{-3} = .6 \times 10^3 \\ &= 120 \\ G_{Ie}(s) &= g_m\ r_i \parallel R_B \parallel r_s \\ &= 200 \times 10^{-3} \times .26 \times 10^3 \\ &= 52.2 \end{aligned}$$

(ii) For the current source

$$\begin{aligned} r_s &= 10\mathrm{K} \\ G_{Vi}(s) &= -75 \\ R_i &= 0.462\ \mathrm{K}\ \Omega \\ G_{Ve}(s) &= 3.31 \\ G_{Ii}(s) &= 120 \\ G_{Ie}(s) &= 88.32 \end{aligned}$$

The output impedance from eq. (6.1.29) in all cases is $1\ \mathrm{K}\Omega$ since r_0 is very large.

Example 6.1.7

In a transistor CE amplifier, the d.c. collector current is 1mA and $\beta = 100$. $R_C = 5\text{K}\Omega$, $R_B = 4\text{K}\Omega$ and $R_L = 600\ \Omega$. The source resistance $r_s = 50\ \Omega$. Calculate the external voltage gain and the input impedance.

Since $I_C = 1\text{mA}$

$r_e = 25\ \Omega$

$g_m = 40 \times 10^{-3}$

and $r_e = r_i = 2500\ \Omega$

hence $R_i = 2.5\text{K} \parallel 4\text{K}\Omega$

$R_i = 1.54\text{K}\Omega$

The external voltage gain

$$G_{Ve}(s) = -g_m \frac{R_i R_{CL}}{R_i + r_s}$$

$$= -40 \times 10^{-3} \cdot \frac{1.54 \times .536}{1.54 + .05}$$

$$= -20.8$$

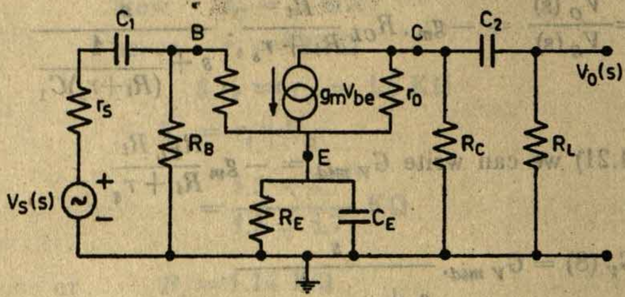
6.2 Frequency Response of CE Amplifier

It has been explained in the previous chapter that the frequency response, that is the variation of the gain and phase with frequency, of the amplifiers is divided in 3 regions for convenience -- low frequency, mid frequency and high frequency. In the mid-frequency range neither the series nor the shunt capacitors are effective, that is, the series capacitors offer practically no impedence and the shunt capacitors offer very large impedance. When the series capacitors are ineffective in the mid-frequency range, they are obviously ineffective in the high frequency range. Similarly the shunt capacitors offer even higher impedance at the lower frequencies compared to the mid-frequency range and are, therefore, not considered in the lower frequency region. The emitter bypass capacitor C_E is a special shunt capacitor across R_E and is used to remove the feedback effect at the emitter at the lowest possible frequencies. The mid-frequency analysis is what has already been done in the previous subsection. The gains and the impedances are constant throughout the mid-band. We shall next consider the behaviour of the amplifier at low and high frequencies seperately.

6.2.1 Low Frequency Response

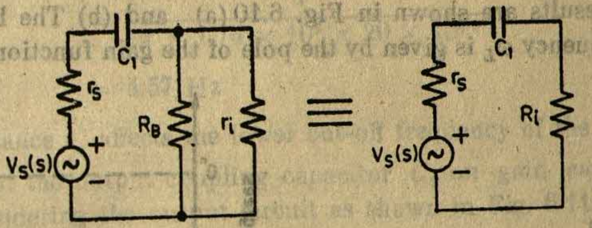
First of all the low frequency region will be considered where the series capacitors C_1, C_2 and the bypass capacitor C_E as shown in Fig. 6.7, are taken into consideration. A general method of analysing the frequency charateristic at low frequencies would be to work out the transfer function of the complete amplifier with all the three capacitors together. This approach would be very tedious.

A simpler approach is followed here by considering the effect of each capacitor individually. The overall equivalent circuit at low frequencies is shown in Fig. 6.9 (a). It is assumed to start with that C_E is very large and R_E is virtually short circuited. The emitter is at ground potential in this case



(a) Complete equivalent circuit

The input coupling capacitor C_1 is considered first. The equivalent circuit of the input side is shown in Fig. 6.9 (b).



(b) Input circuit only

Fig. 6.9 Low Frequency Equivalent Circuit of the CE Amplifier

The voltage $V_i(s)$ is given by

$$V_{be}(s) = V_i(s) = \frac{V_S(s) \times R_i}{r_s + R_i + \dfrac{1}{sC_1}}$$

$$\text{or} \quad V_{be}(s) = \frac{sC_1 \, R_i}{sC_1 (r_s + R_i) + 1} V_S(s) \tag{6.2.1}$$

where $r_i \parallel R_B = R_i$

the output of the amplifier $V_O(s)$ is, thus,

$$V_O(s) = -g_m \cdot V_{be}(s) \cdot R_{CL}$$

$$= -g_m.R_{CL}\frac{sC_1 . R_i}{sC_1(R_i+r_s)+1} . V_S(s) \tag{6.2.2}$$

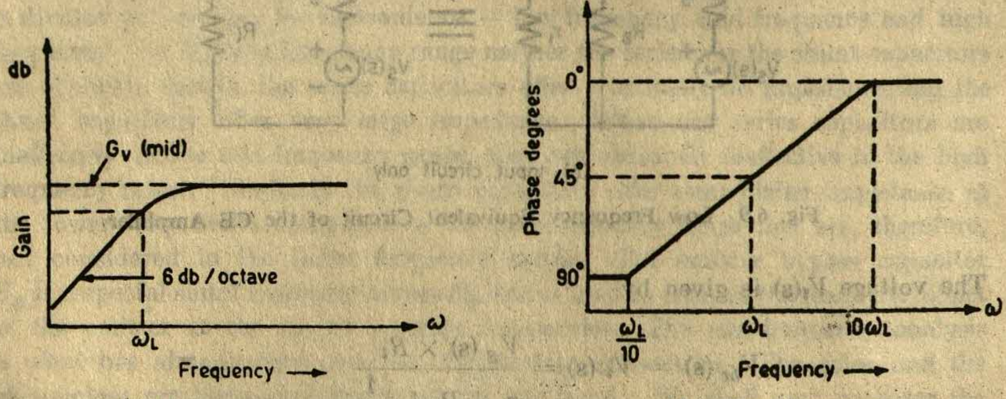
Rewriting eq. (6.2.2) as $G_V(s)$, we have

$$G_V(s) = \frac{V_O(s)}{V_S(s)} = -g_m . R_{CL}\frac{R_i}{R_i+r_s} . \frac{s}{s+\frac{1}{(R_i+r_s)C_1}} \tag{6.2.3}$$

From eq. (6.1.21) we can write $G_{V\,mid} = -g_m\frac{R_{CL}R_i}{R_i+r_s}$

$$\text{and } G_V(S) = G_{V\,mid} . \frac{s}{s+\frac{1}{(R_i+r_s)C_1}} \tag{6.2.4}$$

It is thus seen that the gain at low frequencies is a function of frequency. The input equivalent circuit in Fig 6.9 (b) is similar to the high pass filter discussed in 5.5. and the gain G_V (s) in eq. (6.2.4) has the same form as eq. 5.5.6. The variation of gain and phase versus frequency is plotted by taking $s = jw$ in eq. (6.24). The results are shown in Fig. 6.10 (a) and (b) The break point or the lower 3dB frequency ω_L is given by the pole of the gain function as



(a) Frequency response (b) Phase .frequency

Fig. 6.10 Low frequency response due to input coupling capacitor

$$\omega_L = \frac{1}{(R_i+r_s)C_1}$$

$$\text{or} \quad f_L = \frac{1}{2\pi(R_i+r_s)C_1} \tag{6.2.5}$$

Example 6.2.1

In an *RC* coupled *CE* amplifier, the coupling capacitor C_1 is 20 μf. Find the value of lower 3dB frequency if $I_C = 2\text{mA}$, $R_B = 4.7\text{K}\Omega$, $\beta = 120$ and $r_s = 600\ \Omega$

$$\text{Now} \quad I_C = 2\ \text{mA}$$

$$\text{hence} \quad r_e = 12.5\ \Omega$$

$$\beta\, r_e \approx r_i = 1.5\ \text{K}\Omega$$

$$R_i = r_i \| R_B$$

$$= \frac{1.5 \times 4.7}{1.5 + 4.7}\ \text{K}\Omega$$

$$\text{or} \quad R_i = 1.14\ \text{K}\Omega$$

From eq. (6.2.5) we have

$$f_L = \frac{1}{2\pi (R_i + r_s)\, C_1}$$

$$= \frac{1}{2\pi \times 1.74 \times 10^3 \times 20 \times 10^{-6}}$$

$$= 4.57\ \text{Hz}$$

The source resistance r_s affects the lower cut-off frequency of the amplifier.

The effect of the output coupling capacitor C_2 on gain can similarly be analysed by considering the output circuit as shown in Fig. 6.11. In a manner very similar to the one followed in deriving eq. (6.2.1), we will have the output voltage V_O (s) as

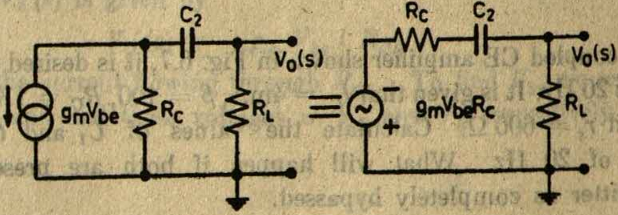


Fig. 6.11 Output coupling capacitor

$$V_O\,(\text{s}) = -\,g_m\, V_{be} \,.\, R_C \,.\, \frac{sC_2\, R_L}{sC_2\,(R_C + R_L) + 1} \tag{6.2.6}$$

Rewriting eq. 6.2.6) we will have

$$V_O(s) = -g_m \cdot V_{be} R_{CL} \frac{s}{s + \dfrac{1}{(R_C + R_L)\, C_2}} \qquad (6.2.7)$$

where $R_{CL} = R_C || R_L$

substituting V_{be} in terms of V_S (s) from eq. (6.1.18) in the eq. (6.2.7) we will get

$$V_O(s) = -g_m R_{CL} \cdot \frac{s}{s + \dfrac{1}{(R_C + R_L)\, C_2}} \; \frac{R_i}{R_i + r_s} \cdot V_S(s)$$

The gain G_V (s) is, thus,

$$G_V(s) = -G_{V\,mid} \cdot \frac{s}{s + \dfrac{1}{(R_i + R_L)\, C_2}} \qquad (6.2.8)$$

Thus, the output coupling capacitor affects the gain in a manner similar to that of the input coupling capacitor and the frequency response is as shown in Fig. 6.10. The lower cut-off frequency due to the output coupling capacitor C_2 is

$$f_L = \frac{1}{2\pi\, (R_C + R_L)\, C_2} \qquad (6.2.9)$$

Truly speaking both these capacitors should be considered together and then the frequency response should be analysed. The expression for the gain becomes a little cumbersome and the effect of individual poles would not be seen seperately particularly because the poles are close to each other and interact.

Example 6.2.2

In an RC coupled CE amplifier shown in Fig. 6.7, it is desired that the lower 3db frequency is 20 Hz. It is given that $I_C = 4\text{mA}$, $\beta = 100$, $R_C = 1\text{K}\Omega$, $R_B = 5\text{k}\Omega$, $R_L = 600\ \Omega$ and $r_s = 600\ \Omega$. Calculate the values of C_1 and C_2 individually to give an f_L of 20 Hz. What will happen if both are present together ? Assume the emitter as completely bypassed.

Now $r_e = 6.25\ \Omega$

$r_i \approxeq \beta\, r_e = 625\ \Omega$

$R_i = R_B || r_i = 0.55\text{K}\Omega$

$R_{CL} = R_C || R_L = 0.375\text{K}\Omega$

For f_L of 20 Hz. ar the input circuit we have from eq. (6.2.5)

$$20 = \frac{1}{2\pi\, (.55 + 0.6) \times C_1 \times 10^3}$$

or $C_1 = 6.9\ \mu f$

similarly for a f_L of 20 Hz at the output circuit, we have from eq. (6.2.9)

$$20 = \frac{1}{2\pi\,(1 + 0.6) \times C_2 \times 10^3}$$

or $C_2 = 5\,\mu f$

Now if these values of C_1 and C_2 are used in the circuit then there will be an interaction and the actual lower 3db frequency will be higher. If two circuits have the same f_{L1}, the actual f_L of the overall amplifier can be shown to be $f_{L1}/0.64$. In other words if the f_L values are designed to be about 13Hz for both the circuits individually, then the overall 3db frequency will be 20 Hz.

Another commonly used technique is to stagger the lower 3db frequencies of the input and the output circuits. Thus, when C_1 is doubled, the response due to C_1 will be 3db down at 10Hz instead of the 20 Hz. The overall low frequency response will then be governed by C_2. We could have changed C_2 instead of C_1 as well.

6.2.2 EFFECT OF THE EMITTER BYPASS

The effect of the emitter bypass capacitor is taken up next and C_1 and C_2 are assumed to be a short circuit. The corresponding equivalent circuit is shown in Fig. 6.12. The emitter now is not really common between the input and the output terminals. Let us find the gain $V_O(s) / V_s(s)$ of the circuit in Fig. 6.12 in terms of the emitter impedance Z_E which is the parallel combination of R_E and C_E. There are 3 nodes B, E, and C in the circuit besides the ground node. The output voltage $V_0(s)$ is given by

$$V_O(s) = -g_m V_{be} / R_{CL}$$

since $g_m V_{be}$ is the current flowing through R_{CL}. To find V_{be} we use KCL at the nodes B and E and call these voltages as V_B and V_E respectively.

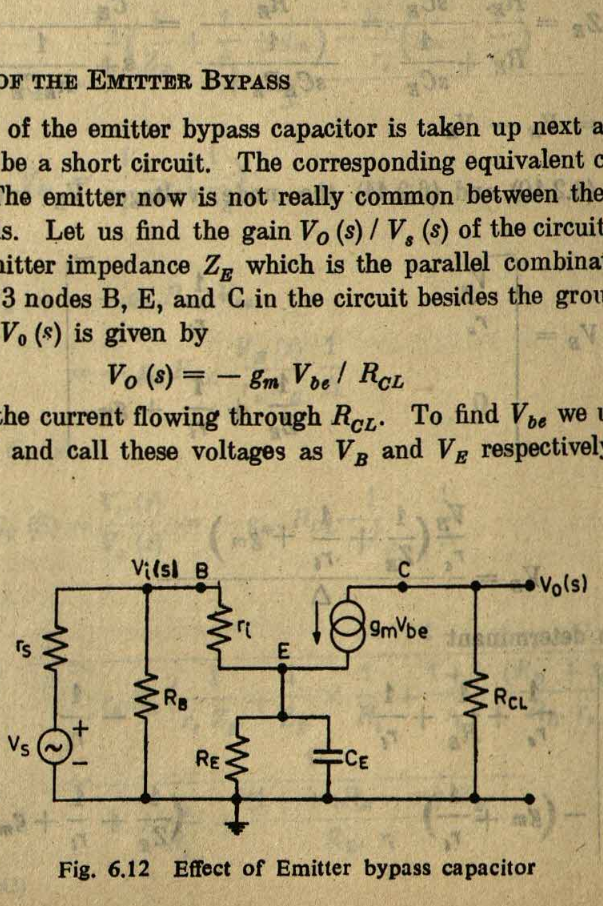


Fig. 6.12 Effect of Emitter bypass capacitor

At node B,

$$\frac{V_B - V_S}{r_s} + \frac{V_B}{R_B} + \frac{V_B - V_E}{r_i} = 0$$

or, $$\left(\frac{1}{r_s} + \frac{1}{R_B} + \frac{1}{r_i}\right) V_B - \frac{1}{r_i} V_E = \frac{V_S}{r_s} \qquad (6.2.10)$$

At node C,

$$\frac{V_E - V_B}{r_i} + \frac{V_E}{Z_E} - g_m (V_B - V_E) = 0$$

or, $$-\left(g_m + \frac{1}{r_i}\right) V_B + \left(\frac{1}{Z_E} + \frac{1}{r_i} + g_m\right) V_E = 0 \qquad (6.2.11)$$

where $$Z_E = \frac{R_E \cdot \frac{1}{sC_E}}{R_E + \frac{1}{sC_E}} = \frac{R_E}{\frac{1}{sC_E R_E + 1}} = \frac{\frac{1}{C_E}}{s + \frac{1}{R_E C_E}}$$

and $V_{be} = V_B - V_E$

From equations (6.2.10) and (6.2.11) the node voltages V_B and V_E can be computed as

$$V_B = \begin{bmatrix} \frac{V_s}{r_s} & -\frac{1}{r_i} \\ 0 & \frac{1}{Z_E} + \frac{1}{r_i} + g_m \end{bmatrix} \Delta$$

or $$V_B = \frac{\frac{V_S}{r_s}\left(\frac{1}{Z_E} + \frac{1}{r_i} + g_m\right)}{\Delta}$$

where Δ is the determinant

$$\Delta = \begin{vmatrix} \frac{1}{r_s} + \frac{1}{R_B} + \frac{1}{r_i} & -\frac{1}{r_i} \\ -\left(g_m + \frac{1}{r_i}\right) & \left(\frac{1}{Z_E} + \frac{1}{r_i} + g_m\right) \end{vmatrix}$$

or
$$\Delta = \left(\frac{1}{r_s} + \frac{1}{R_B} + \frac{1}{r_i}\right)\left(\frac{1}{Z_E} + \frac{1}{r_i} + g_m\right) - \frac{1}{r_i}\left(g_m + \frac{1}{r_i}\right)$$

Rearranging terms and writing $R_i = R_B \parallel r_i$ we have

$$\Delta = \frac{1}{r_s Z_E} + \frac{1}{Z_E} \cdot \frac{1}{R_i} + \frac{(1+\beta)}{r_i} \times \frac{(R_B + r_s)}{R_B \, . \, r_s}$$

Now, the voltage V_E is given by

$$V_E = \frac{\begin{vmatrix} \left(\frac{1}{r_s} + \frac{1}{R_B} + \frac{1}{r_i}\right) & \frac{V_s}{r_s} \\ -\left(g_m + \frac{1}{r_i}\right) & 0 \end{vmatrix}}{\Delta} = \frac{\frac{V_s}{r_s}\left(g_m + \frac{1}{r_i}\right)}{\Delta}$$

Then
$$V_{be} = (V_B - V_E) = \frac{\frac{V_s}{r_s}\left(\frac{1}{Z_E} + \frac{1}{r_i} + g_m\right) - \frac{V_S}{r_s}\left(g_m + \frac{1}{r_i}\right)}{\Delta}$$

or
$$V_{be} = \frac{V_S}{r_s . \Delta} . \left(\frac{1}{Z_E}\right) \tag{6.2.12}$$

Therefore,
$$V_0\,(s) = - g_m . R_{CL} . V_{be}$$
$$= - g_m . R_{CL} . \frac{V_S\,(s)}{r_s . Z_E} \frac{1}{\Delta}$$

The voltage gain $G_V\,(s)$.

$$G_V\,(\mathrm{S}) = \frac{V_0\,(s)}{V_s\,(s)} = - g_m . R_{CL} \frac{1}{r_s Z_E} . \frac{1}{\Delta} \tag{6.2.13}$$

Now
$$\frac{1}{r_s . \ Z_E} . \frac{1}{\Delta} = \frac{1}{r_s Z_E\left(\frac{1}{r_s Z_E} + \frac{1}{Z_E} \times \frac{1}{R_i} + \frac{1+\beta}{r_i} . \frac{(R_B + r_s)}{R_B . \, r_s}\right)}$$

$$= \frac{1}{1 + \frac{r_s}{R_i} + \frac{(1+\beta)\ (R_B + r_s)\ Z_E}{R_B . \ r_i}}$$

$$= \frac{R_i}{R_i + r_s + R_i \times \dfrac{(R_B + r_s)}{R_B \cdot r_i}(1+\beta) Z_E}$$

$$= \frac{R_i}{R_i + r_s + \dfrac{R_B + r_s}{R_B + r_i}(1+\beta) Z_E}$$

because $R_i = \dfrac{R_B \cdot r_i}{R_B + r_i}$ and therefore

$$R_i \times \frac{R_B + r_s}{R_B \cdot r_i} = \frac{R_B \cdot r_i}{R_B + r_i} \times \frac{R_B + r_s}{R_B \cdot r_i} = \frac{R_B + r_s}{R_B + r_i}$$

The voltage gain G_V (s) now becomes

$$G_V(s) = -g_m \cdot R_{CL} \cdot \frac{R_i}{R_i + r_s + \dfrac{R_B + r_s}{R_B + r_i}(1+\beta) \cdot Z_E} \qquad (6.2.14)$$

We now have an interesting and general expression for the voltage gain of the CE amplifier with an emitter impedance. This expression will be of great use in feedback amplifiers and a similar analysis will be used for emitter followers. For example, if there was no emitter resistance and thus obviously no capacitor, then $Z_E = 0$ and the voltage gain from eq. (6.2.14) becomes

$$G_V(s) = -g_m R_{CL} \frac{R_i}{R_i + r_s}$$

which is the same as eqn. (6.1.21) derived for a CE amplifier. In many situations it is necessary to connect a small resistance in the emitter which is not by-passed. The situation can be illustrated as in Fig. 6.13 where R_{E1} is the unbypassed and R_{E2} is the bypassed resistance. For mid frequency ranges R_{E2} is assumed to be completely bypassed or shorted and the emitter impedance $Z_E = R_{E1}$. The voltage gain in this condition becomes, from eq. (6.2.14),

$$G_V(s) = -g_m R_{CL} \left(\frac{R_i}{R_i + r_s + \dfrac{R_B + r_s}{R_B + r_i}(1+\beta) R_{E1}} \right) \qquad (6.2.15)$$

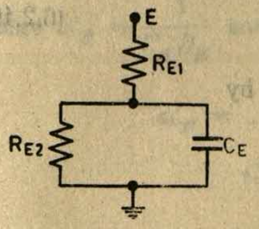


Fig. 6.13 Partially bypassed emitter resistance

We find that the unbypassed resistance R_{E1} reduces the voltage gain. This, as was explained earlier, happens when the R_E is wholly or partially unbypassed. To compensate for this loss in gain the capacitor C_E is required to produce a short circuit across R_E at the frequencies of interest.

Example 6.2.3

A transistor amplifier has $R_E = 2\text{K}\ \Omega$ $R_B = 4.7\text{K}\ \Omega$ and $R_C = 3\text{K}\ \Omega$ and $R_L = 600\ \Omega$. The transistor parameters are $r_i = 1.5\text{K}\ \Omega$, $\beta = 120$ and $r_s = 100\text{k}\ \Omega$. A part of the emitter resistance R_{E1} is left unbypassed. Calculate the value of R_{E1} required to obtain a gain G_{ve} (s) of -10 if $r_s = 600\ \Omega$. What is the gain if whole of R_E is bypassed.

We have $R_i = 1.14\text{K}\ \Omega$ and from eq. (6.2.15)

$$-10 = -.08 \times .5 \times 10^3 \left(\frac{1.14 \times 10^3}{1.14 \times 10^3 + 0.6 \times 10^3 + \left(\frac{4.7 + 0.6}{4.7 + 1.5}\right) \times 121\, R_{E1}} \right)$$

$$10^3\,(1.74 + 0.103\, R_{E1}) = 45.6 \times 10^3$$

$$\text{or} \quad R_{E1} = 425.8\ \Omega$$

Hence let $R_{E1} = 425\ \Omega$ and $R_{E2} = 2000 - 425 = 1575\ \Omega$.

If R_{E2} is also bypassed, the gain from (6.2.15) is ($R_{E1} = 0$)

$$G_V\,(s) = -\, g_m \frac{R_{CL}\, R_i}{R_i + r_s}$$

$$= -\ .08 \times \frac{0.5 \times 1.14}{1.14 + 0.6} \times 10^3$$

$$\text{or } G_V\,(S) = -\ 26.2$$

Let us now go back to finding the effects of C_E or low frequency response of the amplifier, the purpose for which the generalized gain expression has been derived. Since our interest now is on frequency response, we simplify the expression by suitable approximations and assumptions.

Let $\dfrac{R_B + r_s}{R_B + r_i} = \text{K}$, some constant factor

In many practical situations $R_B \gg r_s$ or r_i and so $\text{K} \approx 1$.

$$\frac{R_B + r_s}{R_B + r_i}(1 + \beta)\, Z_E \simeq \mathrm{K}\,\beta\, Z_E \tag{6.2.16}$$

because $(1 + \beta) \approx \beta$ for large β. We now replace Z_E by

$\dfrac{\dfrac{1}{C_E}}{s + \dfrac{1}{R_E\, C_E}}$ in the gain expression of eq. (6.2.14)

$$G_V\,(\mathrm{s}) = -\, g_m R_{CL} \frac{R_i}{R_i + r_s + \mathrm{K}.\,\beta.\, \dfrac{1}{C_E}\left(1/\mathrm{s} + \dfrac{1}{C_B R_E}\right)}$$

$$\text{or } G_V\,(\mathrm{s}) = -\, g_m\, R_{CL}\cdot \frac{R_i}{R_i + r_s} \; \frac{1}{1 + \dfrac{\mathrm{K}.\,\beta}{C_E\,(R_i + r_s)\left(s + \dfrac{1}{R_E C_E}\right)}}$$

$$= G_V\,(\mathrm{mid}).\left[\frac{s + \dfrac{1}{R_E C_B}}{s + \dfrac{1}{R_E C_E} + \dfrac{\mathrm{K}\;\beta}{C_E\,(R_i + r_s)}}\right]$$

$$= G_V\,(\mathrm{mid}).\left[\frac{s + \dfrac{1}{R_E\, C_E}}{s + \dfrac{1}{C_E}\left(\dfrac{(R_i + r_s + \mathrm{K}.\,\beta\, R_E}{R_E\,(R_i + r_s)}\right)}\right]$$

$$= G_V\,(\mathrm{mid}).\left[\frac{s + \left(\dfrac{1}{R_E\, C_E}\right)}{s + \left(\dfrac{1}{R_E C_E\cdot \dfrac{(R_i + r_s)}{R_i + r_s + K.\beta.R_E}}\right)}\right] \tag{6.2.17}$$

so the gain of eq. (6.2.17) has the form of

$$G_V\,(\mathrm{s}) = G_V\,(\mathrm{mid})\,\frac{s + \omega_E}{s + \omega'_E} \tag{6.2.18}$$

where $\omega'_E = \dfrac{1}{C_E R_E}$ and

$$\omega'_E = \frac{1}{C_E R_E \left[\dfrac{(R_i + r_s)}{R_i + r_s + K.\beta R_E} \right]}$$

ω'_E is the pole and ω_E is the zero and $\omega'_E > \omega_E$. The response for such a gain function would be as shown in Fig. 6.14. We see that as the frequency is decreased from the midband value the gain starts decreasing. It decreases by 3 dB at $\omega = \omega'_E$. When $\omega_E \ll \omega'_E$ the pole and the zero do not interact. At $\omega < \omega_E$, the frequency response becomes flat once again. If we neglect ω_E then the gain function at low frequencies is similar to that due to the coupling capacitor. The lower 3 dB frequency due to the emitter bypass capacitor C_E, assuming ω_E to be much smaller, is given by

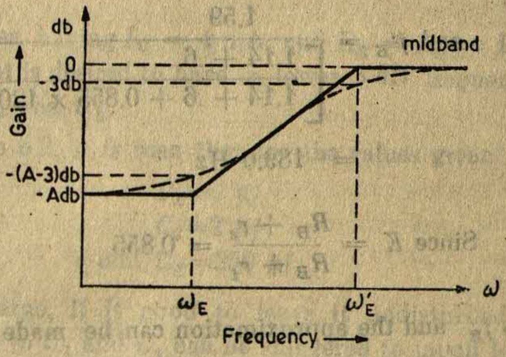


Fig. 6.14 Frequency response due to emitter bypass capacitor

$$f_L = \frac{1}{2\pi C_E R_E \left(\dfrac{R_i + r_s}{R_i + r_s + K\beta R_E} \right)} \tag{6.2.19}$$

$$\text{where } K = \frac{R_B + r_s}{R_B + r_i}$$

Example 6.2.4

The transistor amplifier of Fig. 6.7 has I_C=2m A, R_E= 2KΩ, R_B = 4.7KΩ, R_C = 3KΩ, R_L = 600 Ω, r_s = 600 Ω. The transistor β = 120. A capacitor of $50U\mu f$ is connected across R_E. Calculate the value of ω_E and ω'_E.

$$r_e = 12.5\,\Omega$$
$$R_i = R_B \parallel r_i = 1.4\ \text{K}\Omega$$
$$R_{CL} = R_C \parallel R_L = 0.5\text{K}\Omega$$

The frequencies ω_E and ω'_E are calculated from eq. (6.2.17) as

$$\omega'_E = \frac{1}{R_E\ C_E}$$

$$\text{and} \quad \omega'_E = \frac{1}{C_E R_E \left[\dfrac{R_i + r_s}{R_i + R_s + K\beta R_E}\right]}$$

Thus

$$f_E = \frac{1}{2\pi \times 2 \times 10^3 \times 50 \times 10^{-6}} = 1.59\ \text{Hz}$$

$$\text{and } f'_E = \frac{1.59}{\left[\dfrac{1.14 + .6}{1.14 + .6 + 0.855 \times 120 \times 2}\right]}$$

$$= 189.0\ \text{Hz}$$

$$\text{Since } K = \frac{R_B + r_s}{R_B + r_i} = 0.855$$

We find that $f'_E \gg f_E$ and the approximation can be made that $f_L = 189$ Hz.

The effect of the three capacitors on the low frequency response of the amplifier has been analysed and lower 3dB cut-off frequencies calculated considering the effect of the capacitors seperately and individually. They are summarised in Table 6.2. Values of capacitors required to get the lower 3B cut off frequency f_L at say 50 Hz individually, are also given in the table assuming practical resistance values in the amplifier. Computing the overall frequency response due to all the 3 capacitors taken together would again be very cumbersome. It is seen from the table that in order to get a desired lower 3dB frequency, the emitter bypass capacitor C_E is required to be very large. Thus C_E primarily governs the low frequency response. A proper C_E is chosen to give the desired low frequency response, and then C_1 and C_2 are chosen to be much larger (say 10 times or more) than the values which would give the desired f_L individually. Since C_1 and C_2 are much larger, their 3dB frequencies are much smaller than that due to the C_E and thus do not affect the low frequency response.

Table 6.2 Lower 3 dB cut-off frequencies

[Typical Circuit Values : $R_B = 4.0$ KΩ, $R_E = 1$ KΩ, $I_C = 4$ mA, $R_L = r_s = 600$ Ω, $R_C = 1$ K Ω, $\beta = 80$]

Due to	f_L	C for $f_L = 50$ Hz
1. Input coupling capacitor	$\frac{1}{2\pi (R_i + r_s)\, C_1}$	6 μf
2. Output coupling capacitor	$\frac{1}{2\pi (R_C + R_L)\, C_2}$	2 μf
3. Emitter bypass capacitor	$\frac{1}{2\pi C_E R_E \left(\frac{R_i + r_s}{R_i + r_s + K,\beta . R_E}\right)}$	250 μf
with	$K = \frac{R_B + r_s}{R_B + r_i}$	

Example 6.2.5

For an amplifier having $I_C = 4$ mA and $R_E = R_C = 1$ KΩ, $r_s = R_L = 600$ Ω, $R_B = 4$ KΩ, it is desired to have a lower 3 dB frequency of 50 Hz. Fix the values of C_1, C_2 and C_E.

From the table 6.2, it is seen that for the values given

$$C_1 = 6\ \mu f$$
$$C_2 = 2\ \mu f$$
$$\text{and } C_E = 250\ \mu f$$

Since C_E is quite large, it is good to leave it undisturbed. The lower 3 dB frequency points due to C_1 and C_2 can be staggered to much lower values so that they do not have any appreciable impedance at 50 Hz. For example if $C_1 = 60\ \mu f$ and $C_2 = 20\ \mu f$ then their lower 3dB frequencies will be at 5 Hz and the amplifier as a whole will have a lower 3 dB frequency of 50 Hz, governed solely by C_E.

6.2.3 HIGH FREQUENCY RESPONSE

We shall now discuss the behaviour of the amplifier at high frequencies. The coupling and the bypass capacitors are virtually short circuit at high frequencies and their reactances become negligibly small. The capacitors which come into play at high frequencies are those which appear in shunt between the input and the ground and the output and the ground terminals, effectively making it a low pass filter circuit as shown in Fig. 6.15. Usually no external shunt capacitors are connected deliberately unless the high frequencies are required to be removed. These shunt capacitors are either present inside the device or they

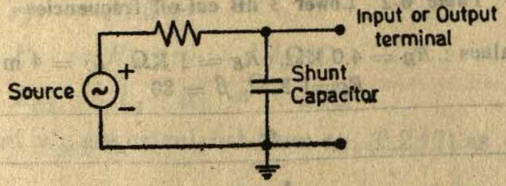


Fig. 6.15 Low Pass filter due to shunt capacitors

are caused by the input and output capacitances of the circuits and system including the stray capacitance, to which the amplifier is connected.

In the bipolar junction transistor the uncovered charges of the depletion layer constitute a junction capacitance known as the Transition capacitance. Since the width of the depletion layer depends on the applied voltage, the transition capacitances varies with the voltage. For a reverse biased junction, the transition capacitance decreases as the reverse voltage is increased because the width of the transition region increases. The width of the depletion layer decreases as the voltage is increased in a forward biased junction and therefore the transition capacitance would increase with applied forward voltage. The forward biased junction has a Diffusion capacitance in addition to the transition capacitance. The diffusion capacitance is due to the excess carriers injected in the junction when it is forward biased. In a forward biased junction holes from p side are injected into the n-region where they become minority carriers. Similarly the electrons injected from the n-region become minority carrier in the p-region. The densities of these excess minority carriers on the two sides are maximum near the junction and decrease gradually away from it. This storage of charge gives rise to the diffusion capacitance which is many times larger than the transition capacitances. The total capacitance appearing across a forward biased junction is the sum of the diffusion and the transition capacitances. No diffusion capacitance exists for a reverse biased junction. The diffusion capacitance is proportional to the forward current. The order of diffusion capacitance ranges from 5*nf* to .05 *nf* whereas the transition capacitance is of the order of 3-8 *pf* for the silicon planar transistors.

In a transistor the diffusion capacitance appears across the forward biased emitter-base junction and the transition capacitance appears across the reverse biased collector-base junction. The equivalent circuit of a transistor discussed earlier in section 5 is modified to include the capacitances and is drawn in Fig. 6.16. This equivalent circuit is known as the hybrid-π (Giacoletto) model of the transistor. The capacitors $C_{b'e}$ and $C_{b'c}$ are the emitter and collector junction capacitances mentioned above.

The resistance $r_{bb'}$ is the bulk resistance of the semiconductor material between the external base terminal B and the active internal base point B' in the device. Its value is of the order of 50 Ω. Also,

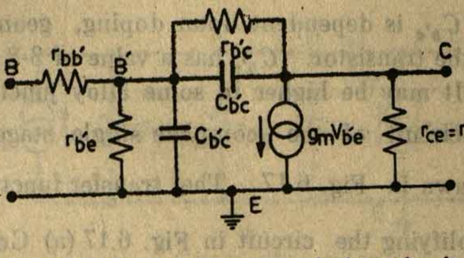


Fig. 6.16 Hybrid $-\pi$ equivalent circuit

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{\beta}{g_m} \cong \beta r_e \qquad (6.2.20)$$

The input resistance r_i between terminals B and E as defined earlier is truly

$$r_i = r_{bb'} + r_{b'e} \cong r_{b'e} \qquad (6.2.21)$$

$$\text{since } r_{b'e} \gg r_{bb'}$$

The resistance $r_{b'c}$ accounts for the feedback effect between the output and the input due to the base-width modulation. Its value is very large and is omitted in our analysis. The resistance r_{ce} is the output resistance between the collector and the emitter terminals and is equal to r_0 as has been defined earlier. Since this value is very large, it is neglected in comparison to $R_{CL} (= R_C \parallel R_L)$.

The effect of the capacitance $C_{b'e}$ in shunt with $r_{b'e}$ is to reduce the voltage $V_{b'e}$ (S) at higher frequencies. Since the controlled generator is $g_m V_{b'e}$ the output will decrease with frequency. The frequency at which $I/\omega\, C_{b'e} = r_{b'e}$ is known as the Beta cut-off (ω_β) frequency of the transistor. As the frequency is increased further, the current gain of the device goes on falling and at the transition frequency, ω_T, the current gain is unity. ω_T is a parameter of the transistor which is specified by the manufacturer and indicates that $\beta = 1$ at this frequency. Evidently, therefore

$$\omega_T = \beta, \omega_\beta$$

$$\text{or } \omega_\beta = \frac{\omega_T}{\beta} \qquad (6.2.22)$$

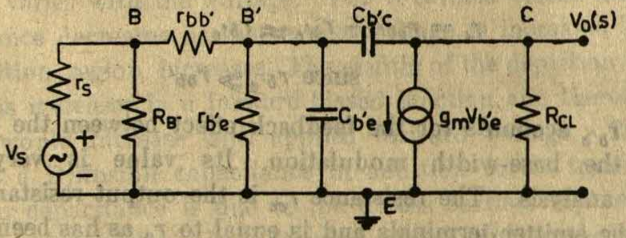
$$\text{hence } C_{b'e} = \frac{1}{r_e \omega_T} = \frac{g_m}{\omega_T} \qquad (6.2.23)$$

$$\text{since } r_{b'e} = \beta r_e$$

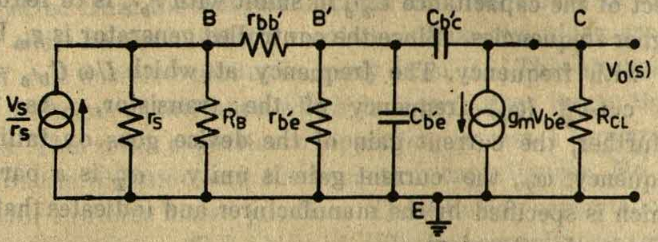
$f_T = \dfrac{\omega_T}{2\pi}$ may be anywhere between 100 to 1000 MHz. for silicon transistors.

The capacitance $C_{b'c}$ is dependent upon doping, geometry of the junction and the packaging of the transistor. $C_{b'c}$ has a value of 3-8 *pf* for silicon planar epitaxial transistors. It may be higher in some alloy junction transistors.

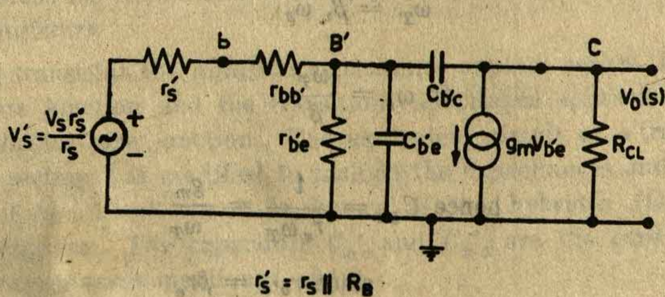
The equivalent circuit of the complete single stage amplifier at high frequencies is thus drawn in Fig. 6.17. The transfer function $G_V(s) = \dfrac{V_O(s)}{V_S(s)}$ can be found by simplifying the circuit in Fig. 6.17 (a) Converting the voltage source to a current source to the left of the terminal *B*, combining r_S and R_B, converting back to voltage source $V_S \left(\dfrac{r'_s}{r_s}\right)$ and finally applying Norton's theorem again we find the situation as shown in Fig. 6.17(d). The transfer function is quite complex to calculate and therefore we shall attempt some simplifications here.



(a) Complete circuit



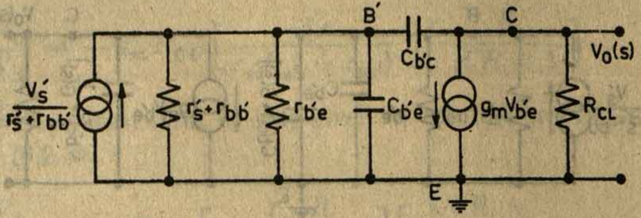
(b) Volt gen to current gen



$r'_s = r_s \parallel R_B$

$V'_s = V_s\,(r'_s / r_s)$

(c) Back to volt gen



(d). Modified circuit

Fig 6.17 High frequency equivalent circuit of transistor CE amlifier

Let us assume a current I through the capacitor $C_{b'c}$. We shall express this current I in terms of the voltages $V_{\dot{b}e}$ and $V_O(s)$ which would enable us to remove $C_{b'c}$ from between the nodes B' and C and place the equivalent capacitors between B' and E and between C and E. The equivalence should guarantee that the node currents at B and C remain unaltered. This simplification is due to Miller and gives fairly accurate results.

$$\text{Now } I = s\,C_{b'c}(V_{b'e} - V_O) \tag{6.2.24}$$

$$\text{or } I = s\,C_{b'c}.V_{b'e}\left(1 - \frac{V_O}{V_{b'e}}\right)$$

$$\text{Let } \frac{V_O(s)}{V_{b'e}(s)} = -\,G(s), \text{ then}$$

$$\text{or } I = s\,[C_{b'e}\cdot(1 + G(s)].V_{b'e} \tag{6.2.25}$$

As far as the B' terminal is concerned the current flowing out of it is given by this eq. (6.2.25). The same current will flow out if a capacitor of value $C_{b'c}\,(1 + G(s))$ is connected from B' to E and B' is disconnected from the collector.

Similarly at the collector terminal C a current of I' is going out

$$I' = s\,C_{b'c}\cdot\left[\,V_O(s) - V_{b'e}(s)\,\right]$$

$$= s\;C_{b'c}\;V_O(s)\left[1 - \frac{V_{b'e}(s)}{V_O(s)}\right]$$

$$= s\,C_{b'c}\left[1 + \frac{1}{G(s)}\right]\cdot V_O(s) \tag{6.2.26}$$

Thus, as far as the collector terminal is concerned the same current will flow if the C and B' are disconnected but a capacitance of $C_{b'c}\left(1 + \frac{1}{G(s)}\right)$ is connected- from C to E. The nodal equations at the nodes B' and C are satisfied if the circuit of Fig. 6.17(b) is redrawn as in Fig. 6.18. The two new

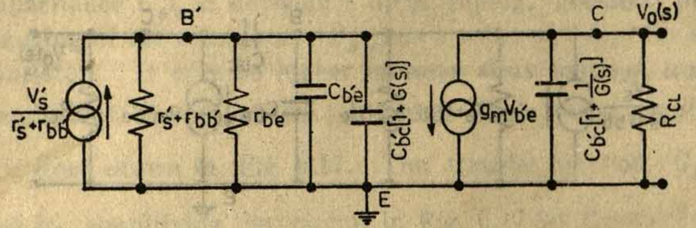


Fig. 6.18 Miller's equivalent circuit

capacitances $(1+G)\,C_{b'c}$ and $\left(1+\frac{1}{G}\right) C_{b'c}$ are known as the Miller's capacitances. Since the gain G is much larger than unity, the capacitance at the collector terminal is approximately equal to $C_{b'c}$. $(1+G)\,C_{b'c}$ in parallel with $C_{b'e}$ makes the base capacitance quite large. In conjunction with the resistances shown the high frequency response is governed, therefore, more by the base circuit than the collector circuit.

For the calculation of the high frequency response, therefore, the input circuit of Fig. 6.18 is again simplified to the one shown in Fig. 6.19. The actual values of R and C are given by

$$R = \frac{(r'_s + r_{bb'})\, r_{b'e}}{r'_s + r_{bb'} + r_{b'e}} \tag{6.2.27}$$

$$\text{and } C = C_{b'e} + (1+G)\, C_{b'c} \tag{6.2.28}$$

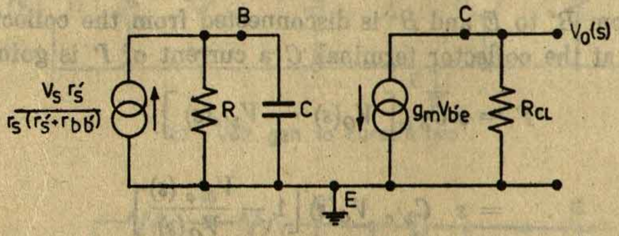


Fig. 6.19 Final Equivalent Circuit

The voltage $V_{b'e}$ can be calculated from eq. (6.2.27) and (6.2.28) as

$$V_{b'e} = \frac{V_S}{r_s}\left(\frac{r_{s'}}{r_{s'} + r_{bb'}}\right)\frac{\mathrm{R}}{\mathrm{sCR}+1} \tag{6.2.29}$$

From Fig. 6.18

$$V_O = -\,g_m V_{b'e} \times R_{CL}$$

neglecting $C_{b'e}$ at the output

Hence $$\frac{V_O}{V_S} = -g_m R_{CL}\left[\frac{r_{s'}}{r_s(r_{s'}+r_{bb'})}\right]\left[\frac{R}{sCR+1}\right] \tag{6.2.30}$$

The frequency dependent term is only given in the last bracket of eq. (6.2.30). Rewriting eq. (6.2.30)

$$\frac{V_O}{V_S} = -g_m R_{CL}\left[\frac{r_{s'}R}{r_s(r_{s'}+r_{bb'})}\right]\left[\frac{1/CR}{s+\frac{1}{RC}}\right] \tag{6.2.31}$$

The eq. (6.2.31) shows one pole at $\omega_H = \frac{1}{RC}$. Hence the upper 3 dB frequency is given by

$$\omega_H = \frac{1}{RC} \tag{6.2.32}$$

$$\text{or } \omega_H = \frac{1}{\frac{(r_{s'}+r_{bb'})\,r_{b'e}}{r_{s'}+r_{bb'}+r_{b'e}}\cdot\left[C_{b'e}+(1+G)C_{b'c}\right]} \tag{6.2.33}$$

Now G has been defined as $-\frac{V_o}{V_{b'e}} = g_m R_{CL} \approx \frac{R_{CL}}{r_e}$

substituting in eq. (6.2.33)

$$\omega_H = \frac{r_{s'}+r_{bb'}+\beta r_e}{(r_{s'}+r_{bb'})\,\beta r_e}\cdot\frac{1}{\left[\frac{1}{r_e\omega_T}+\left(1+\frac{R_{CL}}{r_e}C_{b'c}\right)\right]} \tag{6.2.34}$$

If we neglect $r_{bb'}$ in eq. (6.2.34) and assume that $R_{CL} \gg r_e$ then we can simplify it as

$$\omega_H = \frac{r_{s'}+\beta r_e}{\beta r_{s'}}\left[\frac{1}{\frac{1}{\omega_T}+R_{CL}C_{b'c}}\right] \tag{6.2.35}$$

Similarly the gain equation can be written as, assuming that $R_B \gg r_s$ and neglecting $r_{bb'}$

$$\frac{V_o(s)}{V_s(s)} = -g_m R_{CL}\cdot\left(\frac{r_{b'e}}{r_s+r_{b'e}}\right)\cdot\frac{\omega_H}{S+\omega_H} \tag{6.2.36}$$

$$G_V(s) = \frac{V_O(s)}{V_S(s)} = -G_V(\text{mid}).\frac{\omega_H}{s+\omega_H} \tag{6.2.37}$$

The frequency and phase response are shown in Fig. 6.20.

Example 6.2.6

In a transistor amplifier $I_C = 2\text{mA}$, $\beta = 100$, $r_{bb'} = 50\,\Omega$ $R_C = R_B = 2\text{K}\Omega$, $R_E = 0.68\text{K}\Omega$, $r_s = R_L = 600\,\Omega$, $\omega_T = 250$ MHz, $C_{b'c} = 3\,pf$. Calculate $C_{b'e}$ and the ω_H.

Since $I_C = 2$ mA

$$g_m = 80\ \text{m}\mho$$

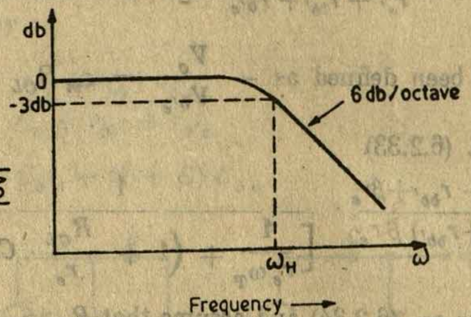
or $$r_e = \frac{1}{g_m} = 12.5\ \Omega$$

$$r_{s'} = r_s \,||\, R_B = 0.462\ \text{K}\,\Omega$$

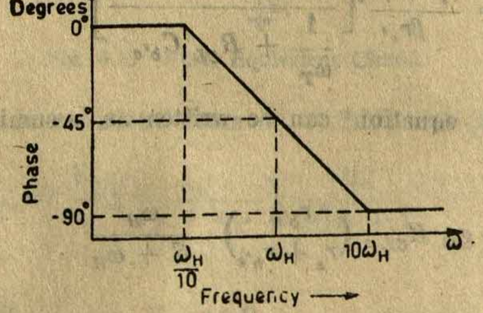
$$r_{s'} + r_{bb'} = 462 + 50 = 512\ \Omega$$

also $$r_{b'e} = \beta\, r_e = 1250\ \Omega$$

$$R_{CL} = 0.462\ \text{K}\ \Omega$$



(a) Frequency response



(b) Phase response

Fig. 6.20 High frequency response of CE amplifier

$$\text{Now} \quad C_{b'e} = \frac{1}{r_e \omega_T}$$

$$= \frac{1}{12.5 \times 2\pi \times 250 \times 10^6}$$

$$\text{or } C_{b'e} = 50.9 \times 10^{-12}$$

We can calculate R and C from eq. (6.2.27) and (6.2.28) as

$$R = \frac{(r_s' + r_{bb'})\, r_{b'e}}{r_s' + r_{bb'} + r_{b'e}}$$

$$= \frac{0.512 \times 1.25}{0.512 + 1.25} \times 10^3$$

$$R = 0.36 \text{ K}\Omega$$

$$\text{and} \quad C = C_{b'e} + (1 + R_{CL}\, g_m).\, C_{b'c}$$

$$= 50.9 \times 10^{-2} + 3.88 \times 10^{-12}$$

$$\text{or} \quad C = 164.8 \ pf$$

$$\text{Hence } f_H = \frac{1}{2\pi RC} = \frac{10^{12}}{2\pi \times 360 \times 164.8}$$

$$\text{or} \quad f_H = 2.68 \text{ MHz}$$

6.2.3 ω_T AND ω

The capacitance $C_{b'c}$ is normally specified by the manufacturer as C_{ob} in the data sheet of the device. The capacitor $C_{b'e}$ is not directly given in the data sheets. It is obtained from a parameter f_T defined as the frequency at which the short-circuit current gain of the CE transistor becomes unity. f_T is specified in the data sheets. Let us consider the CE equivalent circuit shown in Fig. 6.17 for calculating f_T. If we short circut the output, that is make $R_{CL} = 0$, then C and E terminals are at the same potential. Under this condition we can redraw the circuit as shown in Fig. 6.21. The current gain G_I (s) is calculated as

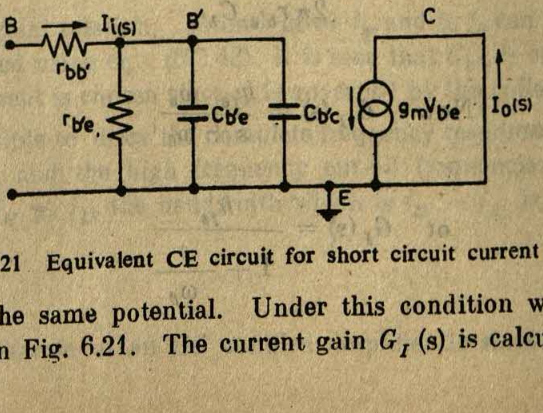


Fig. 6.21 Equivalent CE circuit for short circuit current gain

$$G_I(s) = \frac{I_0\ (s)}{I_i\ (s)} = \frac{g_m V_{b'e}}{I_i\ (s)} \qquad (6.2.38)$$

Writing $V_{b'e}$ in terms of $I_i\,(s)$

$$G_I(s) = \frac{g_m \cdot I_i\,(s)}{I_i\,(s)} \times \frac{r_{b'e} \times \dfrac{1}{s\,(C_{b'e} + C_{b'c})}}{r_{b'e} + \dfrac{1}{s\,(C_{b'e} + C_{b'c})}} \qquad (6.2.38)$$

$$= \frac{h_{fe}\,(\dfrac{1}{r_{b'e}\,(C_{b'e} + C_{b'c})}}{s + \dfrac{1}{r_{b'e}\,(C_{b'e} + C_{b'c})}}$$

since $g_m r'_{b\,e} = \beta$, and hence

$$G_I(s) = \frac{\omega_\beta}{s + \omega_\beta} \qquad (6.2.39)$$

$$\text{where } \omega_\beta = \frac{1}{r_{b'e}\,(C_{b'e} + C_{b'c})}$$

In equation (6.2.39) we see that the short circuit CE current gain at medium and low frequencies is h_{fe}. At $\omega = \omega\,\beta$, the h_{fe} falls by 3 dB. The frequency f_β is known as the β cut off frequency because at this frequency the β decreases by 3 dB Thus

$$f_\beta = \frac{1}{2\pi\ r_{b'e}\ (C_{b'e} + C_{b'c})} \qquad (6.2.40)$$

$$\approx \frac{1}{2\pi\, r_{b'e}\ C_{b'e}}$$

$$\text{Now} \quad G_I(s) = \frac{h_{fe} \cdot \omega_\beta}{s + \omega_\beta}$$

$$\text{or} \quad G_I(s) = \frac{h_{fe}}{1 + \dfrac{s}{\omega_\beta}}$$

Putting $s = j\omega$

$$G_I(j\omega) = \frac{h_{fe}}{1 + j\left(\frac{\omega}{\omega_\beta}\right)} = \frac{h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}$$

Hence $$|G_I(j\omega)| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

Now the magnitude of $G_I j(\omega)$ is unity at a frequency defined and

$$|G_I(j\omega)| = 1 \quad \text{at } f = f_T$$

or $$\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)} = h_{fe}$$

or $$\frac{f_T}{f_\beta} \approx h_{fe}$$

Therefore

$$f_T \approx h_{fe} \cdot f_\beta = \beta \cdot f_\beta \tag{6.2.41}$$

or $$\omega_T = \beta\, \omega_\beta$$

Using the value of f_β as $\dfrac{1}{2\pi r_{b'e} C_{b'e}}$

we rewrite eq. (6.2.41) as

$$\omega_T = \beta \frac{1}{2\pi r_{b'e} C_{b'e}} = \frac{1}{2\pi \beta r_e . C_{b'e}}$$

Hence $$C_{b'e} = \frac{1}{r_e\, \omega_T} \tag{6.2.42}$$

This is a very important relation. From a given f_T and β, f_β can be obtained and $C_{b'e}$ can be calculated using eq. (6.2.42). It is seen that $C_{b'e}$ is calculated directly if the operating current is chosen since r_e is governed by the collector d.c. current.

It is now possible to draw the complete frequency response of the amplifier. The low frequency and the high frequency cut-off frequencies are separately calculated. Since $f_H \gg f_L$, the bandwidth which is $f_H - f_L$ is usually taken as f_H only.

Example 6.2.7

The circuit diagram of an *RC* coupled amplifier is shown in Fig. E.6.2.1

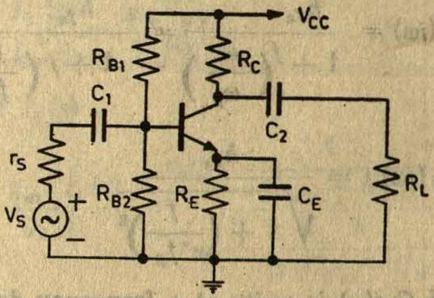


Fig. E. 6.5

The values of the components are $C_1 = C_2 = 25\mu f$, $C_E = 500\ \mu f$, $I_C = 2\text{mA}$, $R_E = 1\ \text{K}\Omega$, $R_{B1} \parallel R_{B2} = R_B = 3\ \text{K}\Omega$, $R_C = 2.2\ \text{K}\Omega$. The transistor parameters are $\beta = 200$, $C_{b'c} = 3\ pf$, $f_T = 200$ MHz. Calculate the f_H, f_L and plot phase response of the amplifier.

Neglect $r_{bb'}$. It is also given that $r_s = R_L = 600\ \Omega$.

Since $I_C = 2\ \text{mA}$

we have $r_e = 12.5\ \Omega$

$$r_{b'e} = \beta r_e = 200 \times 12.5 = 2.5\ \text{K}\Omega$$

$$g_m = 0.08\mho$$

$$r'_{st} = r_s \parallel R_B = 500\Omega$$

$$R_{CL} = R_C \parallel R_L = 470\ \Omega$$

$$C_{b'e} = \frac{1}{r_e \omega_T} = \frac{g_m}{\omega_T} = 63.6\ pf$$

$$R_i = R_B \parallel r_{b'e} = 1.36\ \text{K}\Omega$$

Now the effect of C_1 can be calculated by finding $f_L|_{C_1}$ from eg. 6.2.5 as

$$f_L|_{C_1} = \frac{1}{2\pi (R_i + r_s)\, C_1}$$

$$= 3.25\ \text{Hz}$$

Similarly $f_L|_{C_2}$ from eq. (6.2.7) is

$$f_L|_{C_2} = \frac{1}{2\pi (R_C + R_L)\, C_2}$$

$$= 2.27\ \text{Hz}$$

From eq. 6.2.19 we can calculate the $f_L|\, C_E$ as

$$f_L\Big|_{C_E} = \frac{1}{2\pi(C_E R_E)} \quad \frac{R_1 + r_s}{R_1 + r_s + K\beta R_E}$$

$$\text{or} \quad f_L\Big|_{C_E} = 21.6 \text{ Hz}$$

We can calculate f_H by finding R and C of (6.2.27) and (6.2.28) as

$$R = \frac{0.5 \times 2.5}{0.5 + 2.5} = 0.417 \text{ K}\Omega$$

$$C = 63.6 \times 10^{-12} + 115.8 \times 10^{-12}$$

$$= 179.4 \; pf$$

$$\text{Hence } f_H = \frac{1}{2\pi \times RC} = 2.12 \text{ MHz}$$

The lower 3dB frequency is virtually decided by C_E and is 21.6 Hz. The bandwidth is thus $(2.12 \times 10^6 - 21.6)$ HZ $\approx 2.12 \times 10^6$ Hz only.

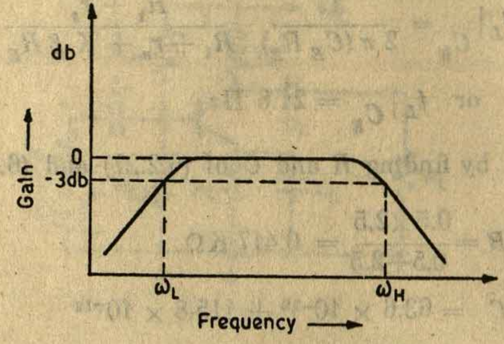
The phase response is plotted with the help of plots shown in Fig. (5.16) and Fig. (5.15). The frequency and phase response is shown in Fig. E 6.2.2 (a) and (b).

6.3 FET Amplifier

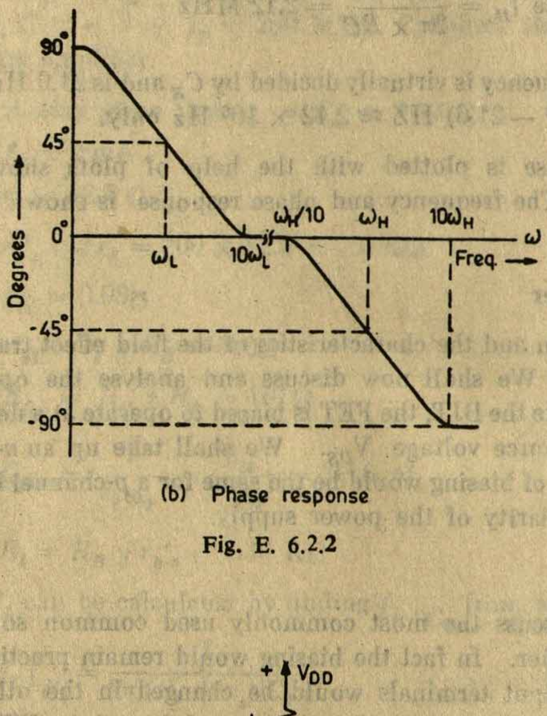
The operation and the characteristics of the field effect transistors have been described earlier. We shall now discuss and analyse the operation of a FET amplifier. Just like the BJT, the FET is biased to operate at a desired drain current I_D and drain-to-source voltage V_{DS}. We shall take up an *n*-channel FET only but the techniques of biasing would be the same for a *p*-channel FET except for the reversal of the polarity of the power supply.

6.3.1. SELF BIAS

We shall discuss the most commonly used common source configuration of the FET amplifier. In fact the biasing would remain practically the same but the input and output terminals would be changed in the other configurations. The gate-to-source junction is always reversed biased in FETs. The gate has to be at a negative voltage compared to the source for an *n*-channel FET. The drain-to-source d.c. supply is positive to enable the majority carriers to travel from the source to the drain. A seperate negative supply may be used for the gate-to-source biasing. Alternatively a resistance is placed in the source lead as shown in Fig. 6.22. The current flowing from drain to the source would develop a voltage across this source resistance R_S with the source end being positive. If the gate is connected to the other end of the resistor R_S through a resistance R_G then the gate is biased negatively with respect to the source. From the I_{DS}



(a) Frequency response



(b) Phase response

Fig. E. 6.2.2

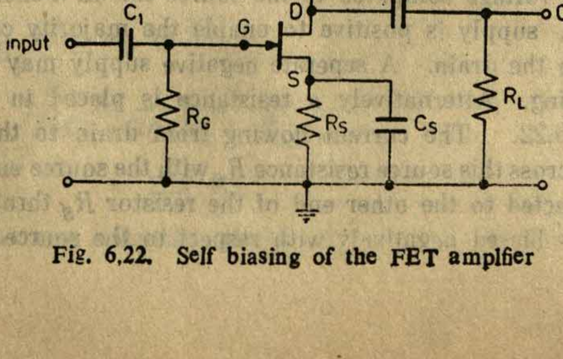


Fig. 6.22. Self biasing of the FET amplfier

versus V_{DS} output characteristics and the I_{DS} versus V_{GS} transfer characteristics, supplied by the manufacturer, the required V_{GS} for a given Q point is read out. The resistance R_S is then given by

$$R_S = \frac{|V_{GS}|}{I_{DS}} \tag{6.3.1}$$

The resistance R_D is calculated as

$$R_D = \frac{V_{DD} - V_{DS} - R_S \cdot I_{DS}}{I_{DS}} \tag{6.3.2}$$

The gate resistance R_G is provided to give a d.c path between the gate and the source. Since the gate-source junction is reversed biased, its resistance is quite large and the input impedance of the FET amplifier is decided by the R_G. Therefore R_G can be chosen to be very large except that its value should be smaller than the reverse resistance of the G-S diode. Also the reverse saturation current, which is extremely small, a few nA, should not cause an appreciable drop across R_G.

Usually, the output and the transfer characteristics supplied by the manufacturer is required for calculating the values of the biasing resistances. It has been pointed out earlier in chapter 3 that the transfer characteristics of the FET may be approximated by the following relation

$$I_D = I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{6.3.3}$$

where I_D is the desired drain current,

$I_{DSS} = I_{DS}$ with $V_{GS} = 0$

and V_P = Pinch-off voltage (it is a negative voltage for an n-channel FET)

The voltage V_{GS} can be found using the relation in eq. (6.3.3) and the characteristic curves are not needed. The parameters like V_P and I_{DSS} are, however required to be known and the manufacturers normally specify them.

Example 6.3.1.

A FET is to be biased for a I_D = 2mA and V_{DS} of $5V$ using the self baising resistance R_S. The characteristics V_{DS}—I_{DS} and V_{GS}—I_{DS} are given in the Fig. E. 6.3.1 (a) and (b). It is given that $V_{DD} = 12V$, $V_P = -2.5$V, $I_{DSS} = 4$ mA.

From the transfer characteristic V_{GS}—I_{DS} given in Fig. E. 6.3.1 we find a suitable operating point Q. The drain current is I_D and the gate-source voltage is V_{GS} at this point. The bias line joins the origin to Q giving the slope of the resistance R_S. Thus

$$R_S = \frac{-V_{GS}}{I_D} = \frac{10^3}{2} = 500\,\Omega$$

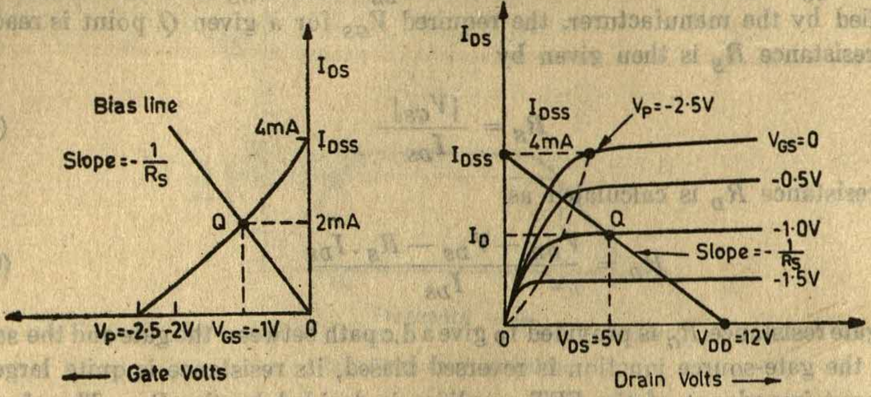


Fig. E 6.3.1

Extending to the output-characteristics in Fig. E· 6.3.1 we locate the point Q as shown. Joining V_{DD} to Q gives the slope of the resistance $\frac{1}{R_D + R_S}$. Since we have already calculated R_S, we get the value of R_D as 3 KΩ.

Example 6.3.2.

While biasing a FET at $I_D = 2$ mA, $V_{DS} = 6$ V, it is given that $V_P = -4.8V$ and $I_{DSS} = 4$ mA. The circuit shown in Fig. 6.22 is used for the self biasing. Calculate the values of R_S and R_D.

From eq (6.3.3)

$$2 \times 10^{-3} = 4 \times 10^{-3}\left(1 + \frac{V_{GS}}{4.8}\right)^2$$

It should be remembered that V_{GS} is negative

Hence $V_{GS} = -1.406$ volt

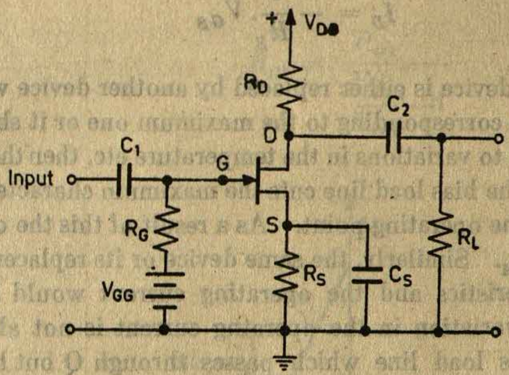
From eq. (6.3.1), we get $R_S = 0.7\text{K}\ \Omega$ and from eq. (6.3.2)

$$R_D = 2.3\text{K}\ \Omega$$

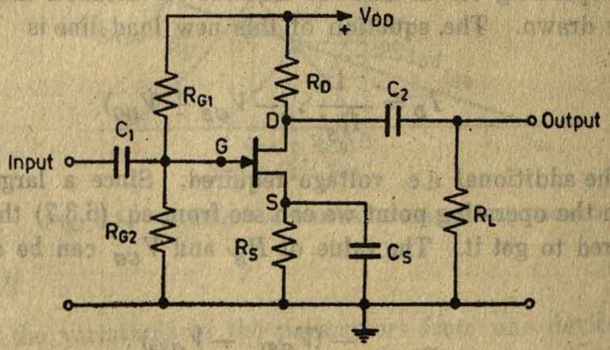
6.3.2. MODIFIED BIASING

There are device-to-device variations and the device parameters change due to the temperature in the FET also. It is required that the operating point be stable inspite of these variations. The resistance R_S, used actually for producing a bias voltage, helps in reducing the effects of the temperature and device to device variations of the parameters. For example, if due to some reasons the drain current increases, the voltage across R_S would increase making the FET conduct less because V_{GS} becomes more negative. Thus I_D would not be allowed to change much. However, a large R_S, used for better stability, requires a large supply voltage as seen from eq. (6.3.2.). To get a proper value of V_{DS} and R_D the V_{DD} would have to be increased. This difficulty can be avoided by employing a supply V_{GG} as shown in Fig. 6.23 (a). Considering the gate source loop, we can find the value of R_S as follows. It is seen that $V_{GG} = V_{GS} + I_D . R_S$. If we neglect any voltage drop across R_G due to reverse saturation current, we obtain

$$R_S = \frac{V_{GG} - V_{GS}}{I_D} \tag{6.3.4}$$



(a) Two supplies biasing circuit



(b) Single supply biasing circuit

Fig. 6.23 Modified FET Biasing curcuit

Comparing the eq. (6.3.4) with equation (6.3.1) it is seen that R_S can now be controlled to any desired value because of the inclusion of V_{GG}.

How much should the R_S be depends upon the amount of control desired on the variations of the operating point. The manufacturers normally specify the extreme limits within which all the devices of one type are likely to have their characteristics. Typical transfer characteristics of an FET are shown in Fig. 6.24.

The maximum and minimum variations in the transfer characteristics are also shown. The operating point is taken at Q where the drain current is I_{DQ} and the gate-source voltage is V_{GSQ}. To get this operating point, the value of R_S is

$$R_S = \frac{-V_{GSQ}}{I_{DQ}} \tag{6.3.5}$$

The bias load line is given by the equation

$$I_D = -\frac{1}{R_S} . V_{GS} \tag{6.3.6}$$

If this particular device is either replaced by another device which happens to have the characteristics corresponding to the maximum one or it shifts to the maximum characteristic due to variations in the temperature etc. then the operating point Q would be shifted. The bias load line cuts the maximum characteristics at a point which then becomes the operating point. As a result of this the operating current changes from I_{DQ} to I_{DA}. Similarly, the same device or its replacement may follow the minimum characteristics and the operating current would become I_{DB}. If this large amount of variation in the operatng current is not allowed, then we can draw another bias load line which passes through Q but has smaller slope than the previous one. Such a load line with a slope of $1/R_S'$, is shown in Fig. 6.24. The currents then would be I_{DA}' and I_{DB}' and the variations in I_{DQ} are reduced. Depending on the allowed amount of variation the bais load line is appropriately drawn. The equation of this new load line is

$$I_D = \frac{1}{R_S'} . (-V_{GS} + V_{GG}) \tag{6.3.7}$$

where V_{GG} is the additional d.c. voltage required. Since a larger R_S' reduces the variations in the operating point we can see from eq. (6.3.7) that a larger V_{GG} would be required to get it. The value of R_S' and V_{GG} can be calculated from Fig. 6.24 as

$$R'_S = \frac{-(V_{GS1} - V_{GS2})}{I_{D1} - I_{D2}} \tag{6.3.8}$$

and

$$V_{GG} + |V_{GS1}| = I_{D1} . R_S' \tag{6.3.9}$$

where I_{D1} and I_{D2} are the two limits of the current, with $I_{D1} > I_{D2}$ and V_{GS1} and V_{GS2} are the two corresponding gate-source voltage with $|V_{GS1}| > |V_{GS2}|$. We can thus calculate R'_S and V_{GG} to limit the variations in I_D even when the temperature varies or the device is replaced. The resistances R_G and R_D are chosen as discussed earlier.

Since V_{GG} is positive and the gate current is practically zero, it can be derived from V_{DD} with the help of potential divider R_{G1} and R_{G2} as shown in Fig. 6.23 (b).

$$V_{GG} = \frac{V_{DD}}{R_{G1} + R_{G2}} \times R_{G2} \tag{6.3.10}$$

Taking $\qquad R_{G1} \,||\, R_{G2} = R_G$

$$R_{G1} = \frac{V_{DD} \,.\, R_G}{V_{GG}} \tag{6.3.11}$$

$$R_{G2} = \frac{R_{G1}}{\dfrac{V_{DD}}{V_{GG}} - 1} \tag{6.3.12}$$

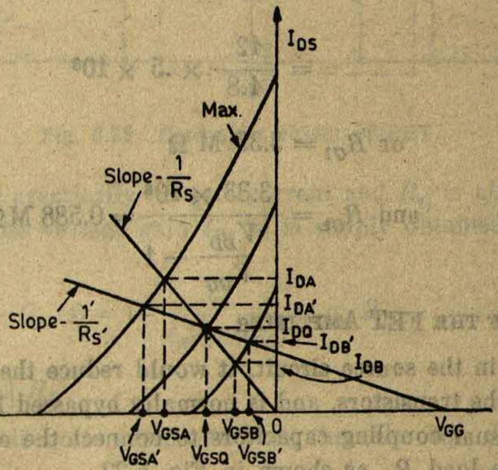


Fig. 6.24 Extreme variations of transfer characteristics

Example 6.3.3

Due to the variations of the parameters from one device to another and also the temperature, if is found that in a FET circuit with $V_{GG} = 0$ the drain current changes from 0.3 mA to 0.8 mA and gate source voltage changes from $-.35\ V$ to $-.95$ volts. The Q point is desired to be at $I_D = .5$ mA, $V_{GS} = -0.6\ V$ with $V_{DD} = 12$ volts. It is required to stabilise this operating point so that the change in I_D is from 0.6 to 0.4 mA and in V_{GS} from $-.2\ V$ to $-1.2\ V$. Calculate the values of $R_{S'}$, $-V_{GG}$ required to obtain the specified stability.

The resistance $R_{S'}$ when $V_{GG} = 0$, is calculated simply to be $\dfrac{|V_{GS}|}{I_D} = \dfrac{+0.6}{0.5} \times 10^3 = 1.2$ K Ω.

Now if the variation in I_D is reduced to the desired value by including V_{GG}, then from eq. (6.3.8) we can calculate

$$R_{S'} = \frac{-(-1.2+.2)}{0.6 - 0.4}\ 10^3 = 5K\,\Omega$$

From eq. (6.3.9) we get

$$V_{GG} = 0.6 \times 10^{-3} \times 5 - 10^3 \times 1.2$$

$$\text{or}\quad V_{GG} = 1.8\text{ V}$$

This voltage can be derived from potential divider chain as shown in Fig. 6.23 (b). Let us assume that $R_G = 0.5\,\text{M}\Omega$. Then from eq. (6.3.11) and (6.3.12) we get

$$R_{G1} = \frac{V_{DD}}{V_{GG}} \cdot R_G$$

$$= \frac{12}{1.8} \times .5 \times 10^6$$

$$\text{or}\ R_{G1} = 3.33\text{ M}\,\Omega$$

$$\text{and}\ R_{G2} = \frac{3.33 \times 10^6}{\dfrac{V_{DD}}{V_{GG}} - 1} = 0.588\text{ M}\Omega.$$

6.3.3 ANALYSIS OF THE FET AMPLIFIER

Since R_S is in the source circuit, it would reduce the gain of the amplifier, as the R_E did in the transistors, and is normally bypassed by C_S. Capacitors C_1 and C_2 are the usual coupling capacitors to connect the amplifier to the signal source and to the load R_L as shown in Fig. 6.22.

The small signal mid-frequency range equivalent circuit of the FET is shown in Fig. 6.25. The parameter g_m is the transconductance described earlier and is given by the slope of the transfer characteristics. Hence

$$g_m = \frac{\Delta I_D}{\Delta V_{GG}} \tag{6.3.14}$$

Differentiating eq. (6.3.3) and making $V_{GS} = V_{GS} + V_{gs}$, where V_{gs} is the signal gate-source voltage, we obtain

$$g_m = -\frac{2 I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{6.3.15}$$

The eq. (6.3.15) can be re-written as

$$g_m = \left(-\frac{2\,I_{DSS}}{V_P}\right).\sqrt{\frac{I_D}{I_{DSS}}} \qquad (6.3.16)$$

Thus, the value of g_m can be calculated for the given quiescent current I_D. The resistance r_d is the drain resistance and can be obtained from the output characteristics as

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}} \qquad (6.3.17)$$

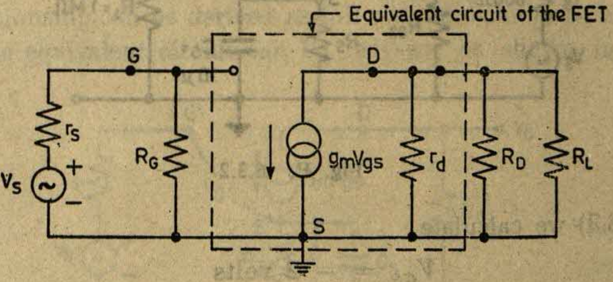


Fig. 6.25 Equivalent circuit of FET

Since there is practically no gate current and R_G is also very large we can write $V_{gs} = V_s$. The voltage gain G_V (s) is simply obtained as

$$G_V(s) = -\frac{r_d}{r_d + R_{DL}} \times g_m R_{DL} \qquad (6.3.18)$$

where $R_{DL} = R_D \parallel R_L$

If $r_d \gg R_{DL}$ which is quite often the case, then the eq. (6.3.18) simplifies to

$$G_V(s) = -g_m R_{DL} \qquad (6.3.19)$$

The input impedance is R_G in parallel with the reverse resistance of the gate source junction which is usually very large. The output impedance is the resistance R_D in parallel with r_d. The current gain is practically infinity because the input current is nearly zero. The current gain is thus not significant here. The values of the coupling capacitor C_1 and C_2 and the bypass capacitor C_S which determine the low frequency response of the FET amplifier are obtained individually following the same technique as was used for the transistors.

Example 6.3.4

A practical FET amplifier is shown in Fig. E. 6.3.2. The parameters for the FET are $I_{DSS} = 8$ mA, $V_P = -4$ volts, $r_d = 50$ K Ω. The quiescent drain current is $I_D = 2$ mA. Calculate the value of g_m, the voltage gain and the lower

3dB frequency of the amplifier. It is given that $R_S = 2\text{K}\ \Omega, R_D = 4.5\text{K}\Omega$, $R_G = R_{G1} \parallel R_{G2} = 1\text{M}\Omega$

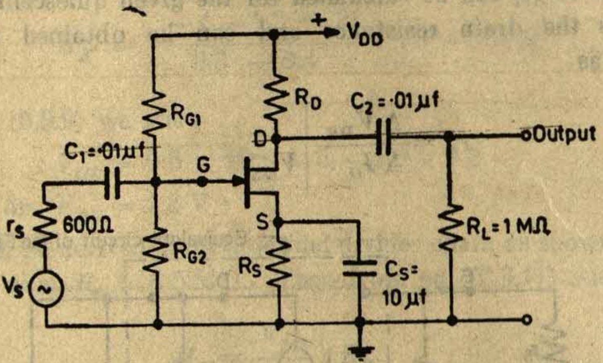


Fig. E. 6.3.2

From eq. (6.3.3) we calculate

$$V_{GS} = -\ 2 \text{ volts}$$

From eq. (6.3.16) we can get g_m as

$$g_m = \frac{2 \times 8}{4} \sqrt{\frac{2}{8}}$$

$$\text{or } g_m = 2 \text{ mA / volts}$$

From eq. (6.3.9)

$$V_{GG} = R_S \times I_D - |V_{GS}|$$

$$\text{or } V_{GG} = +\ 2 \text{ volts}$$

$$R_G = 1\ \text{M}\Omega$$

$$\text{Gain} = -\,g_m\,(R_D \parallel R_L)$$

$$= -\,2 \times 10^{-3} \times 4.5 \times 10$$

$$= -\,9.0$$

The lower 3dB frequencies due to C_1, C_2 and C_S can be calculated as follows

$$f_L \Big|_{C_1} = \frac{1}{2\,\pi\,C_1\,(R_G + r_s)}$$

$$= 1.6 \text{ Hz}$$

$$f_L \Big|_{C_2} = \frac{1}{2\,\pi\,C_2\,(R_L + R_D)}$$

$$= 1.6 \text{ Hz}$$

To calculate the effect of C_S and R_S, it can be shown in a manner very similar to eq. (6.2.19) but much more simply as

$$\frac{V_O(s)}{V_S(s)} = -g_m R_{DL} \frac{s + \dfrac{1}{C_S R_S}}{\left[s + \dfrac{1}{R_S C_S}(1 + g_m R_S) \right]}$$

$$\text{Hence } f_L \Big|_{C_S} = 35 \text{ Hz}$$

The above relationship can be derived as follows. Assuming C_1 and C_2 to be a short circuit, the equivalent circuit can be redrawn as shown in Fig. *E.* 6.3.3

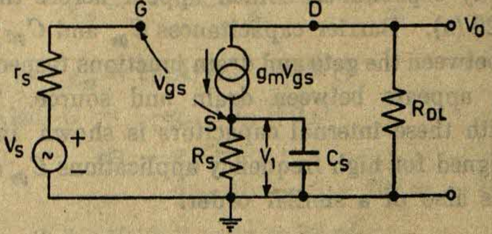


Fig. E. 6.3.3

$$V_{gs} = V_S - V_1$$

where V_1 is the voltage drop across the source terminal, and V_S is the signal voltage If the parallel combination of R_S and C_S is designated as Z_S, then

$$Z_S = \frac{R_S}{sC_S R_S + 1}$$

then $V_1 = g_m V_{gs} \cdot Z_S$

$$\text{hence } V_{gs} = \frac{V_S}{1 + g_m Z_S}$$

The output voltage V_O is given by

$$V_O = -g_m U_{gs} \cdot R_{DL}$$

substituting the value of V_{gs} we get

$$V_O = -g_m \cdot \frac{V_S \cdot R_{DL}}{1 + g_m Z_S}$$

$$\text{or } \frac{V_O}{V_S} = G_V(s) = -\frac{g_m R_L}{1 + g_m Z_S}$$

$$\text{or} \quad \frac{V_O}{V_S} = -g_m R_{DL} \frac{s + \dfrac{1}{C_S R_S}}{s + \dfrac{1}{C_S R_S}(1 + g_m R_S)}$$

The pole at the low frequency will be

$$f_L \mid C_S = \frac{(1 + g_m R_S)}{2\pi C_S R_S}$$

The high frequency response of the FET amplifier is governed by the device capacitances and stray capacitances which appear across the various terminals as shown in Fig. 6.26 (a). Barrier capacitances C_{gs} and C_{gd} appear between the gate and source and between the gate and drain junctions respectively. Capacitance of the channel C_{ds} appears between drain and source. The high frequency equivalent circuit with these internal capacitors is shown in Fig. 6.26 (b). In small transistors designed for high frequency applications C_{gs} and C_{gd} are between 1 to 5 *pf* and C_{ds} is also of a similar order.

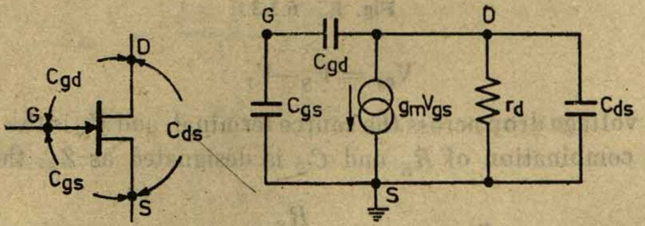


Fig. 6.26 High frequency equivalent circuit of FET

By applying Miller's theorem explained in Section 6.2.3 the effect of C_{gd} can be included as an input capacitor $C_{gd}(1 + G)$ at the gate terminal and an output capacitor of $C_{gd}\left(1 + \dfrac{1}{|G|}\right)$. The high frequency response is then easily found by obtaining the transfer function of the amplifier. Since these capacitors appear in shunt with the input and output terminals, they give rise to poles in the transfer function and the gain decreases with increasing frequency. The output capacitance causes the dominant pole and the transfer function is a single pole one. The slope of the gain-frequency curve is thus 6 *db*/octave.

Example 6.3.5

Calculate the high frequency response of an amplifier which has a FET as its active device. Given $r_d = 50\ \text{K}\Omega$, $C_{gs} = C_{gd} = 2\ pf$, $C_{ds} = 8\ pf$, $r_s = 600\ \Omega$, $R_D = 5\ \text{K}\Omega$, $I_D = 2\text{mA}$, $I_{DSS} = 8\ \text{mA}$, $V_P = -4V$, $R_L = 500\text{K}\Omega = R_G$. The equivalent circuit is shown in Fig. E. 6.3.4.

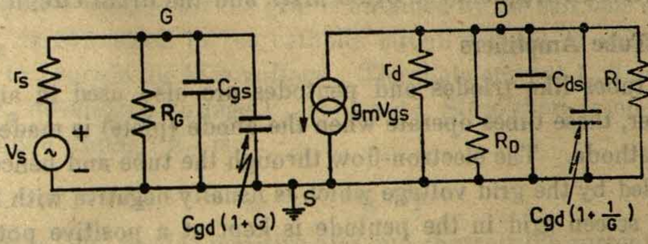


Fig. E. 6.3.4

g_m can be calculated using eq. (6.3.16) as

$$g_m = +\frac{2 \times 8 \times 10^{-3}}{4}\sqrt{\frac{2}{8}}$$

$$\text{or} \quad g_m = 2\text{mA/volt} = 2m\,℧$$

$$\text{Also} \quad G = -g_m\,(R_D\,||\,R_L)$$

$$\approx -g_m\,R_D$$

$$= -2 \times 10^{-3} \times 5 \times 10^3 = -10$$

$$\text{hence} \quad C_{gd}\,(1 + |G| = 2 \times 11 = 22\,pf$$

$$C_{gd}\left(1 + \frac{1}{|G|}\right) \approx 2\,pf$$

Now the net capacitance at the Gate is

$$C_g = 22 + 2 = 24\,pf$$

and at the drain

$$C_d = 10\,pf$$

The two networks will have the following upper 3dB frequencies

$$f_H\,|_{gate} = \frac{1}{2\pi\,(r_s\,||\,R_G)\,.\,C_g}$$

$$= \frac{1}{2 \times 600 \times 24 \times 12^{-12}}$$

$$= 110 \text{ MHz}$$

$$f_H\,|_{drain} = \frac{1}{2\pi\,(R_D\,||\,R_L)\,C_d}$$

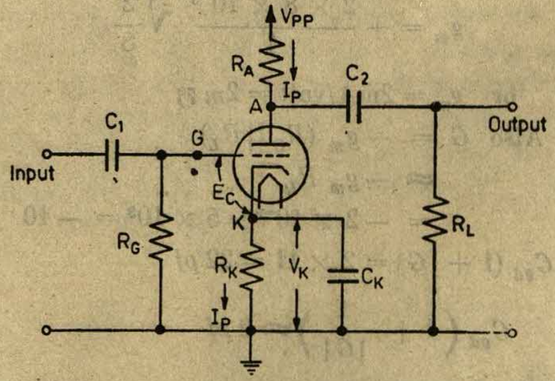
$$= \frac{1}{2 \times 5 \times 10^3 \times 10 \times 10^{-12}}$$

$$= 31.85 \text{ MHz}$$

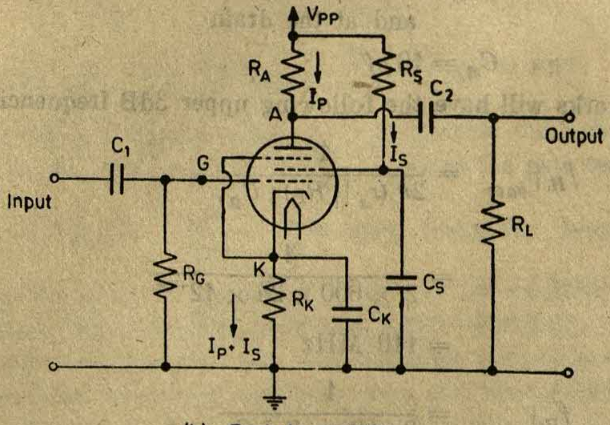
Hence the upper 3dB frequency is 31.85 MHz and the drain circuit is dominant.

6.4 Vacuum Tube Amplifiers

Vacuum tubes like triodes and pentodes are also used in amplifiers. As discussed earlier, these tubes operate when the anode (plate) is made positive with repect to the cathode. The electron-flow through the tube and hence the current flow is controlled by the grid voltage which is usually negative with respect to the cathode. The screen grid in the pentode is kept at a positive potential that is approximately equal to the plate potential. The suppressor grid is at the same potential as the cathode. The biasing circuits of the triode and pentode are shown in Fig. 6.27. The plate and the screen grids are made positive with the help of



(a) Triode amplifier



(b) Pentode amplifier

Fig. 6.27 Vacuum Tube Amplifier Biasing Circuit

d.c. supply voltage V_{PP}. The voltage is of the order of 150 to 400 volts for normal tubes. Special purpose and high power tubes have anode voltages as high as

10 KV. The negative voltage for the grid is obtained by the self bais arrangement. A resistance R_K is connected in the cathode circuit instead of using a separate negative supply to provide the bias voltage. The plate current I_P flowing through the resistance R_K develops a voltage V_K across it. Since there is no grid current, the grid to cathode voltage E_C is

$$E_C = -V_K = -R_K \,.\, I_P \tag{6.4.1}$$

This provides the needed negative bias and controls the current. The plate current I_P depends on the grid voltage E_C which in turn depends on I_P. The resistance R_A is calculated with the help of the input and the output characteristics of the vacuum tube to obtain a specified operating point with a current I_P and a plate drop V_P. The resistance R_A is instrumental in fixing the requisite voltage gain and a proper voltage drop across the plate and the cathode. The resistance R_G is connected to provide a d.c. path between the grid and the cathode. If a large R_G is used the input impedance would be very large. R_G in the range of few hundred kilo-ohms to a few megaohms are commonly used. Some electrons are itercepted by the grid and they find a path through R_G to the cathode. If R_G is very large then an undesirable large voltage drop may develop across it. Therefore there is an upper limit to the value of R_G to be used. The screen resistance R_S is calculated using

$$V_S = V_{PP} - R_S \cdot I_S \tag{6.4.2}$$

A desired screen potential is obtained with a given screen current I_S obtained from the manufacturer's sheets.

The desired operating point is marked on the output plate characteristics of the tube. A load line of slope corresponding to $1/R_A + R_K$ is drawn through this point. This load line has to satisfy the following equation

$$V_P = V_{PP} - I_P\ (R_A + R_K) \tag{6.4.3}$$

The grid bias line satisfying the equation

$$E_C = -\ V_K = -R_K\, I_P \tag{6.4.4}$$

is also drawn on the output characteristics. The intersection of these two lines is the actual operating point.

Example 6.4.1

The output characteristic of a typical triode are shown in Fig. E.6.4.1. It is given that $V_{PP} = 250\,\text{V}$ and $I_P = 3\,\text{mA}$

Locating the operating point around in the middle of total operating range of E_C(0 to 14 V), we select $E_C = -6\text{V}$. Intersection of the $I_P = 3\,\text{mA}$ and $E_C = -6$ V lines fixes the point Q. Joining $V_{PP}$and Q and extending the line gives us the load line. Thus

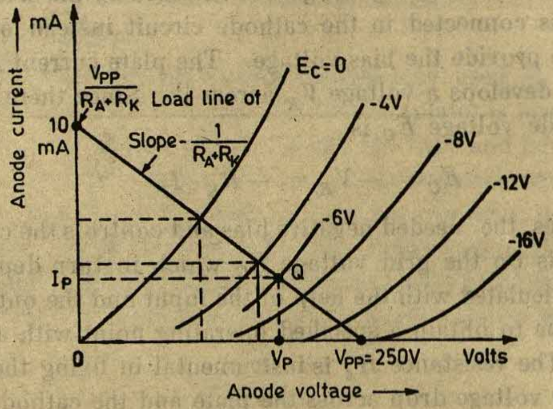


Fig. E. 6.4.1

$$R_K = \frac{6}{3} \times 10^3 = 2K\Omega$$

Now from the load line we have $R_A + R_K = 25\ K\Omega$ hence $R_A = 23\ K\Omega$. From the graph, the drop across the tube V_P is approximately 160 V. The error is because of the graphical construction.

6.4.1 VACUUM TUBE AMPLIFIER ANALYSIS

Just as in the case of BJT and FET, the V.T. amplifiers are also required to be coupled to the source and the load. To provide d.c. isolation either capacitive or transformer coupling is used. A capacitively coupled pentode amplifier is shown in Fig. 6.27 (b). The cathode resistance R_K will develop an a.c. signal voltage across it and would thus reduce the gain of the amplifier. This is prevented by by-passing the cathode resistance R_K with a capacitor C_K. The capacitor C_S by-passes the a.c. signal which would otherwise appear at the screen grid terminal. The screen grid terminal should have only a d.c. voltage. The low frequency response of the amplifier is governed by the coupling capacitors C_1, C_2 and the cathode by pass capacitor C_K. Their effect on the low frequencies can be considered individually. Let us first consider the response due to C_1 by drawing an equivalent circuit as shown in Fig. 6.28.

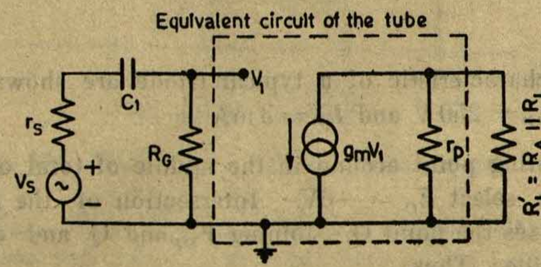


Fig. 6.28 Equivalent circuit with C_1

$$\text{Now} \quad V_1(s) = \frac{V_S(s)}{R_G + \frac{1}{sC_1}} \times R_G = \frac{V_S(s).s}{s + \frac{1}{R_GC_1}}$$

$$\text{Hence} \quad G_V(s) = \frac{V_O(s)}{V_S(s)} = -g_m R'_L \left(\frac{s}{s + \frac{1}{R_GC_1}} \right).$$

(assuming $r_P \gg R'_L$ and $R_G \gg r_S$)

$$\text{Let} \quad \omega_L \Big|_{C_1} = \frac{1}{R_G\, C_1}. \tag{6.4.5}$$

Similarly considering C_2 alone,

$$\omega_L \Big|_{C_2} = \frac{1}{(R_A + R_L)\, C_2} \tag{6.4.6}$$

where $r_P \gg (R_A \parallel R_L)$ and $R_G \gg r_s$

We now consider the cathode by-pass capacitor C_K. The equivalent circuit is drawn in Fig. 6.29. The grid to cathode voltage V_1 is given by $V_1 = V_S - V_K = V_S - Z_K \cdot g_m \cdot V_1$

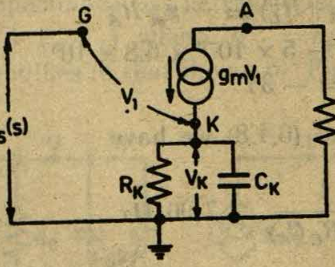


Fig. 6.29 Equivalent Circuit with C_K

$$\text{where} \quad Z_K = R_K \,\Big\|\, \frac{1}{sC_K}$$

$$\text{Rearranging } V_1(s) = -\frac{V_S(s)}{1 + Z_K \cdot g_m}$$

Now the output $V_O(s) = -g_m \cdot R'_L\, V_1(s)$

$$\text{and } V_O(s) = -g_m \cdot R'_L \cdot \frac{V_S(s)}{1 + Z_K g_m} \tag{6.4.7}$$

The transfer function $G_V(s)$ is now

$$G_V(s) = \frac{V_O(s)}{V_S(s)} = -g_m \cdot R'_L \frac{s + \dfrac{1}{R_K \cdot C_K}}{s + \dfrac{1}{C_K R_K}(1 + g_m . R_K)} \tag{6.4.8}$$

This has a pole at $s = -\frac{1}{C_1}\left(\frac{1}{R_K} + g_m.\right)$ and zero at

$s = -\frac{1}{R_K C_K}$. The lower cut-off frequency will be governed by the pole.

Example 6.4.2

In the pentode amplifier of Fig. 6.28 we have $g_m = 5\ \text{m}\Omega$, $I_p = 7.5$ mA, $I_S = 2.5$ mA, $r_p = 300\ \text{K}\Omega$, the external resistors are $R_A = 6.8\ \text{K}\Omega$, $R_G = 1\ \text{M}\Omega$, $R_K = 180\Omega$. Find the gain and lower 3db frequency if $C_1 = C_2 = 0.02\ \mu f$, $C_K = 32\ \mu f$, $r_s = 10\ \text{K}\Omega$ and $R_L = 1\text{M}\Omega$

Total current through the pentode $= 7.5 + 2.5 = 10$ mA. Hence the cathode voltage $= 180 \times 10 \times 10^{-3}$

or $E_C = 1.8$ volts

Gain $= -g_m R'_L = -g_m(R_A \| R_L) \simeq -g_m R_A$

Now $-g_m R_A = -5 \times 10^{-3} \times 6.8 \times 10^3$

hence Gain $= -34$

From eqs. (6.4.5), (6.4.6) and (6.4.8) we have

$$f_L\Big|_{C_1} = \frac{1}{2\pi(R_G C_1)} = 7.96\ \text{Hz}$$

$$f_L\Big|_{C_2} = \frac{1}{2\pi(R_A + R_L)C_2} = \frac{1}{2\ R_L C_2} = 7.96\ \text{Hz}$$

$$f_L\Big|_{C_K} = \frac{1 + g_m R_K}{2\pi C_K R_K} = 52.5\ \text{Hz}$$

The capacitors C_1, C_2 and C_K are ineffective at mid and high frequencies. The high frequency response is decided by the interelectrode capacitances C_{gk}

C_{gk} and C_{pk} and any other stray shunt capacitances coming in parallel with the input and output ports. The interelectrode capacitances are shown in Fig. 6.30.

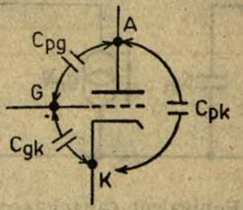
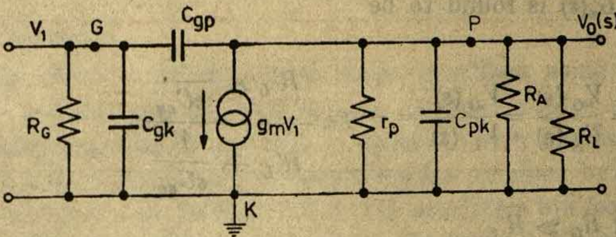


Fig. 6.30 Interelectrode capacitances in a triode

The equivalent circuit of a vacuum tube amplifier with inter-electrode capacitances is shown in Fig. 6.31. This circuit is useful in evaluating the high frequency response of the amplifier.



Fig, 6.31 High Freq. equivalent circuit of a Vacuum triode amplifier.

C_{gp} is extremely small in the case of pentodes. With the help of Miller's theorem as discussed earlier, the capacitance C_{gp} is transferred to the input terminals with a value equal to $C_{gp}(1 + g_m R'_L)$ where $R'_L = r_p \| R_A \| R_L$. The equivalent circuit of Fig. 6.31 then modifies to that shown in Fig. 6.32.

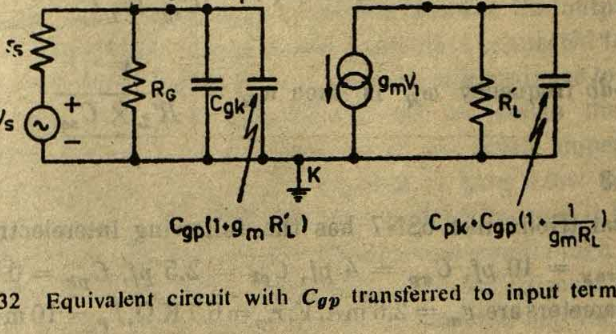


Fig. 6.32 Equivalent circuit with C_{gp} transferred to input terminals.

If the source is an ideal voltage source i.e $r_s = 0$ or $r_s \ll R_G$, then $V_1 = V_S$ and the capacitance $C_{gk} + C_{gp}(1 + g_m R'_L)$ is ineffective. However when two amplifier stages are cascaded then the capacitance at the input terminals of the 2nd stage appears at the output terminals of the first stage as shown in Fig. 6.33 where

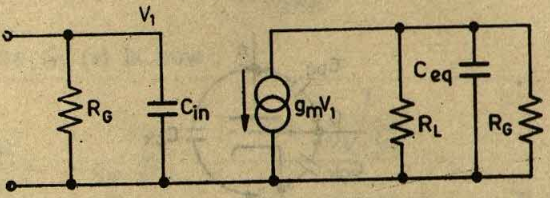


Fig. 6.33 Equivalent capacitance at the output

$$C_{eq} = C_{pk} + C_{gk}\ (\text{next stage}) + C_{gp}\left(1 + \frac{1}{g_m R'_L}\right) + C_{stray}$$

$$C_{in} = C_{gk} + C_{gp}\,(1 + g_m R'_L) + C_{stray}$$

The stray capacitances have also been included in C_{in} and C_{eq}. Now the voltage gain function $G_v(s)$ is found to be

$$G_V(s) = \frac{V_O(s)}{V_S(s)} = \frac{V_O(s)}{V_1(s)} = -g_m \frac{R'_L \times \dfrac{1}{sC_{eq}}}{R'_L + \dfrac{1}{sC_{eq}}} \tag{6.4.9}$$

assuming $R_G \gg R'_L$

Hence

$$G_V(s) = -g_m \cdot R'_L \cdot \frac{1}{sC_{eq} \cdot R_L' + 1}$$

$$\text{or } G_v(s) = -g_m \cdot R'_L \cdot \frac{1}{C_{eq} \cdot R'_L\left(s + \dfrac{1}{C_{eq} \cdot R'_L}\right)} \tag{6.4.10}$$

The upper 3-*db* frequency ω_H is then $\omega_H = \dfrac{1}{R'_L \times C_{eq}}$ (6.4.11)

Example 6.4.3

A typical triode like 6SN7 has the following interelectrode capacitances

$C_{stray} = 10\ pf$, $C_{gp} = 4\ pf$, $C_{gk} = 2.5\ pf$, $C_{pk} = 0.7\ pf$.

The other parameters are $g_m = 2.6$ mA/V, $r_p = 6.7$ KΩ, $I_P = 10$ mA, $R_G = 500$ KΩ, $R_A = 8$ KΩ, $R_L = 500$ KΩ

Calculate the gain and upper 3dB frequency

$$\text{Now } R'_L = 8\text{ K}\Omega \parallel 500\text{ K}\Omega$$

$$= 7.87\text{ K}\Omega$$

$$\text{Hence Gain} = -g_m R'_L = -2.6 \times 7.87 \approx -20.5$$

From eq. (6.4.11)

$$C_{eq} = C_{pk} + C_{gk}(1 + g_m R'_L) + C_{stray}$$

$$= 3.2 \times 10^{-12} + 4 \times 21.5 \times 10^{-12} + 10 \times 10^{-12}$$

$$C_{eq} = 99.2\ pf$$

$$\text{Hence } f_H = \frac{1}{2\pi \times R'_L C_{eq}} = \frac{1}{2 \times 7.87 \times 10^3 \times 99.2 \times 10^{-12}}$$

$$= 0.204\text{ MHz}$$

or

$$f_H = 204\text{ KHz}$$

6.5 Emitter follower

The most common of the single stage amplifiers using BJTs, FETs and vacuum tubes are the common emitter, the common source and the common cathode amplifiers respectively and their analysis has been discussed. The common base, common gate or common grid amplifiers are obtained by keeping the same biasing arrangements as in the *CE*, *CS* or *CK* amplifiers but feeding the input at the emitter, source or cathode as the case may be, instead of the base, gate or the grid. These amplifiers have some useful characteristics such as low input impedance. However, they are used in some special applications and so are not analysed here. The interested students may attempt to analyse them by drawing the equivalent circuits.

A third type of commonly used amplifier is the common/collector, common drain or common anode amplifier. The important features of this amplifier are (1) high input impedance (2) low output impedance (3) almost unity voltage gain and (4) no phase inversion between the output and the input signals. We have discussed earlier that if a circuit is connected to the output side of another circuit then it should have a high input impedance to prevent loading. This common collector type of amplifier is used to isolate the output side of circuit from being loaded by another circuit of low input impedance. Simlarly in many situations a source is normally required to have a low output impedance. This can be achieved by connecting the CC amplifier because it has a low output impedance. The FETs and the vacuum tubes have normally high input impedence whereas the BJTs have low input impedance. We shall discuss the *CC* amplifier here. It is also known as emitter follower because the emitter follows the base so far as the signal is concerned. The student may analyse the CD and CA (calthode follower) amplifiers similarly on his own.

The circuit diagram of an emitter follower is shown in Fig. 6.34. Sometimes there are two biasing resistances R_{B1} and R_{B2} in the base circuit as in the CE amplifiers. They will appear in shunt with the input thus reducing the input impedence. With a single resistance, the input impedance would not be lowered much though the d.c. bias stability will be poor. The equivalent circuit of the emitter follower is drawn in Fig. 6.35. The resistance $r_{bb'}$ has been neglected for simplicity. By applying the KCL at the nodes B and E, the output voltage $V_O = V_E$ can be found. Then the voltage gain G_V is obtained as follows

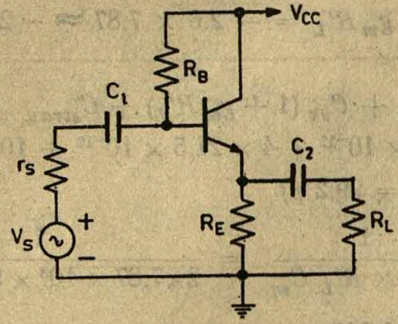


Fig. 6.34 Emitter Follower

$$V_0 = \frac{\begin{vmatrix} \dfrac{1}{r_s'} + \dfrac{1}{r_{b'e}} & \dfrac{V_s}{r_s} \\[2ex] -\dfrac{1}{r_e} - \dfrac{1}{r_{b'e}} & 0 \end{vmatrix}}{\Delta}$$

$$\text{where } \Delta = \begin{vmatrix} \dfrac{1}{r_s'} + \dfrac{1}{r_{b'e}} & -\dfrac{1}{r_{b'e}} \\[2ex] -\dfrac{1}{r_e} - \dfrac{1}{r_{b'e}} & \dfrac{1}{r_e} + \dfrac{1}{R_E} + \dfrac{1}{r_{b'e}} \end{vmatrix}$$

$$\text{and } G_V = \frac{V_0}{V_S} = \frac{\dfrac{1}{r_s}\left[\dfrac{1}{r_e} + \dfrac{1}{r_{b'e}}\right]}{\dfrac{1}{r_s}\left[\dfrac{1}{r_e} + \dfrac{1}{R_E} + \dfrac{1}{r_{b'e}}\right] + \dfrac{1}{r_{b'e} \cdot R_E}} \tag{6.5·1}$$

$$\text{where} \quad g_m \approx \frac{1}{r_e}$$

$$r_s' = r_s \parallel R_B$$

If $r_s \ll R_B$, then $r_s' \approx r_s$ and the eq. (6.5.1) can be simplified to

$$G_V = \frac{R_E}{R_E + r_e + \dfrac{r_s}{1+\beta}} \tag{6.5.2}$$

$$\text{or} \quad G_V \approx \frac{R_E}{R_E + r_e} < 1 \tag{6.5.3}$$

$$\text{since} \quad \frac{r_s}{1+\beta} \text{ is small}$$

The input impedance R_i to the right of R_B, i.e., without the biasing resistance, is calculated by finding V_B from above node equations and then finding the input current I_i. The input impedence R_i is then found to be

$$R_i = \frac{V_B}{I_i} = r_{b'e} + (1+\beta)\, R_E \tag{6.5.4}$$

$$\text{or } R_i \approx (1+\beta)\, R_E \tag{6.5.5}$$

If the actual input impedence is required then R_B is in parallel with R_i and hence will be smaller than R_i.

The output impedance and current gain of an emitter follower can be similarly calculated as

$$R_0 = \frac{r_{b'e}' + r_s}{1+\beta} \approx r_e \tag{6.5.6}$$

$$\text{and } G_I \approx \beta$$

Example 6.5.1

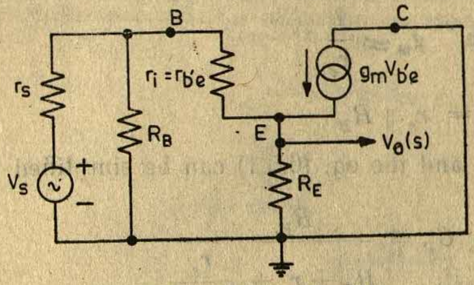
The emitter follower shown in Fig. 6.35 has $I_C = 2$ mA $\beta = 120$, $R_E = 2.7$ KΩ, $R_B = 330$ K Ω, The value of $r_s = 600$ Ω, $R_L = 600$ Ω.

Calculate the gain, input impedance and output impedance of the CC amplifier.

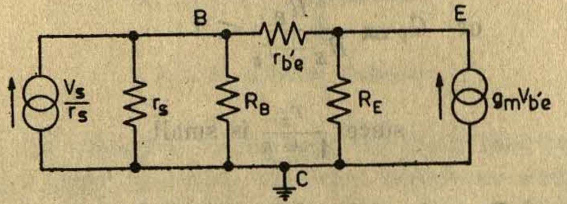
Since $I_C = 2$ mA

$r_e = 12.5$ Ω

$r_{b'e} = \beta\, r_e = 1.5$ KΩ



(a) Equivalent circuit



(b) Circuit redrawn

Fig. 6.35 Equivalent circuit for the analysis of the *CC* amplifier

Gain from eq. (6.5.3) is

$$G_V = \frac{2.7 \times 10^3}{2.7 \times 10^3 + 12.5}$$

$$\text{or } G_V = 0.995$$

R_i from eq. (6.5.5) is

$$R_i = 1.5 \times 10^3 + 121 \times 2.7 \times 10^3$$
$$= 328 \text{ K}\Omega$$

This resistance is in parallel with $R_B = 330$ KΩ hence the actual input impedance seen by the signal source will be 165 K Ω only.

The output impedance $\simeq$ 12.5 Ω

Review Questions

6.1. Distinguish between class A, B and C amplifiers.

6.2. What is thermal runaway ? How is it prevented ?

6.3. What is the variation of I_{CO} and V_{BE} with temperature ?

6.4. How does a resistance in the emitter circuit stabilise the operating point ?

6.5. Define S. What are the units of $S_{I_{CO}}$, S_β and $S_{V_{BE}}$?

6.6. What will happen if the emitter resistance is left unbypassed ? Will it effect the stability of the amplifier ?

6.7. Why are the capacitors C_1 and C_2 used in the circuit of Fig. 6.7 ?

6.8. Which out of the capacitances C_1, C_2 and C_E dominate the low frequency response of the CE amplifier ?

6.9. Distinguish between the internal and the external gain of an amplifier.

6.10. What is $r_{bb'}$? Distinguish between $r_{bb'}$ and $r_{b'e}$.

6.11. What is the phase difference between the input and the output signal at the lower 3dB cut-off frequency of the CE amplifier ?

6.12. What is Miller's theorem ?

6.13. Is the upper 3dB cut-off frequency of a CE amplifier solely governed by the parameters of the transistor ?

6.14. At what rate does the response in a CE amplifier at high frequencies fall ?

6.15. Does the output lag behind the input in phase at high frequencies ?

6.16. What are the limitations of self bias in a FET amplifier ?

6.17. What are the advantages of the modified biasing arrangement in the FET circuit ?

6.18. It is said that the gain of the CD amplifier is normally much less than the CE amplifier. What may be the reason ?

6.19. What limits the input impedance of a FET amplifier ?

6.20. Since the gain of an emitter follower is less than unity, what is the necessity of using this circuit.

6.21. Is the output impedance of an emitter follower dependent upon (i) collector current (ii) source resistance ?

6.22. Will the input impedance of an emitter follower be effected by the loading at the output of the circuit ?

Problems

P 6.1 An amplifier has a d.c. power supply of 15 volts and draws a current of 10 mA. It produces an output of 5 volts peak across a load resistance of 600 Ω for a signal frequency of 1 KHz. Calculate the a.c. power output and the efficiency of the amplifier.

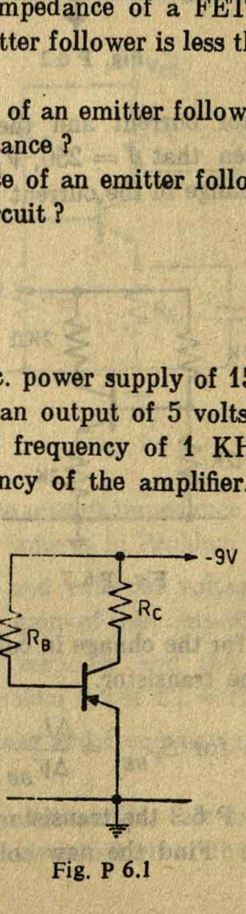


Fig. P 6.1

P 6.2 In the *pnp* Germanium transistor biasing circuit shown in Fig. P 6.1, calculate the values of R_C and R_B to obtain an operating point of $V_{CE} = -4V$ and $I_C = 1$ mA. It is given that $\beta = 120$.

P 6.3 In the biasing circuit of Fig. P 6.2, it is desired to have a $S_{I_{CO}} = 6$ and $I_C = 1$ mA with $V_{CE} = -4$ volts. Assume $I_{CO} = 1\mu A$ $V_{BE} = .3V$ and $\beta = 100$. Prepare a table of the possible combinations of R_E, R_B and R_C values. Now if the temperature changes by 60 °C, Calculate the percentage change of collector current in each case. (Select at least four combination of resistances over the whole range).

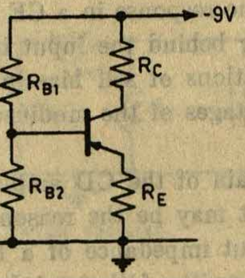


Fig. P 6.2

P 6.4 Calculate the collector current and the drop V_{CE} for the circuit in Fig. P 6.3. It is given that $\beta = 250$, $V_{BE} = 0.7$ V and $I_{CO} = 0.01$ µA at 20°C. Find the change in the current if the temperature rises to 80°C.

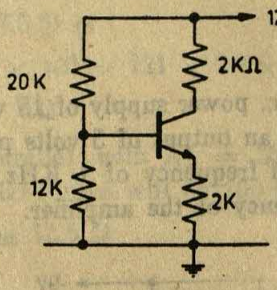


Fig. P 6.3

P 6.5 Derive an expression for the change in collector current ΔI_C for a change $\Delta\beta$ in the beta of the transistor.

P 6.6 Derive an expression for $S_{V_{BE}} = \frac{\Delta I_c}{\Delta V_{BE}}$. What are the units of $S_{V_{BE}}$?

P 6.7 In the circuit of Fig. P 6.3 the transistor is replaced with another transmitor whose β is 80. Find the new collector current.

P 6.8 A biasing arrangement is shown in Fig. P 6.4. It is required that $I_C = 2$ mA and $V_{CE} = 5$ volts. Find the values of R_C and R_B. Given $\beta = 100$, $V_{BE} = .7$ V. Neglect I_{CO}

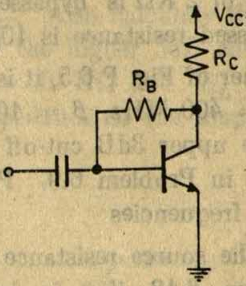


Fig. P 6.4

P 6.9 In the amplifier of Fig. P 6.5, calculate the midband voltage gain and current gain, both internal and external. The circuit values are $R_C = 3.3\text{K}\Omega$, $R_E = 2\ \text{K}\Omega$, $R_{B1} \,||\, R_{B2} = 6\ \text{K}\Omega$, $R_L = 1\text{K}\Omega$ $r_s = 100\ \Omega$ and $I_C = 2$ mA.

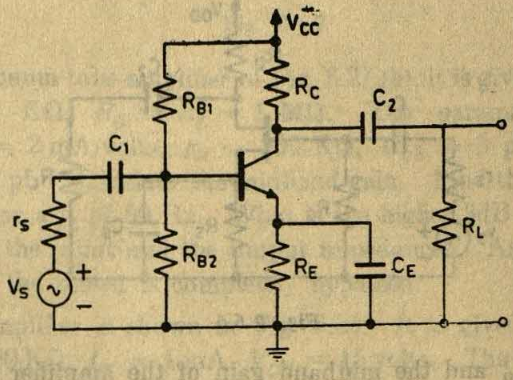


Fig. P 6.5

P 6.10 Find the input and the output impedance of the amplifier in Fig. P 6.5 with the circuit values same as in Problem 6.9. What is the power gain ?

P 6.11 Calculate the internal and external voltage gains in the Problem 6.9 if r_s is 1 K Ω. Can the gain of this amplifier be made 200 ?

P 6.12 Find the low frequency response and the lower 3dB cut off frequency of the amplifier in Problem 6.9 if $C_1 = C_2 = 10\ \mu f$ and $C_E = 500\ \mu f$.

P 6.13 Draw the complete phase and frequency response at low frequencies for the Problem 6.12.

P 6.14 Assuming C_E and C_2 to be infinite, calculate the low frequency response of the amplifier in Problem 6.9 given that $C_1 = 1\ \mu f$.

P 6.15 Repeat the Problem 6.14 with $C_1 = C_E = \infty$ and $C_2 = 1\ \mu f$.

P 6.16 Assuming $C_1 = C_2 = \infty$, plot the low frequency response of the amplifier in Problem 6.9 with $C_E = 100\ \mu f$.

P 6.17 In the Problem 6.9, R_E of 2 KΩ is bypassed partially only. Calculate the gain if the unbypassed resistance is 100 Ω.

P 6.18 In the transistor amplifier of Fig. P 6.5, it is given that the parameters of the transistor are $f_T = 400$ MHz, $\beta = 100$, $r_{bb'} = 60\ \Omega$, $C_{b'c} = 3pf$. Find $f_{B'}$, $C_{b'c}'$ and the upper 3dB cut-off frequency f_H. The circuit values are the same as in Problem 6.9. Plot the frequency and phase response at the higher frequencies

P 6.19 What is the effect of the source resistance r_s on the upper 3dB cut-off frequency? In Problem 6.18, if r_s is increased to 1 KΩ, calculate the change in the f_H.

P 6.20 The self bias circuit of Fig. P 6.6 has $V_{DD} = 18$ V $V_P = -4$ V, I_{DSS}=8 mA. It is desired to have a drain current of 1 mA. Find values of R_S, R_D and R_G if the input impedance has to be larger then 200 KΩ and $V_{DS} = 5$ V.

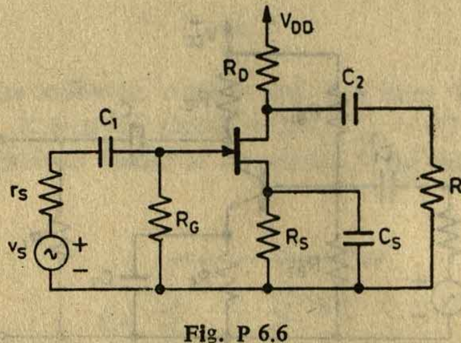


Fig. P 6.6

P 6.21 Find the g_m and the midband gain of the amplifier of Problem 6.20 if $R_L = 500$ KΩ, and $r_s = 10$ KΩ. Does the value of r_s have much effect on the gain of the amplifier?

P 6.22 In the Problem 6.20 draw the transfer characteristic assuming it to be absolutely linear, Draw the biasing line corresponding to R_S on this characteristic and locate the operating point. Estimate graphically the change in I_D if V_P and I_{DSS} change by ± 25% due to device-to-device variation.

(Hint : See Fig. P 6.7)

P 6.23 The variations of the FET in an amplifier are as given in Problem 6.22. A drain current of 4 mA with $V_{GS} = -2$ V is desired as the operating point. The operating point may not change by more than ± 5%. Calculate the values of R_D, R_S, R_{G1} and R_{G2}.

P 6.24 In the FET amplifier of Fig. P 6.7 it is given that $V_P = -2.5, I_{DSS}=4$ mA, $I_D = 2$ mA, $V_{DS} = 4$ V, $V_{DD} = 15$ V. The parameters of the device are $r_d = 200$ KΩ, $C_{gd} = C_{gs} = 2\ pf$ and $C_{ds} = 10\ pf$. The stray capacitances at the input and output ports are 5 *pf* each. Find the values of R_D, R_S, R_{G1}, R_{G2}. Also calculate the values of C_1, C_2 and C_S for a $f_L = 50$ Hz. Find the higher 3dB cut-off frequency and the midband gain. Assume $r_s = 10$ KΩ and $R_L = 200$ KΩ What is the input and the output impedance of the amplifier ?

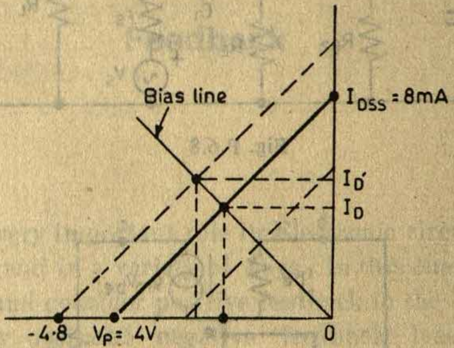


Fig. P 6.7

P 6.25 In the vacuum tube amplifier of Fig. 6.27 (b), it is given that $R_K = 2$ KΩ, $R_A = 47$ KΩ, $R_G = R_L = 1$ MΩ. The parameters of the tube are $g_m = 2$ mA/volts, $r_P = 200$ KΩ, $C_{gk} = 3$ pf, $C_{gp} = 1$ pf and $C_{pk} = 3$ pf. Calculate the midband gain. Find the values of C_1, C_2 and C_K for a f_L of 50 Hz. What is the higher 3dB cut off frequency ? Estimate the input and the output impedances. Assume $r_s = 10$ k Ω, and that the screen is completely bypassed.

P 6.26 A CC amplifier is shown in Fig. 6.34. It is given that $R_E = 5$ KΩ, $R_B = 250$ KΩ, $I_C = 1$ mA, $V_{CC} = 15$ volts. The transistor parameters are $\beta = 200, f_T = 250$ MHz, $r_{bb'} = 50$ Ω, $C_{b'c} = 5$ pf, $r_O = 80$ KΩ. If the source resistance $r_{bb}' = 50$ Ω and $R_L = 1$ KΩ, calculate the midband gain and the input impedance of the amplifier. What is the output impedance ? Estimate the change in the input impedance if the R_L is 50 Ω . Will the output impedance be effected if $r_s = 600$ Ω ?

P 6.27 Find the frequency response i.e., the upper 3dB frequency of the CC amplifier in Problem 6.26 with $r_s = R_L = 500$ Ω.

P 6.28 A common base amplifier is shown in Fig. P 6.8. Assuming $I_C = 1$ mA and $R_C = R_E = 2$ KΩ, $R_{B1} = 20$ KΩ, $R_{B2} = 12$ KΩ, $V_{CC} = 12$ volts, calculate the midband gain. The transistor parameters are $\beta = 150$, $r_O = 80$ KΩ. Assume that r_{bb}' is negligible. Find the input and the output impedance.

[Hint: Draw the equivalent circuit and ground the base as shown in Fig. P 6.9.]

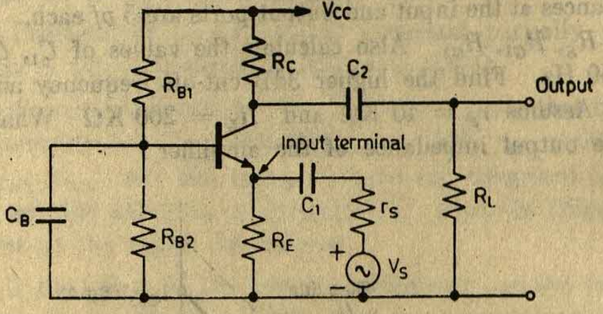


Fig. P 6.8

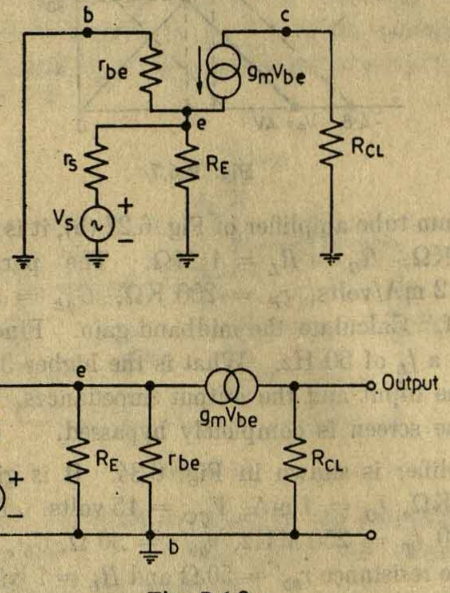


Fig. P 6.9

7

Feedback

7.0 Introduction

Feedback plays a very important role in Electronic circuits and is employed for a variety of reasons and in a variety of ways. In this chapter we shall discuss negative feedback only and consider positive feedback in the chapter on waveform generators. A properly designed negative feedback leads to a significant improvement in the performance of the circuit. Feedback is, sometimes, unavoidable as in the case of feedback through parasitic capacitances etc., but in most cases it is introduced deliberately to obtain some desirable features. Feedback reduces an amplifier's sensitivity to the variations of the active device parameters, it reduces the harmonic distortion and noise output of an amplifier and also increases its bandwidth. Large amount of feedback though, introduces the possibility of instability and oscillations. This is a serious drawback of negative feedback in amplifiers and requires a careful approach to its design and implementation.

An analysis of negative feedback amplifiers can be carried out using different techniques but the equivalent circuit method brings out some important effects of feedback and has been used here. Advantages and disadvantages of negative feedback have been discussed followed by an analysis of the four typical configurations.

7.1 Principles of Feedback

It is always a requirement of an amplifier that it reproduces the input signal faithfully. If ideal circuit elements including active devices are available without any limitations then any linear amplifier will be adequate and feedback will not be necessary. It is only when we have to use non-ideal circuit elements and devices that negative feedback becomes essential and we hope to build an amplifier with feedback which will be satisfactory. Consider the block diagram of an amplifier with feedback as shown in Fig. 7.1. It consists of the amplifier in the forward path and a feedback network through which a portion of the output is fedback to the

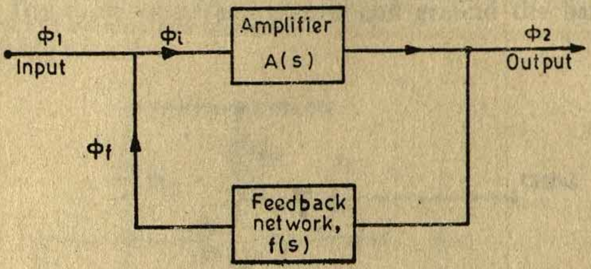


Fig. 7.1 General feedback

input. This forms what is called a feedback loop. If the loop is opened such that $\phi_f = 0$, then the forward gain function of the amplifier is given as

$$A(s) = \frac{\phi_2}{\phi_i} = \frac{\phi_2}{\phi_1}\Bigg|_{\phi_f = 0} \tag{7.1}$$

Here the ϕ term has been used to indicate either voltage V or current I as the input and the output parameter.

We shall assume that the amplifier is unilateral and the reverse transmission from the output to the input is zero. Similarly it is assumed that the forward transmission through the feedback network is zero. The feedback function $f(s)$ is defined as

$$f(s) = \frac{\phi_f}{\phi_2} \tag{7.2}$$

Ideally, therefore, the signal flows in certain directions only as shown by the arrows in Fig. 7.1. The gain of the amplifier with the loop connected is defined as $A_f(s)$ and is given by

$$A_f(s) = \frac{\phi_2}{\phi_1} \tag{7.3}$$

Now $\phi_1 + \phi_f = \phi_i$ as seen in the Fig. 7.1. Thus, substituting equations (7.1) and (7.2) in (7.3) we get

$$A_f(s) = \frac{\phi_2}{\phi_1} = \frac{\phi_2}{\phi_i - \phi_f} = \frac{\phi_2}{\dfrac{\phi_2}{A(s)} - f(s).\phi_2}$$

$$\text{or} \quad A_f(s) = \frac{A(s)}{1 - A(s).\,f(s)} \tag{7.4}$$

We see that the gain with feedback is a modified function of $A(s)$, the gain without feedback. The modification factor $|1\text{-}A(s).\,f(s)|$ plays a very important role in the analysis and design of feedback amplifiers. If $|[1\text{-}A(s).\,f(s)]|$ is greater than unity then the feedback is a negative feedback, whereas if it is smaller than unity then the feedback is called a positive feedback.

$[1\text{-}A(s).f(s)]$ is called the feedback factor $F(s)$ and indicates the amount by which the gain of the amplifier is reduced after feedback. The term $[A(s).f(s)]$ is defined as the loop transmission function $T(s)$. Thus

$$A_f(s) = \frac{A(s)}{1-A(s).f(s)} = \frac{A(s)}{1-T(s)} = \frac{A(s)}{F(s)} \tag{7.5}$$

For a negative feedback circuit, the gain $A_f(s) < A(s)$ and hence $T(s)$ must necessarily be negative. This means that either $A(s)$ is negative or $f(s)$ is negative. Now when the magnitude of $T(s)$ is much larger than unity, then eq. (7.5) can be simplified to

$$A_f(s) = -\frac{1}{f(s)} \tag{7.6}$$

This shows that $A_f(s)$ is only dependent upon the feedback function $f(s)$ and is independent of $A(s)$. In other words if the feedback network consists of passive elements only the gain depends upon them and is not effected by the active device nonlinearities and parameter variations.

The assumption of unilateral transmission through the amplifier and the feedback network is obviously an ideal one and in practice the signal flow in the other direction is not negligible. Parasitic capacitances in active devices allow some signal flow from the output to the input. Similarly since the feedback network is a passive one there is an equal amount of signal flow in both directions, and the assumption of zero forward transmission is invalid. However, if the forward transmission of the amplifier is much larger than the forward transmission of the feedback network and the reverse transmission of the feedback network is much larger than the reverse transmission of the amplifier, then the assumption regarding the flow of the signal in Fig. 7.1 is practically valid.

7.2 Advantages and Disadvantages of Feedback

As mentioned earlier, the negative feedback in amplifiers makes them less sensitive to parameter variations of the active devices, reduces distortion and noise output, affords a control over the input and output terminal impedances and increases the bandwidth of the amplifier. We must remember that all the above quantities are affected simultaneously when the feedback is employed and the control of one quantity alone, say impedance, cannot be achieved without affecting other quantities say the gain and bandwidth.

7.2.1 DESENSITIVITY TO PARAMETER VARIATIONS

We have seen that if the loop transmission $T(s)$ is large compared to unity then the gain of the amplifier depends only on $f(s)$, eq (7.6). This certainly is a very attractive feature of the amplifier—particularly so in a transistor amplifier. First of all the gain of the transistor amplifier is normally high and reduction in gain through feedback is desirable in many cases from this view point only. Secondly the transistors are much more affected by the environmental conditions, manufacturing tolerances and quiescent point variation etc. and a negative feedback makes the amplifier less sensitive to these. In fact with the advent of IC technology very large gain amplifiers called operational amplifiers are marketed and the user obtains the desired gain by utilising negative feedback across the amplifier. As shown by eq.(7.6) the gain now depends upon the passive network only.

Quantitatively the sensitivity of the overall gain A_f to the variation of a particular parameter K is defined as

$$S_K = \frac{\partial A_f/A_f}{\partial K/K} \qquad (7.7)$$

It is the ratio of percentage change in A_f to a percentage change in the parameter K. For example, the change in A_f due to a change in A will be obtained as

$$S_A = \frac{\partial A_f/A_f}{\partial A/A}$$

From eq. (7.4)

$$S_A = \frac{1}{1-A.f} = \frac{1}{F} \qquad (7.8)$$

$A(s)$ and $f(s)$ etc. have been written as A and f for simplificity in eq. (7.8). Eq. (7.8) can be also be rewritten as

$$\frac{\partial A_f}{A_f} = \frac{1}{F} \cdot \frac{\partial A}{A} \qquad (7.9)$$

Eq. (7.9) clearly shows that the percentage change in A_f will be $\frac{1}{F}$ times the percentage change in the open loop gain function A. Let us suppose, for example, that the feedback factor F is 25 in a transistor amplifier. The gain A of the amplifier changes by 20% due to a change in the h_{fe} of the transistor. The change in gain A_f after feedback will only be 0.8%—a remarkable improvement.

7.2.2 REDUCTION OF NOISE AND DISTORTION

Distortion due to nonlinearity of the active devices, power supply ripple voltage and disturbance due to the noise generated inside the amplifiers active devices etc. are reduced by the application of negative feedback. At this stage we must remember a very important point connected with the reduction of noise. Any noise which is introduced at the input of the amplifier is treated like a signal by it and both the signal and the noise are amplified equally by the amplifier. Thus, the ratio of signal to noise remains the same at the input and the output. To illustrate a case where the noise (or distortion) is reduced by the action of negative feedback, let us consider the two stage amplifier shown in Fig. 7.2.

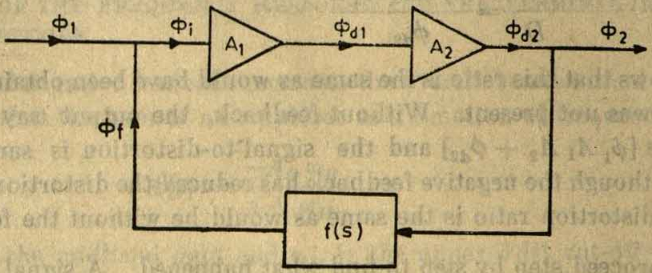


Fig. 7.2 Noise and Distortion in an Amplifier

We shall assume that distortion is introduced both at the output of the first as well as the second amplifier and is designated as ϕ_{d1} and ϕ_{d2}. For all practical purposes we can say that A_1 and A_2 are perfect and that ϕ_{d1} and ϕ_{d2} are noise or distortion sources connected externally as if. The gain function is derived as follows. The output signal ϕ_2 in terms of ϕ_1 is

$$\phi_2=\phi_1 \cdot \frac{A_1A_2}{1-(A_1A_2)f}+\phi_{d1}\frac{A_2}{1-(A_1A_2)f}+\phi_{d2}\frac{1}{1-(A_1A_2).f} \tag{7.10}$$

If we assume that $|(A_1A_2).f| \gg 1$, then Eq. (7.10) reduces to

$$\phi_2=-\frac{\phi_1}{f}-\frac{\phi_{d1}}{A_1 . f}-\frac{\phi_{d2}}{(A_1A_2) . f} \tag{7.11}$$

We notice from eq. (7.11) that ϕ_{d2} is reduced by a factor of $(A_1A_2.f)$ while ϕ_{d1} is only reduced by a factor of A_1f. The amount of reduction in the distortion or noise depends very much on the origin of the disturbing signal. Since in most of the amplifiers the nonlinear distortion is introduced when the signal level is high, the distortion will predominantly be contributed by the last stage at the output of the amplifier. In such cases we can say that the distortion is reduced by a factor F in a negative feedback amplifier. It is also obvious from eq. (7.11) that any noise or distortion introduced along with ϕ_1 is not reduced at all and is amplified by a factor $(1/f)$—the same as the signal.

Another very interesting feature of the negative feedback is that no improvement due to feedback will occur if the input signal level before and after feedback is kept the same. Let us illustrate the point by assuming that ϕ_{d1} is zero in Fig. 7.2 and the output is obtained from eq. (7.10) as

$$\phi_2=\phi_1\frac{A_1A_2}{1-A_1A.f}+\phi_{d2} \cdot \frac{1}{1-A_1A_2f} \tag{7.12}$$

The first term on the right hand side of eq. (7.12) is the signal part S and the second term is the distortion part D at the output of the amplifier. The ratio of signal-to-distortion at the output is

$$\frac{S}{D}=\frac{\phi_1 . A_1 A_2}{\phi_{d2}} \tag{7.13}$$

Eq. (7.13) shows that this ratio is the same as would have been obtained even when the feedback was not present. Without feedback, the output say ϕ_2 for an input of ϕ_1 is $[\phi_1 A_1 A_2+\phi_{d2}]$ and the signal-to-distortion is same as in eq. (7.13). Even though the negative feedback has reduced the distortion, we find that the signal-to-distortion ratio is the same as would be without the feedback.

Let us proceed step by step to find what happened. A signal ϕ_1 is applied to the amplifier of gain $(A_1 A_2)$. The signal output is $\phi_1 . A_1A_2$, the distortion is d_2 and total output is ϕ_2. Now a negative feedback is applied and the overall output goes down to ϕ'_2. The signal and distortion components are as indicated in eq. (7.12). Now, if the input ϕ_1 is increased such that $\phi_2=\phi_2'$ again, then the signal component is approximately $\phi_1 A_1 A_2$ and the distortion component is $\phi_{d2}/(1-A_1A_2 f)$ and their ratio is

$$\frac{S}{D}\approx\frac{\phi_1 A_1 A_2(1-A_1 A_2 f)}{\phi_{d2}}$$

$$\approx\frac{\phi_1 A_1 A_2}{\phi_{d2}} . F \tag{7.14}$$

Thus the signal-to-distortion improves by a factor F only if $\phi_2=\phi_2'$ or in other words the input is increased by an amount F after the feedback is applied.

Example 7.2.1

An amplifier using transistors has an input of 10 mV and a gain of 200 without feedback. The distortion produced at the output is 10%. It is desired to reduce the distortion to 1% by negative feedback. Calculate the gain and the input and the output voltages.

Signal input = 10 mV
Gain = 200
Therefore, signal output = 200 × 10 = 2 V
Distortion = 10% = 0.2 V

The distortion is to be reduced to 1%, therefore,

$$F=\frac{0.2}{0.02}=10$$

With $F=10$, the signal output becomes 0.2 V. Thus the signal output is 0.2 V and the distortion output is 0.02 V.

The percentage distortion is still 10%. Now we increase the input from 10 mV to 100 mV. The signal output will be 2 V but the distortion will remain at 0.02V and hence the distortion has reduced to 1%.

7.2.3 EFFECT OF THE FREQUENCY RESPONSE AND THE TERMINAL IMPEDANCE OF THE AMPLIFIER

The use of negative feedback increases the overall bandwidth of an amplifier. Let us assume that the gain of an amplifier as a function of frequency is given as

$$A(s) = \frac{-A_O\,\omega_H}{s + \omega_H} \tag{7.15}$$

where $-A_O$ is the midband gain and ω_H is the upper 3 dB cut-off frequency as derived in chapter VI. Let us further assume that $f(s)$ is not frequency dependent and is simply given as f_O. Thus, the gain with feedback from eq. (7.15), is

$$A_f\,(s) = \frac{-A_O\,\omega_H/(s+\omega_H)}{1 + A_O\,\omega_H.\,f_O/(s+\omega_H)}$$

or

$$A_f\,(s) = \frac{-A_O\,\omega_H}{s + (1 + A_O\,f_O).\,\omega_H} \tag{7.16}$$

The new upper 3db breakpoint is at $(1 + A_O f_O)\,\omega_H$ or $F.\omega_H$, an increase by F times over the previous value.

It can be shown similarly that the lower 3db break point is reduced by the negative feedback and thereby the bandwidth is increased. The frequency response with and without feedback is shown in Fig. 7.3 As seen the overall bandwidth increases by using negative feedback.

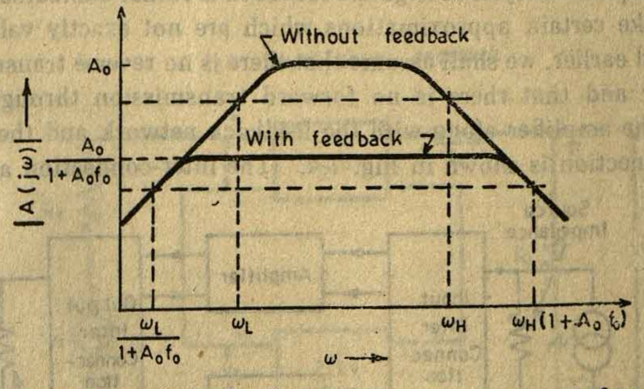


Fig. 7.3 Effect of Negative feedback on the frequency response of an amplifier

Negative feedback helps us to modify the terminal impedances at the input and the output ports in any given direction. For example the input impedance can either be increased or decreased depending upon the way the feedback loop is closed. Similarly the output impedance can also be increased or decreased by feedback. We shall discuss the details in the next section.

The use of negative feedback helps us to realise transfer functions which cannot be realised by RC elements alone. RC networks in combination with amplifiers using feedback are extensively used for shaping the response of amplifiers and making active filters.

7.2.4 DISADVANTAGES OF NEGATIVE FEEDBACK

We have seen that negative feedback gives a lot of advantages in terms of desensitivity to parameter variations, noise, a better control over the frequency response and the terminal impedances. The price paid for all this is sometimes quite exacting. A serious problem encountered in the use of negative feedback is the introduction of instability in the amplifier. It is clear from Fig 7.1 and Eq. (7.4) that there has to be a phase shift of 180° between ϕ_1 and ϕ_f when a negative feedback is desired. Now both the amplifier and the feedback networks are frequency sensitive and unwanted phase shifts may occur at the extremes of the frequency band. It may so hapen that at frequencies much higher or lower than the passband there is an extra phase shift of 180°, with the result that the input and the feedback signal are in the same phase. If the gain of the amplifier is more than unity at this juncture the amplifier will burst into self oscillations. Thus one has to be very careful while designing or making an amplifier with feedback and ensure that the feedback does not become positive while the loop gain is more than unity. Oscillators discussed in chapter XI require a positive feedback with a loop gain more than unity to start building up the oscillations.

7.3 Types of Feedback

The complete analysis of negative feedback is rather cumbersome and tedious. We shall make certain approximations which are not exactly valid all the time. As mentioned earlier, we shall assume that there is no reverse transmission through the amplifier and that there is no forward transmission through the feedback network. The amplifier along with the feedback network and the input and output port connection is shown in Fig. 7.4. The inter-connection at the input and

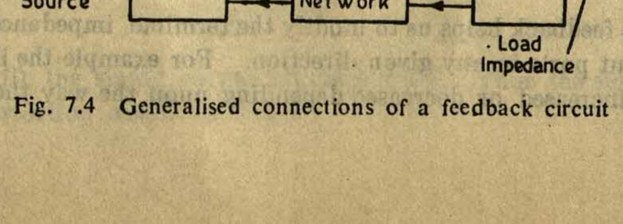
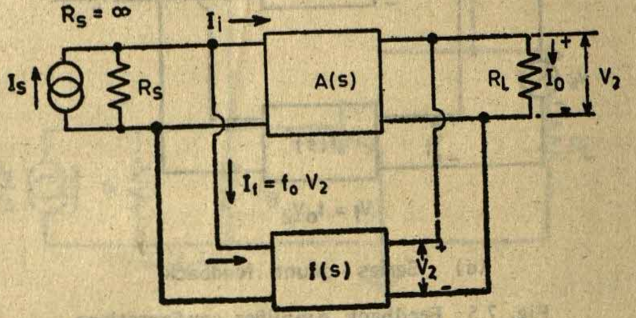


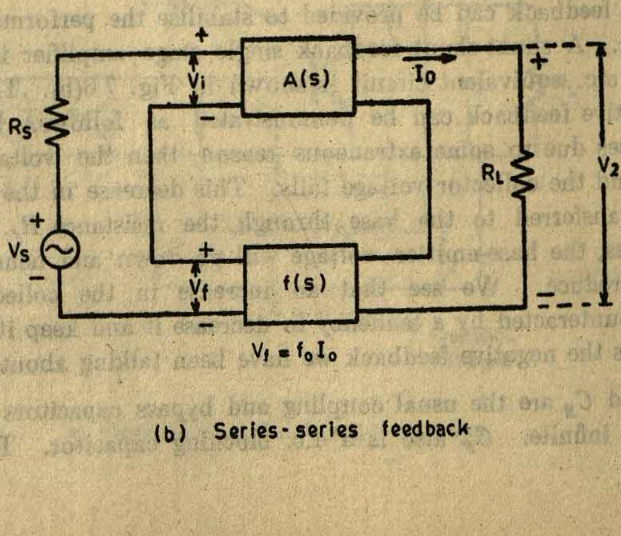
Fig. 7.4 Generalised connections of a feedback circuit

the output ports can either be series or parallel. The source ϕ_1 can either be a current source or a voltage source. The source and load impedances shown could be resistive as a simple assumption. For the generalised amplifier of Fig. 7.4 four interconnections at the input and the output ports are possible. For example in Fig. 7.5(a) the input ports of the amplifier and the feedback network are connected in parallel and at the same time the output ports are also connected in parallel. The configuration is called the shunt-shunt connection. The connection in Fig. 7.5(b) is a series-series feedback since both the ports at the input and the output are in series. Now in Fig. 7.5(c) the input ports are in shunt but the output ports are in series and hence this is known as the shunt-series feedback. Finally in Fig. 7.5(d) the interconnection makes it a series-shunt feedback.

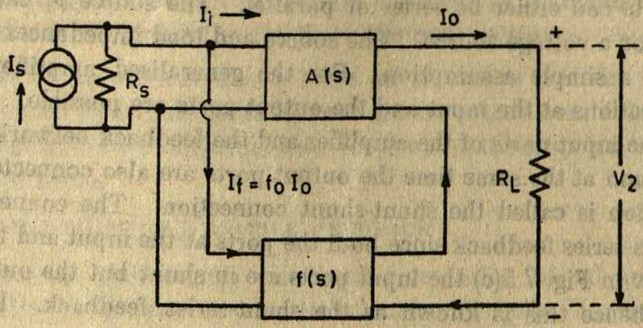
The amplifier in Fig. 7.5(a) is also called voltage output-shunt input feedback amplifier because the feedback voltage is proportional to the voltage at the output port and is connected in shunt at the input. In the same way, the amplifiers in Fig. 7.5(b), (c) and (d) are known as current-series, current-shunt and voltage-series feedback amplifiers respectively



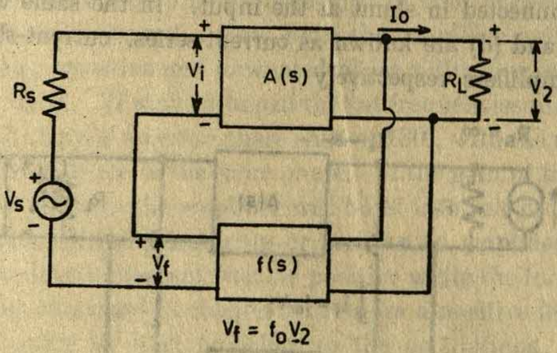
(a) Shunt-shunt feedback



(b) Series-series feedback



(c) Shunt-series feedback



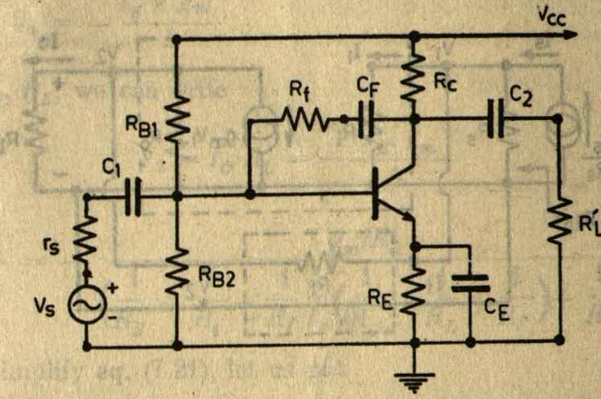
(d) Series - shunt feedback

Fig. 7.5 Feedback Amplifier configurations

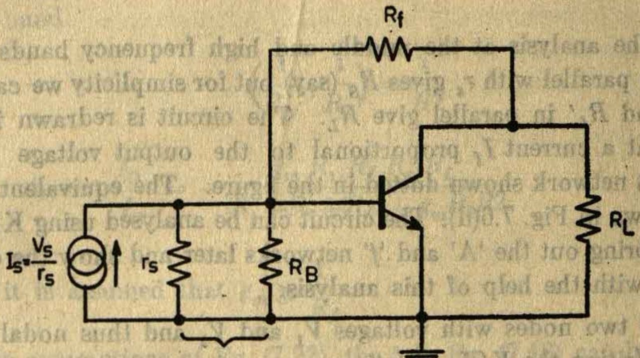
7.4 Shunt-Shunt Amplifier

Negative feedback can be provided to stabilise the performance of a single stage amplifier. A shunt-shunt feedback single stage amplifier is shown in Fig. 7.6(a) and its a.c. equivalent circuit is shown in Fig. 7.6(b). That this circuit produces negative feedback.can be demonstrated as follows. If the collector current increases due to some extraneous reason, then the voltage drop across R_C increases and the collector voltage falls. This decrease in the voltage at the collector is transferred to the base through the resistance R_f. Once the base voltage reduces, the base-emitter voltage will go down and hence the collector currrent will reduce. We see that an increase in the collector current is immediately counteracted by a tendency to decrease it and keep it under control. This in effect is the negative feedback we have been talking about.

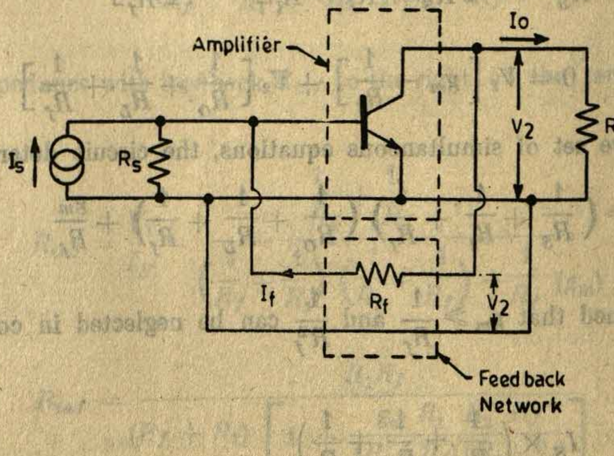
C_1, C_2 and C_E are the usual coupling and bypass capacitors and have been assumed to be infinite. C_F also is a d.c. blocking capacitor. These capacitors



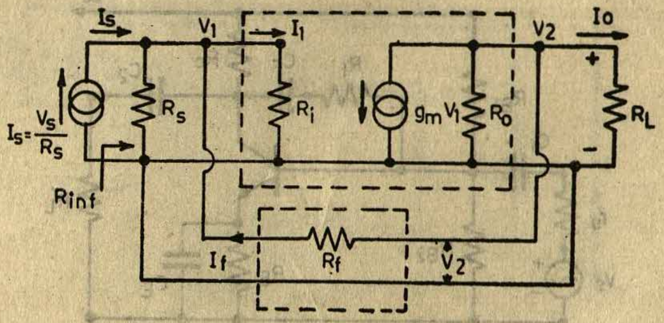
(a) Actual circuit



(b) AC Equivalent circuit



(c) Seperation of the A and f networks



(d) Complete equivalent circuit

Fig. 7.6 Shunt-shunt negative feedback single stage CE amplifier

do not effect the analysis at the middle and high frequency bands of operation. R_{B1} and R_{B2} in parallel with r_s gives R_S (say) but for simplicity we can assume that $r_s \approx R_S$. R_C and R_L' in parallel give R_L. The circuit is redrawn in Fig. 7.6(c) and we see that a current I_f proportional to the output voltage V_2 is fedback through the $f(s)$ network shown dotted in the figure. The equivalent circuit of the amplifier is drawn in Fig. 7.6(d). The circuit can be analysed using KCL equations. We shall also bring out the 'A' and 'f' networks later and show the direct method of calculation with the help of this analysis.

There are two nodes with voltages V_1 and V_2 and thus nodal analysis will be simpler. Writing the KCL equations

$$I_S = \frac{V_S}{R_S} = V_1\left[\frac{1}{R_S} + \frac{1}{R_f} + \frac{1}{R_i}\right] - V_2\left[\frac{1}{R_f}\right] \tag{7.17.a}$$

$$0 = V_1\left[g_m - \frac{1}{R_f}\right] + V_2\left[\frac{1}{R_O} + \frac{1}{R_L} + \frac{1}{R_f}\right] \tag{7.17b}$$

Solving the above set of simultaneous equations, the circuit determinant Δ is

$$\Delta = \left(\frac{1}{R_S} + \frac{1}{R_i} + \frac{1}{R_f}\right)\left(\frac{1}{R_O} + \frac{1}{R_L} + \frac{1}{R_f}\right) + \frac{g_m}{R_f} \tag{7.18}$$

where it is assumed that $g_m \gg \frac{1}{R_f}$ and $\frac{1}{R_f^2}$ can be neglected in comparison.

Hence

$$V_1 = \frac{I_S \times \left(\frac{1}{R_O} + \frac{1}{R_L} + \frac{1}{R_f}\right)}{\Delta} \tag{7.19}$$

and $$V_2 = -\frac{I_S \times g_m}{\Delta} \tag{7.20}$$

Since $V_2 = I_O R_L$, we can write

$$V_2 = I_O R_L = -\frac{I_S \cdot g_m}{\Delta}$$

or $$\frac{I_O}{I_S} = -\frac{g_m/R_L}{\left(\frac{1}{R_S}+\frac{1}{R_i}+\frac{1}{R_f}\right)\left(\frac{1}{R_O}+\frac{1}{R_L}+\frac{1}{R_f}\right)+\frac{1}{R_f}(g_m)} \tag{7.21}$$

In order to simplify eq. (7.21), let us put

$$\left(\frac{1}{R_S}+\frac{1}{R_i}\right)=\frac{1}{R_1}$$

and $$\tag{7.22}$$

$$\left(\frac{1}{R_O}+\frac{1}{R_L}\right)=\frac{1}{R2}$$

Hence $$A_{if} = \frac{I_O}{I_S} = -\frac{g_m R_1 R_f R_2/R_L}{R_1+R_2+R_f+g_m R_1 R2} \tag{7.23}$$

where again it is assumed that $g_m \gg \frac{1}{R_f}$

In view of the assumptions of Eq. (7.22), the Δ in Eq. (7.18) can be rewritten as

$$\Delta = \left(\frac{1}{R_f}+\frac{1}{R_1}\right)\left(\frac{1}{R_2}+\frac{1}{R_f}\right)+\frac{1}{R_f}(g_{in})$$

The input impedance with feedback R_{inf} to the right of the terminal (1,1) is $\frac{V_1}{I_S}$.

Hence

$$R_{inf} = \frac{V_1}{I_S} = \frac{\frac{1}{R_2}+\frac{1}{R_f}}{\left(\frac{1}{R_f}+\frac{1}{R_1}\right)\left(\frac{1}{R_2}+\frac{1}{R_f}\right)+\frac{1}{R_f}(g_m)}$$

or $$R_{inf} = \frac{R_1 R_f}{(R_f+R_1)\left[1+\frac{g_m R_1 R_2 R_f}{(R_1+R_f)(R_2+R_f)}\right]} \tag{7.24}$$

If we can assume that $R_1 + R_f \simeq R_f$

then

$$R_{inf} \simeq \frac{R_1}{1 + \dfrac{g_m R_1 R_2}{(R_2 + R_f)}} \tag{7.25}$$

It should be noted that R_1 is the input impedance without feedback. The Eq. 7.24 can also be written as

$$R_{inf} = \frac{R_1'}{1 + \dfrac{g_m R_1' R_2}{(R_2 + R_f)}}$$

when R_1' is the parallel combination of R_1 and R_f. If $R_1' \simeq R_1$ then Eq. (7.25) follows. We thus find that the input impedance of a shunt-shunt feedback amplifier is less than that of the amplifier without feedback.

The output impedance can be found by connecting a voltage source across the output terminals 2-2 in Fig. 7.6(d) and making $I_S = 0$,. Proceeding in a similar manner as the input impedance calculation we get,

R_{outf} = output impedance with feedback

$$\text{or} \quad R_{outf} = \frac{\dfrac{1}{R_1} + \dfrac{1}{R_f}}{\Delta} \tag{7.26}$$

Solving Eq. (7.26)

$$R_{outf} = \frac{\dfrac{R_2 R_f}{R_2 + R_f}}{1 + \dfrac{g_m R_1 R_2 R_f}{(R_2 + R_f)(R_1 + R_f)}} \tag{7.27}$$

where $R_2 = R_O \,||\, R_L$ = output impedance without feedback.

If we assume that $(R_1 \,||\, R_f) \simeq R_1$ and $(R_2 \,||\, R_f) \simeq R_2$

then

$$R_{outf} \simeq \frac{R_2}{1 + \dfrac{g_m R_1 R_2 R_f}{(R_2 + R_f)(R_1 + R_f)}}$$

$$\text{or} \quad R_{outf} \approx \frac{R_2}{1 + \dfrac{g_m R_1 R_2}{R_2 + R_f}} \tag{7.28}$$

It should be noted that while deriving eq. (7.26) and hence R_{outf} in eq. (7.28), it has been assumed that R_L is connected while the output impedance is measured or calculated. We thus see that the shunt-shunt feedback reduces the output impedance.

The gain in eq. (7.23) has been derived as a current gain but the eq. (7.20) can be used with equal facility to obtain the voltage gain $\frac{V_2}{V_S}$ by substituting for I_S, as

$$V_2 = \frac{V_S}{R_S} \cdot \left[- \frac{g_m}{\Delta} \right]$$

or

$$\frac{V_2}{V_S} = - \frac{g_m / R_S}{\frac{1}{R_1}\left[\frac{1}{R_2} + \frac{1}{R_f}\right] + \frac{1}{R_f R_2}\left[g_m R_2 + 1\right]}$$

Simplifying

$$\frac{V_2}{V_S} = - \frac{g_m R_1 R_2 R_f / R_S}{R_1 + R_2 + R_f + g_m R_1 R_2} \tag{7.29}$$

In most of the amplifier circuits, it can be assumed that $g_m R_2 \gg 1$ and $R_2 \approxeq R_L$, hence eq. (7.23) and (7.29) can be written as

$$\frac{I_O}{I_S} \approxeq - \frac{g_m R_1 R_f}{R_1 + R_2 + R_f + g_m R_1 R_2} \tag{7.30a}$$

and

$$\frac{V_2}{V_S} = - \frac{g_m R_1 R_2 R_f / R_S}{R_1 + R_2 + R_f + g_m R_1 R_2} \tag{7.30b}$$

Example 7.4.1

The single stage shunt-shunt feedback amplifier shown in Fig. 7.6a, has the following parameters

$$I_C = 2\text{mA}$$
$$h_{fe} = 250$$
$$R_O = 60\ \text{K}\Omega$$
$$R_C \,||\, R_{LI} = R_L = 600\Omega$$
$$r_s \,||\, R_B = R_S = 600\Omega$$
$$R_f = 10\ \text{K}\Omega$$

Calculate the current and voltage gains, input and output impedances with and without feedback.

$$\text{Now } g_m = 40\, I_C$$
$$\text{or } g_m = 80 \times 10^{-3} \text{ mhos}$$
$$R_1 = R_s \,||\, R_i$$
$$= 503\ \Omega$$

$$\text{where} \quad R_i \approx \frac{h_{fe}}{g_m} = \frac{250}{80} \times 10^3 = 3.125\,\text{K}\Omega$$

$$R_2 = R_O \,||\, R_L$$

$$= 594\ \Omega$$

From eq. (7.23) we have

$$A_{if} = \frac{I_0}{I_S} = -\frac{80 \times 10^{-3} \times .503 \times 10^3 \times 10 \times 10^3 \times .594 \times 10^3/.6 \times 10^3}{(.503 + .594 + 10) \times 10^3 + 80 \times 10^{-3} \times .503 \times .594 \times 10^6}$$

$$= -11.38.$$

From eq. (7.29)

$$A_{vf} = \frac{V_2}{V_S} = -\frac{80 \times 10^{-3} \times .503 \times .594 \times 10^6 \times 10 \times 10^3/.6 \times 10^3}{(0.503 + 10.594) \times 10^3 + 80 \times .503 \times .594 \times 10^3}$$

$$A_{vf} = -11.38.$$

The current and voltage gains are the same because $R_S = R_L$ and $R_1 \approx R_2$ in this problem. From eq. (7.25)

$$R_{inf} = \frac{.503 \times 10^3}{1 + \dfrac{80 \times 10^{-3} \times .503 \times .594 \times 10^6}{10.594 \times 10^3}}$$

$$= \frac{.503 \times 10^3}{1 + 2.256}$$

$$\text{or} \quad R_{inf} \approx 154\ \Omega$$

Similarly from eq. (7.28)

$$R_{out\,f} \approx \frac{.594}{1 + 2.265}$$

$$\approx 182\ \Omega$$

The current gain without feedback ($R_f = \infty$) is

$$\frac{I_0}{I_S} = -\frac{g_m R_1 R_0}{R_L + R_0}$$

$$= -\frac{80 \times 10^{-3} \times .503 \times 10^3 \times 60 \times 10^3}{0.6 \times 10^{+3} + 60 \times 10^{+3}}$$

$$\text{or} \quad \frac{I_0}{I_S} = -40.63$$

Making $R_f = \infty$ in A_{vf} we get the voltage gain without feedback as

$$A_v = -\frac{R_1}{R_S} \cdot g_m \cdot R_2$$

$$= -39.8$$

The input impedance without feedback is 503Ω and the output impedance without feedback is 594 Ω.

Instead of solving the feedback circuit problem using KCL directly we may identify the 'A' and the '*f*' networks seperately in the Figure of 7.6(d), as mentioned earlier. Ordinarily this is a difficult task but in some feedback circuits the identification may be done easily. In Fig. 7.6(d) the current I_f is caused by the output voltage V_2 of the feedback network. Taking into account the loading effect of R_f across the input and output terminals of the amplifier, the two networks A and f can be seperated as shown in Fig. 7.7. The values of A and f can now be calculated seperately as

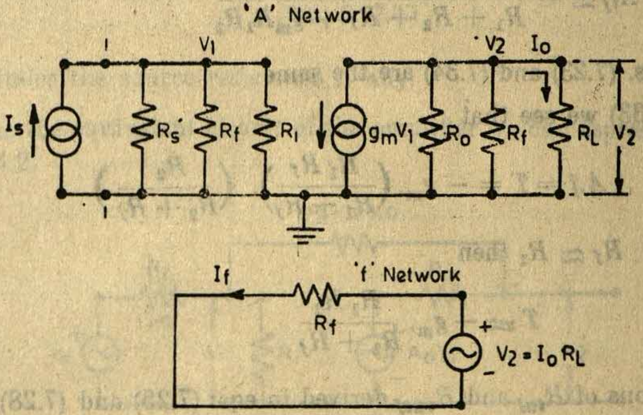


Fig. 7.7 Separation of 'A' and 'f' networks

$$A = \frac{I_o}{I_S} = -\frac{g_m}{R_L}\left(\frac{R_1 R_f}{R_1+R_f}\right)\left(\frac{R_2 R_f}{R_2+R_f}\right) \tag{7.31}$$

where $R_1 = R_S \,||\, R_i$

and $R_2 = R_O \,||\, R_L$ as before.

Now from Fig. 7.7 $I_f = V_2/R_f$ where $V_2 = I_o R_L$, hence

$$f = \frac{I_f}{I_o} = \frac{I_f}{V_2/R_L} = \frac{R_L}{R_f} \tag{7.32}$$

Since

$$A_{if} = \frac{A}{1 - A.f},$$

We can substitute the values of A and f from eq. (7.31) and (7.32) and obtain

$$A_{if} = \frac{-\dfrac{g_m}{R_L}\left(\dfrac{R_1 R_f}{R_1+R_f}\right)\left(\dfrac{R_2 R_f}{R_2+R_f}\right)}{1+\dfrac{g_m}{R_L}\cdot\left(\dfrac{R_1 R_f}{R_1+R_f}\right)\left(\dfrac{R_2 R_f}{R_2+R_f}\right)\cdot\dfrac{R_L}{R_f}} \qquad (7.33)$$

If we make the same assumptions as before, i.e. $R_f \gg R_1$. $R_f \gg R_2$ and $g_m \gg \dfrac{1}{R_f}$ we can simplify eq. (7.33) as

$$A_{if} = -\frac{g_m R_1 R_2 R_f/R_L}{R_1 + R_2 + R_f + R_1 R_2 (g_m + 1/R_f)}$$

or

$$A_{if} \approx -\frac{g_m R_1 R_2 R_f/R_L}{R_1 + R_2 + R_f + g_m R_1 R_2} \qquad (7.34)$$

Note that eqs. (7.23) and (7.34) are the same

From eq. (7.33) we see that

$$A.f = T = -g_m\cdot\left(\frac{R_1 R_f}{R_1 + R_f}\right)\cdot\left(\frac{R_2}{R_2 + R_f}\right)$$

Again if $R_1 \| R_f \approx R_1$ then

$$T \approx -g_m\cdot\frac{R_1 R_2}{R_2 + R_f} \qquad (7.35)$$

The expressions of R_{inf} and R_{outf} derived in eqs. (7.25) and (7.28) are seen to be

$$R_{inf} \approx \frac{R_1}{1-A.f} = \frac{R_1}{F} \qquad (7.36)$$

and

$$R_{outf} \approx \frac{R_2}{1-A.f} = \frac{R_2}{F} \qquad (7.37)$$

We have obtained, therefore, an expression between the input impedance with and without feedback in eq. (7.36). The input impedance of a shunt-shunt feedback amplifier is reduced approximately by a factor of $(1-Af) = F$. Similarly the output impedance also of a shunt-shunt feedback amplifier is reduced approximately by a factor of $(1-Af) = F$.

We have described a single stage amplifier and shown its terminal properties after an application of shunt-shunt feedback. The amplifier may, in general, be a multistage one but we can always represent it equivalently in terms of R_i, R_o and generator $g_m V_1$. If the A and f network are seperated then the feedback circuit can be analysed simply.

Example 7.4.2

The circuit in Fig. E 7.4.2 shows a very large gain amplifier with a shunt-shunt feedback. The input impedance R_i of the amplifier is 500 $k\,\Omega$ and $R_o = 75\,\Omega$, and the gain A_o without feedback is $-$ 10,000. Calculate the gain with feedback.

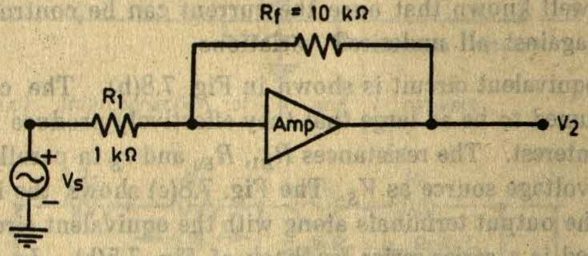


Fig. E. 7.4.1

Note R_1 includes the source resistance if any.

Drawing the equivalent circuit of the amplifier we can represent it as shown in Fig. E 7.4.2.

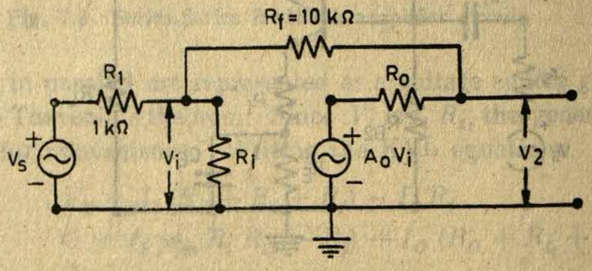


Fig. E. 7.4.2

Assuming $R_i >> R_1$ and solving we get

$$\frac{V_2}{V_S} = -\frac{R_f}{R_1} \cdot \left[\frac{A_O R_1}{\left(R_O + \frac{R_1 R_O}{R_f} + R_1 + R_f\right) + A_O R_1} \right]$$

Since A_O is very high, the above expression is approximated as

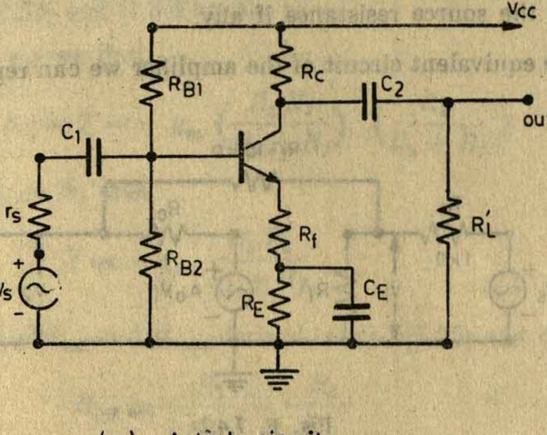
$$\frac{V_2}{V_S} \approx -\frac{R_f}{R_1}$$

Hence gain with feedback $\approx -$ 10

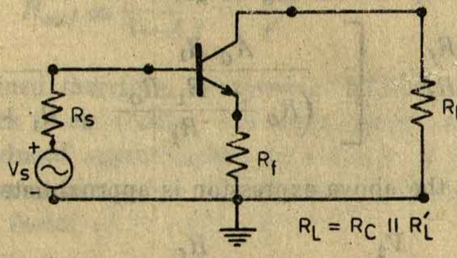
7.5 Series-Series Feedback

A single stage series-series feedback or a current-series feedback amplifier is shown in Fig. 7.8(a). The resistance R_f left unbypassed in the emitter lead of a common-emitter amplifier gives rise to negative feedback. For example any increase in the collector current results in an increase of emitter current and hence a rise in voltage across R_f. Since the emitter voltage rises, the base-emitter voltage difference reduces and consequently the collector current is reduced. Thus, we see that an opposing effect is immediately produced to any change in the collector current. It is well known that once the current can be controlled the amplifier will be stable against all undesired variations.

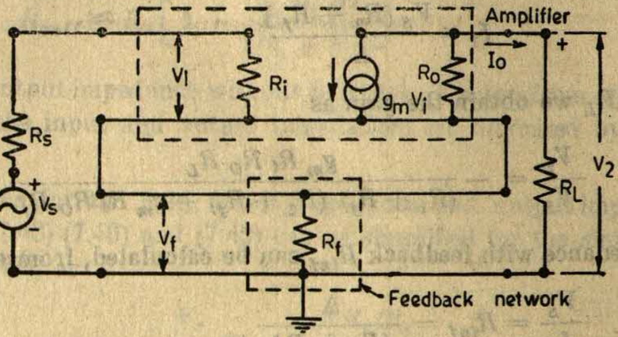
The a.c. equivalent circuit is shown in Fig. 7.8(b). The capacitances C_1, C_2 and C_E are assumed to be so large that they effectively produce a short circuit at frequencies of interest. The resistances R_{B1}, R_{B2} and r_S in parallel are represented by R_S and the voltage source as V_S. The Fig. 7.8(c) shows the interconnection at the input and the output terminals along with the equivalent circuit of the amplifier. This indeed is a series-series feedback of Fig. 7.5(b). In order to simplify the analysis the circuit is redrawn in Fig. 7.8(d). The current generator $g_m V_i$



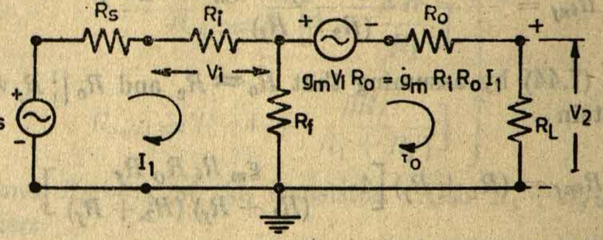
(a) Actual circuit



(b) Equivalent circuit



(c) Interconnection of A and f network



(d) Circuit redrawn

Fig. 7.8 Series-Series feedback amplifier circuit

and resistance R_o in parallel are represented as a voltage source $g_m V_i R_o$ with R_o in series using the Thevenin's theorem. Since V_i is $I_1 R_i$, the generator is written as $(g_m R_o R_i I_1)$ for convenience. Writing the KVL equations

$$V_S = I_1 (R_S + R_i + R_f) - I_o R_f \tag{7.38(a)}$$

$$O = I_1 (g_m R_i R_O - R_f) + I_O (R_O + R_L + R_f) \tag{7.38(b)}$$

Now $g_m R_i R_o \gg R_f$ in eq. 7.38(b) and can safely be neglected in comparison. The circuit determinant Δ can thus be written as

$$\Delta = (R_S + R_i + R_f)\ (R_O + R_L + R_f) + g_m R_i R_O R_f \tag{7.39}$$

Assuming that

$$R_S + R_i = R_1$$

$$R_O + R_L = R_2$$

eq. (7.39) is

$$\Delta = (R_1 + R_f)\ (R_2 + R_f) + g_m R_i R_O R_f \tag{7.40}$$

Solving for I_1 and I_o we get,

$$I_0 = -\frac{V_s \cdot g_m R_i R_o}{\Delta} \tag{7.41}$$

and
$$I_1 = \frac{V_S\,[R_2 + R_f]}{\Delta} \tag{7.42}$$

Since $V_2 = I_o R_L$ we obtain the gain as

$$\frac{V_2}{V_S} = -\frac{g_m R_t R_O R_L}{(R_1 + R_f)\,(R_2 + R_f) + g_m R_t R_O R_f} \tag{7.43}$$

The input impedance with feedback R_{inf} can be calculated, from eq. (7.42), as

$$\frac{V_S}{I_1} = R_{inf} = \frac{\Delta}{(R_2 + R_f)}$$

or,
$$R_{inf} = \frac{(R_1 + R_f)\,(R_2 + R_f) + g_m R_t R_O R_f}{(R_2 + R_f)} \tag{7.44}$$

Simplifying eq. (7.44) by assuming that $R_0 \approx R_2$ and $R_0 \,||\, R_f \approx R_f$ for the CE amplifier we obtain

$$R_{inf} = (R_1 + R_f)\left[1 + \frac{g_m R_t R_O R_f}{(R_1 + R_f)\,(R_2 + R_f)}\right]$$

or
$$R_{inf} \approx R_1 + (1 + g_m R_t)\, R_f \tag{7.45}$$

Now $g_m R_t$ the effective gain of the amplifier without feedback is far greater than one and hence eq. (7.45) is further simplified to

$$R_{inf} \approx R_1 + g_m R_t R_f \tag{7.46}$$

or
$$R_{inf} \approx R_1\left[1 + \frac{g_m R_t R_f}{R_1}\right]$$

Similarly the output impedance with feedback R_{outf} is given by finding I_o in equations 7.38(a) and (b) with a generator connected at the output terminals. Therefore

$$R_{outf} = \frac{\Delta}{R_1 + R_f} \tag{7.47}$$

$$= \frac{(R_1 + R_f)\,(R_2 + R_f) + g_m R_t R_O R_f}{R_1 + R_f}$$

Rewriting

$$R_{outf} = (R_2 + R_f)\left[1 + \frac{g_m R_t R_O R_f}{(R_1 + R_f)\,(R_2 + R_f)}\right] \tag{7.48}$$

Assuming that $R_2 + R_f \approx R_2$ and $R_o \approx R_2$

$$R_{outf} \approx R_2\left[1 + \frac{g_m R_t R_O R_f}{(R_1 + R_f)\,(R_2 + R_f)}\right] \tag{7.49) (a}$$

or
$$R_{outf} \approx R_2\left[1+\frac{g_m R_i R_f}{(R_1+R_f)}\right] \tag{7.49 (b)}$$

where R_2 is the output impedance without feedback. We see from eqs. (7.46) and (7.49) that both the input and output impedances are increased by series-series feedback.

The equations for the gain, input impedance and output impedance with feedback in eqs. (7.43) (7.46) and (7.49) can be simplified for the single stage CE amplifier of Fig. (7.8) as

$$\left.\begin{aligned} \frac{V_2}{V_S} &\approx -\frac{\beta R_L/R_1}{(1+\beta R_f/R_1)} \\ R_{inf} &\approx R_1\left[1+\frac{\beta R_f}{R_1}\right] \\ R_{outf} &\approx R\left[1+\frac{\beta R_f}{(R_1+R_f)}\right] \end{aligned}\right\} \tag{7.50}$$

since $g_m R_i = \beta$ and $R_O = r_0$ of the transistor. Also $R_1 + R_f \approx R_1$ in such single stage amplifiers.

Example 7.5.1

In a series-series feedback amplifier of Fig. 7.8(a) it is given that $R_L = R_C \parallel R_L' = 1\text{K}\,\Omega$, $R_f = 100\Omega$, $R_O = 80\text{K}\Omega$, $R_{B1} \parallel R_{B2} = 6\text{K}\Omega$, $r_s = 100\,\Omega$, $I_C = 1\text{ mA}$, $\beta = 200$, Calculate the gain with and without feedback, the feedback factor F, the input impedance and the output impedance.

Since $\quad I_C = 1\text{mA}$

$$g_m = \frac{1}{r_e} = 40 \times 10^{-3}\ \mho$$

$$R_i \approx \beta r_e = 5\,\text{K}\Omega$$

$$R_s = 100\ \Omega \parallel 6\text{ K} = 98\ \Omega$$

$$R_1 = 5.098\,\text{K}\Omega$$

$$R_2 = 80 + 1 = 81\ \text{K}\Omega$$

From eq. (7.43), the gain with feedback is

$$\frac{V_2}{V_S} = -\frac{40\times10^{-3}\times5\times10^{-3}\times80\times10^{-3}\times1\times10^{3}}{5.198\times10^{3}\times81.1\times10^{3}+40\times10^{-3}\times5\times10^{3}\times80\times10^{3}\times100}$$

$$\text{or}\quad \frac{V_2}{V_S} = -\ 7.92$$

Using eq. (7.50) the gain is

$$\frac{V_2}{V_S} \approxeq - \frac{200 \times \dfrac{1}{5.098}}{1 + \dfrac{200 \times 0.1}{5.098}}$$

$$= -7.96$$

We see that eq. (7.50) is a fairly good approximation of eq. (7.43).

From eq. (7.44)

$$R_{inf} = \frac{5.198 \times 10^3 \times 81.1 \times 10^3 + 40 \times 10^{-3} \times 5 \times 10^3 \times 80 \times 10^3 \times .1 \times 10^3}{81.1 \times 10^3}$$

or,

$$R_{inf} = 24.93\ \text{K}\Omega$$

From eq. (7.46)

$$R_{inf} \approxeq 5.098 \times 10^3 \left(1 + \frac{200 \times 0.1 \times 10^3}{5.098 \times 10^3}\right)$$

or $R_{inf} \approxeq 25.1\ \text{K}\Omega$

From eq. (7.49) (a) R_{outf} is

$$R_{outf} = 81 \times 10^3 \left[1 + \frac{200 \times 80 \times 10^3 \times .1 \times 10^3}{5.198 \times 10^3 \times 81.1 \times 10^3}\right]$$

or $R_{outf} = 388.4\ \text{K}\Omega$

From eq. (7.50), the approximate $R_{outf} = 392.66\ \text{K}\Omega$

The gain without feedback is

$$A_V = -\frac{\beta R_L}{R_1}$$

$$= -\frac{200 \times 1}{5.098}$$

or $A_V = -39.2$

$$R_{in} = R_1 = 5.098 \times 10^3\ \Omega$$

$$R_{out} = R_2 = 81 \times 10^3\ \Omega$$

$$F = \frac{A_V}{A_{Vf}} = 4.95$$

The network of Fig. 7.8(c) can be seperated into the 'A' and 'f' networks easily by identifying the circuits as shown in Fig. 7.9. The effect of R_f is taken into account by including it in the input and output mesh equations.

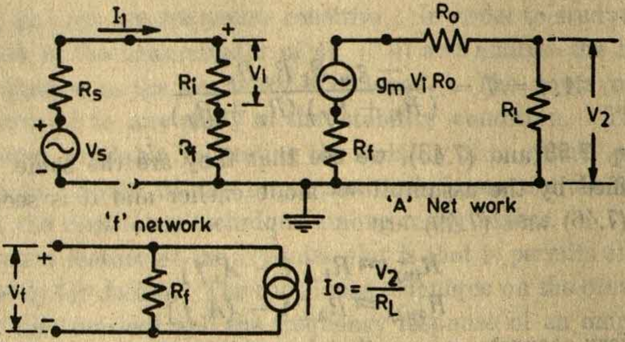


Fig. 7.9 Seperation of the 'A' and 'f' networks in the series-series feedback amplifier

$$V_2 = I_O \cdot R_L$$

or
$$V_2 = \frac{g_m V_i R_O R_L}{R_O + R_L + R_f}$$

Similarly
$$V_i = \frac{V_s \cdot R_i}{R_s + R_i + R_f}$$

Substituting for V_i in the above equation we get

$$A = \left.\frac{V_2}{V_S}\right|_{f=0} = -\frac{g_m R_i R_O R_L}{(R_i + R_f)(R_2 + R_f)} \tag{7.51}$$

Now $V_f = I_o R_f = V_2 \cdot \dfrac{R_f}{R_L}$

hence
$$f = \frac{V_f}{V_2} = \frac{R_f}{R_L} \tag{7.52}$$

Therefore

$$A_f = \frac{A}{1 - A \cdot f}$$

or
$$A_f = \frac{\dfrac{-g_m R_i R_o R_L}{(R_1 + R_f)(R_2 + R_f)}}{1 + \dfrac{g_m R_i R_o R_f}{(R_1 + R_f)(R_2 + R_f)}}$$

Simplifying, the gain is

$$A_f = -\frac{g_m R_i R_o R_L}{(R_1 + R_f)(R_2 + R_f) + g_m R_i R_o R_f} \tag{7.53}$$

and T is

$$A.f = T = \frac{-g_m R_i R_o R_f}{(R_1 + R_f)(R_2 + R_f)} \tag{7.54}$$

Comparing eq. 7.53 and (7.43), we see that they are the same. The eq. (7.54) can be simplified by the assumptions made earlier and it is seen that R_{inf} and R_{outf} of eq. (7.46) and (7.49) are

$$R_{inf} \cong R_1 1 [- A.f] \tag{7.55}$$

$$R_{outf} \cong R_2 [1 - (A.f] \tag{7.56}$$

Though not very accurate, we see that for series-series feedback the input and the output impedances are increased by the factor F approximately.

We have seen that both the input and output impedances decrease with shunt-shunt feedback and increase with series-series feedback. In case the amplifier has series-shunt feedback, the input impedance will increase but the output impedance will decrease. Similarly for the shunt-series feedback the input impedance will decrease and the output impedance will increase. Table I shows the terminal impedance of negative feedback amplifiers under different interconnections.

Table I Behaviour of terminal impedance with negative feedback

	Types of feedback			
Terminal Impedance	shunt-shunt	Shunt-series	Series-series	Series-shunt
Input impedance	decreases	decreases	increases	increases
Output impedance	decreases	increases	increases	decreases

7.6 Stability and other Considerations

We have seen that the application of negative feedback requires that the feedback signal is 180° out of phase with the input signal. In other words, any signal applied inside the feedback loop circulates around the loop and returns to the same point with its phase shifted by 180°. This is true and will hold for signals in the middle band of frequencies. As the signal frequency is increased, however, each transistor or active device stage will produce a phase lag which will increase with frequency. Now, if the forward amplifier is such that this extra phase lag becomes 180 or more at the high frequencies, the feedback voltage will become in-phase with the input voltage. This is clearly regenerative or positive feedback and the output of the amplifier will go on increasing with time. The amplifier is unstable if the loop gain exceeds unity when the total phase change around the loop is 0° or 360°.

Going back to eq. (7.4) we see that

$$A_f(s) = \frac{A(s)}{1 - A(s)\,f(s)} = \frac{A(s)}{F(s)} \tag{7.4}$$

and both $A(s)$ and $f(s)$ are frequency sensitive. In order to study the problems of stability we look at the denominator of eq. (7.4) and analyse the behaviour of the roots of this equation as the frequency is changed. The roots of this equation $F(s) = 0$ are central to any study of the stability condition. There are several methods, however, available for testing the stability of a system without actually finding the roots. Some of the important techniques are the Nyquist plot, the Bode plot and the root-locus technique among many others.

An attractive feature of the Nyquist plot is that it permits experimental data to be used directly for design. The root-locus technique on the other hand provides a control over the transient and the frequency response of an amplifier simultaneously and provides a wide view of the transfer function.

In some of the amplifiers we have discussed earlier in this chapter we have not examined the case whether the amplifiers remained stable after the feedback has been given. Particularly in the two stage amplifiers, if the feedback is increased, it is quite likely that the whole circuit will oscillate. Other than the problem of oscillation the feedback also controls the locations of the poles of the amplifier and thus it is possible to design circuits with maximally flat magnitude (MFM) response which may be optimum under many requirements.

Review Questions

7.1 Why should feedback be used if the gain of the amplifier is actually reduced ?

7.2 What is the sensitivity S_A of an amplifier ?

7.3 In a feedback amplifier does the noise introduced at the input get reduced ? Explain.

7.4 In a multistage feedback amplifier, is it correct to say that negative feedback is most effective where the distortion introduced is highest ? Explain.

7.5 By what factor does the upper 3 db frequency increase in a negative feedback amplifier ?

7.6 What are the disadvantages of negative feedback ?

7.7 Will a circuit with negative feedback always remain stable ?

7.8 What are the possible interconnections between an amplifier and its feedback network ?

7.9 In a shunt-shunt amplifier, what happens to the input impedance after the application of the feedback ?

7.10 Does the current gain of the shunt-shunt amplifier also reduce by the application of negative feedback ?

7.11 By what factor does the output impedance decrease in a shunt-shunt feedback amplifier in comparison to an amplifier without feedback ?

7.12 Does the input impedance increase in a series-shunt amplifier? By what factor ?

7.13 It is required to have a large input impedance. What type of input terminal connections should be used ?

7.14 Will the lower 3db cut-off frequency of an amplifier be affected by a series-series feedback circuit ?

7.15 What type of feedback has been used in an emitter follower circuit ?

7.16 Draw a circuit of a shunt-series feedback amplifier.

7.17 When will a negative feedback amplifier circuit be unstable ?

7.18 What is a Bode Plot ?

Problems

P 7.1 An amplifier has a gain of—200 an output of 5V peak and has a distortion of 20 percent. Due to parameter variations the gain is likely to change by 25 percent. It is essential that the distortion is less than or equal to two percent. What should be the feedback factor of the feedback amplifier ? Find the new gain and its sensitivity to parameter variations. What should be the new input ?

P 7.2 In a single stage shunt-shunt amplifier of Fig. 7.6 (a), it is given that $R_C || R'_L = 600\ \Omega$, $r_s || R_{B1} || R_{B2} = 100\ \Omega$, $I_C = 2\ \text{mA}$, $\beta = 150$. Find R_f if the voltage gain is -10. Assume $R_O \gg R_L$. What is the feedback factor F ?

P 7.3 If β changes by ± 50 percent in P 7.2 what would be the change in voltage gain ? Can this change be made ± 5 percent by a proper choice of R_f. Find the new value of R_f.

P 7.4 In P 7.2, the transistor's other parameters are given as $r_{bb'} = 50\ \Omega$, $C_{b'c} = 5$ pf, $\omega_T = 250$ Mrad/sec. Estimate the bandwidth (upper 3db frequency only) without and with feedback.

P 7.5 Calculate the input and the output impedances with and without feedback in P 7.2.

P 7.6 A single stage FET amplifier with a shunt-shunt feedback is shown in Fig. P 7.1. Find the value of R_f if a gain of -5 is desired. It is given

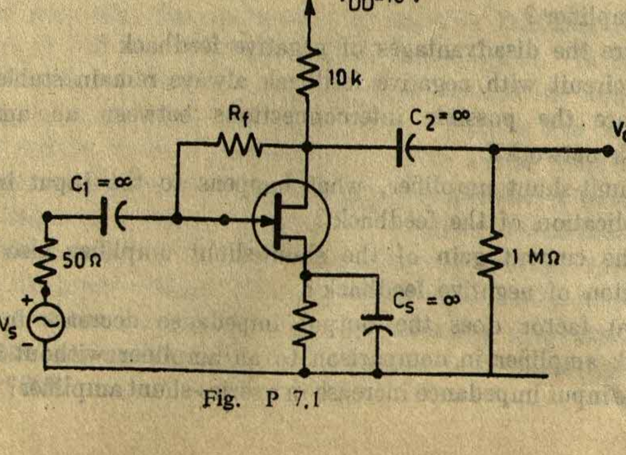


Fig. P 7.1

that $I_D = 1$ mA and $g_m = 2$ mA/volt. Neglect r_d. What are the input and the output impedances ?

P 7.7 An amplifier's gain is reduced using series-series feedback as shown in Fig. 7.8 (a). The parameters of the circuit and the transistor are $I_C = 5$ mA, $\beta = 200$, $R_S = 0.6$ K Ω, $R_L = 1$ K Ω, $R_0 = 80$ K Ω, what value of R_f should be used to get a voltage gain of -8 ? Find the input impedance with feedback. What is the loop transmission function ?

P 7.8 In P 7.7, if the transistor's high frequency parameters are given as $r_{bb'} = 60\ \Omega$, $C_{b'c} = 3\ pf$, $f_T = 200$ MHz, find the upper 3 db cut-off frequency with and without feedback.

P 7.9 A negative feedback amplifier is shown in Fig. P 7.2. What is the type of feedback ? Calculate the gain, input and output impedances of the circuit. It is given that $I_D = 1.5$ mA and $g_m = 1.5$ mA/volt.

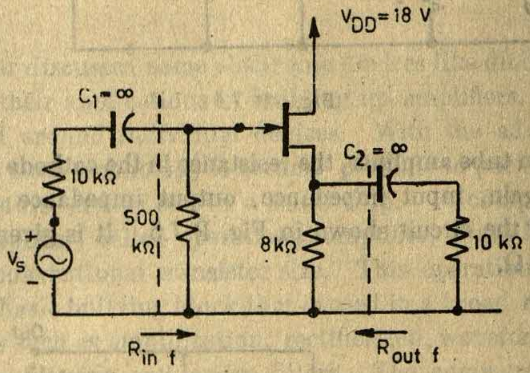


Fig. P 7.2

P 7.10 An a.c. equivalent of a shunt-series amplifier is shown in Fig. P 7.3. If it is given that $I_{C1} = 1$ mA, $I_{C_2} = 5$ mA, $R_L = 600\ \Omega$, $r_s = 600\ \Omega$, $R_C = 1$ K Ω, $R_E = 200\ \Omega$, $\beta_1 = \beta_2 = 100$. Find the voltage gain with feedback and the input impedance.

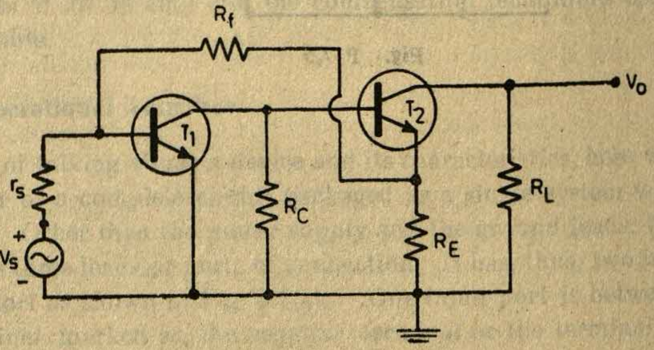


Fig. P 7.3

P 7.11 A series-shunt amplifier using FET is shown in Fig. P 7.4. If the transistors are identical with $I_{D1} = I_{D2} = 2\,\text{mA}$, $g_m = 1.5$ mA/volt and $r_d = 100\ \text{K}\ \Omega$, find the voltage gain, what are the advantages of this circuit ?

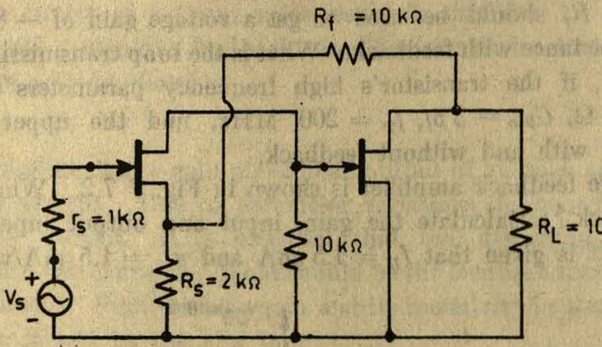


Fig. P 7.4

P 7.12 In a vacuum tube amplifier, the resistance in the cathode is left unbypassed. Find the gain, input impedance, output impedance and the feedback factor F of the circuit shown in Fig. P 7.5. It is given that $\mu = 20$ and $r_p = 10\ \text{k}\ \Omega$.

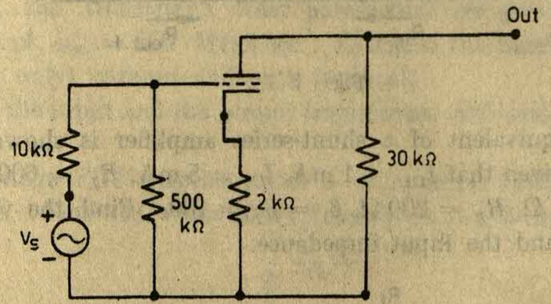


Fig. P 7,5

8

Operational Amplifiers And Their Applications

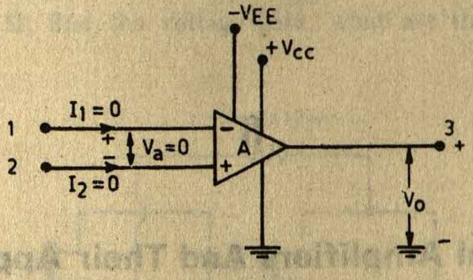
8.0 Introduction

We have so far discussed some electronic devices like diodes, transistors and vacuum tubes and their applications in building up amplifiers, rectifiers etc. The circuits were based around individual devices. With the advent of microminiaturization in solid state technology it became possible to package a large number of transistors, resistors, diodes etc. in a small chip. A complete very high gain direct—coupled amplifier, called operational amplifier, could be packaged into a size equal to one conventional transistor size. This operational amplifier or op-amp has become a basic building block that is used in a broad range of electronic circuit applications such as amplification, rectification, waveform generation, non-linear waveshaping, filtering and active filters. The commercially available op-amps are so well designed and trouble free that amplifiers and other circuits etc. built around single transistors are not used any more except in very special cases of very high frequency applications.

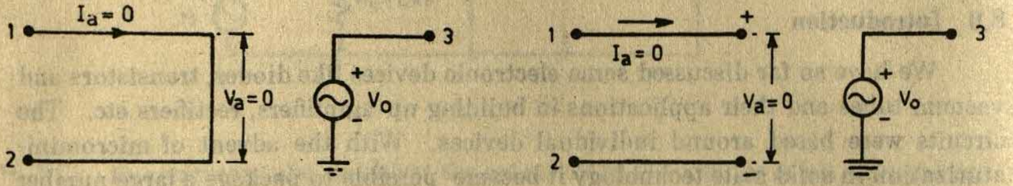
In this chapter we shall discuss the principles of op-amps, their performance limitations and some simple applications. We shall describe the input and the output circuits of an op-amp and the compensation techniques used for making the circuit stable.

8.1 Ideal operational Amplifier

Instead of talking about a device and its characteristics, here we shall discuss the behaviour of a complete circuit packaged as a single system with some leads brought out. Other than the power supply and the ground leads, the operational amplifier has three leads or ports of connection. It has, thus, two input ports and one output port as shown in Fig. 8.1(a). One input port is between the ground and the terminal marked as the negative terminal or the terminal 1. The other input port is between terminals marked as the positive terminals or the terminal 2 and the ground. The output port is between the terminal 3 and the ground and the output is designated as V_O. The polarity of the output is as assumed.



(a) Ideal op-amp



(b) Equivalent circuit

(c) Afernative equivalent circuit

Fig. 8.1 Op-amp

Let us assume that the operational amplifier is working in the linear region. Its ideal characteristics are

(i) its gain is infinite i.e., $A = \propto$

(ii) its input impedance at both the ports is infinite

(iii) its output impedance is zero

Let us examine the implications of the three properties given above. The infinite gain property will mean that for a finite V_O, the input voltage V_a between the positive and negative terminals is zero. Infinite input impedance will mean that none of the input terminals draw any current i.e. $I_1 = 0$ and $I_2 = 0$. Zero output impedance will mean that any current can be taken from the output without disturbing V_O.

An equivalent circuit of the op-amp can be modelled either as shown in Fig. 8.1(b) or as in (c). The equivalent circuit of Fig. 8.1(b) satisfies the condition that $V_a = 0$. The simultaneous requirement that the op-amp does not draw any current at any of its input ports is indicated by stipulating that $I_a = 0$. Thus, inspite of a short circuit at its input ports, the op-amp does not draw any current at the input. The alternative equivalent circuit of Fig. 8.1(c) satisfies the condition that

$I_a = 0$. The simultaneous requirement that $V_a = 0$ is indicated on the diagram. While analysing op-amp circuits we can use either of the equivalent circuits with equal ease.

Some additional assumptions about ideal op-amps are

(i) their bandwidth is infinite

(ii) they are perfectly balanced i.e. $V_O = 0$ if $V_1 = V_2$

(iii) their characteristics are stable against temperature variations.

We shall examine some of these properties later in detail.

8.2 Amplifiers using Op-Amps

Practical amplifiers are built using op-amps with negative feedback. The output terminal is connected through a resistive feedback to the negative terminal. The input may either be connected to the negative terminal or to the positive terminal. If the input is connected to the negative terminal we obtain what is called an inverting amplifier. Noninverting amplifier is obtained when the input is connected to the positive terminal. There is a third possibility when the two inputs are connected to the positive and the negative terminals and the difference of the two inputs is amplified. This is known as the difference amplifier. The amount of amplification is controlled by the feedback arrangement and can be set to any reasonable value including unity and less than unity.

8.2.1 NON-INVERTING AMPLIFIER

A non-inverting amplifier is shown in Fig. 8.2(a). The resistance R_2 is connected between the output terminal 3 and the negative input terminal 1. A resistance R_1 is connected to ground as shown. The input signal V_i is connected to the positive terminal 2. A load resistance R_L is also connected at the output. The equivalent circuit is shown in Fig. 8.2(b), where we have used the equivalent circuit of Fig. 8.1(c). The technique of solving for V_O will consist in obtaining and then equating V_a to zero. Thus, in Fig. 8.2(b), we have

$$V_a = \left(\frac{R_1}{R_2+R_1}\right)V_O - V_i \tag{8.1}$$

Setting $V_a = 0$, we get from eq. (8.1)

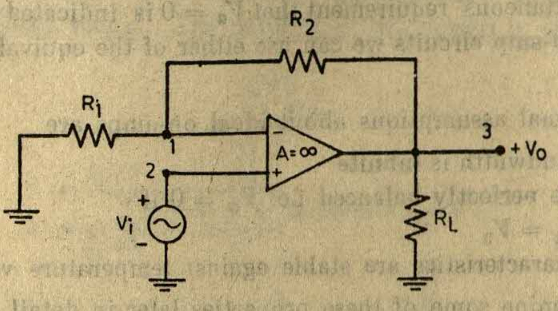
$$V_O \cdot \frac{R_1}{R_2+R_1} = V_i$$

or

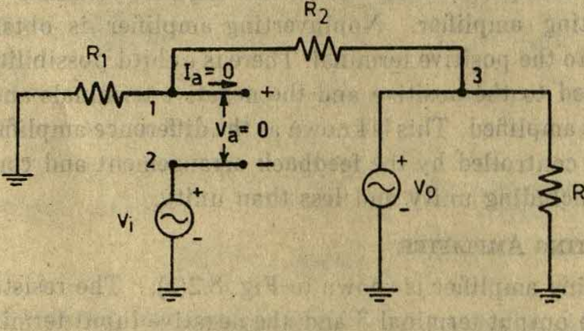
$$\frac{V_O}{V_i} = \frac{R_2+R_1}{R_1}$$

or

$$\frac{V_O}{V_i} = G_v = 1 + \frac{R_2}{R_1} \tag{8.2}$$



(a) Circuit connection



(b) Equivalent circuit

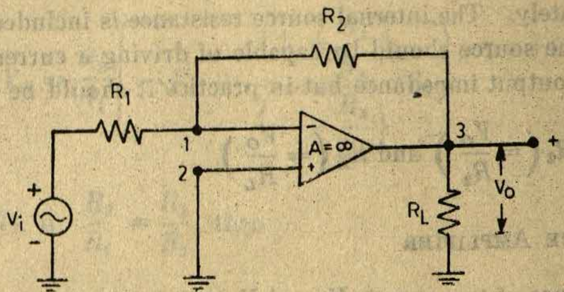
Fig. 8.2 Non-Inverting Amplifier

From eq. (8.2) as well as from Fig. 8.2 we observe that the gain is positive. This is the reason why it is called a non-inverting amplifier. The gain is equal to or greater than one. If $R_2 = 0$, then the gain is $+1$. Unity gain will also be obtained if $R_1 = \infty$.

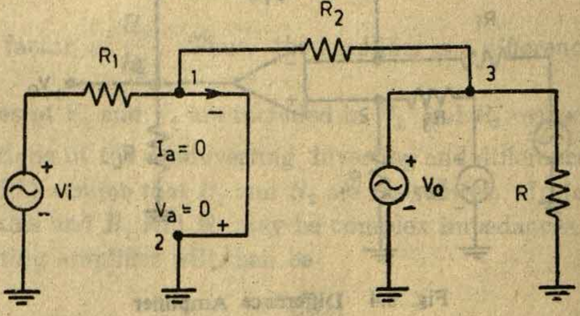
Another very interesting thing about this amplifier is that the gain G_v is only governed by two resistances R_1 and R_2 and is independent of (i) the source resistance (ii) the load resistance R_L and (iii) the parameters of the op-amp as long as the assumptions about it are valid. The output impedance is zero and hence the output can be loaded independently of the gain. In practice, however, the op-amp should be capable of supplying the output currents required by the feedback network and the load resistance R_L. The gain obtained is thus very stable and trouble free.

8.2.2 INVERTING AMPLIFIER

The circuit diagram of an inverting amplifier is shown in Fig. 8.3(a). The source V_i is connected in series with R_1 and R_2 is connected across the output and the negative input terminals as before. The positive terminal is connected to ground. The equivalent circuit is shown in Fig. 8.3(b). Here we have drawn the other equivalent circuit of Fig. 8.1(b) for illustration.



(a) Circuit diagram



(b) Equivalent circuit

Fig. 8.3 Inverting Amplifier

Now, writing down an equation for I_a we have

$$I_a = \frac{V_i}{R_1} + \frac{V_O}{R_2} \tag{8.3}$$

Since $I_a = 0$, we obtain from eq. (8.3)

$$\frac{V_O}{R_2} = -\frac{V_i}{R_1}$$

$$\frac{V_O}{V_i} = G_v = -\frac{R_2}{R_1} \tag{8.4}$$

From eq. (8.4) as well as from Fig. 8.3 we observe that the gain is negative. This is the reason why this circuit is called an inverting amplifier. The gain is obtained as a ratio of two resistors and hence is independent of the load resistance R_L and other parameters of the op-amp. The gain can be set to any value and maintained accurately. The internal source resistance is included as a part of the resistance R_1. The source should be capable of driving a current of V_i/R_1. The op-amp has zero output impedance but in practice it should be able to drive the current through $R_2\left(=\frac{V_O}{R_2}\right)$ and $R_L\left(=\frac{V_O}{R_L}\right)$.

8.2.3 DIFFERENCE AMPLIFIER

If the difference of two signals V_1 and V_2 is to be amplified, then the op-amp is connected as shown in Fig. 8.4. Taken individually, the inverting gain $\left(\frac{R_2}{R_1}\right)$ is less than the non-inverting gain $\left(1+\frac{R_2}{R_1}\right)$. For subtracting V_1 and V_2 it is essential, therefore, to make the gains of the two input ports equal. The non-inverting input is thus reduced in amplitide by the R_3, R_4 network shown. In order to calculate V_O we can use the idea of the linear superposition theorem, that is, we consider first that V_1 alone is present and find V_O. Next, we take V_2 alone as present and calculate V_O. We then add the two together to obtain the overall output. Thus, considering V_1 alone as present we obtain V_O as

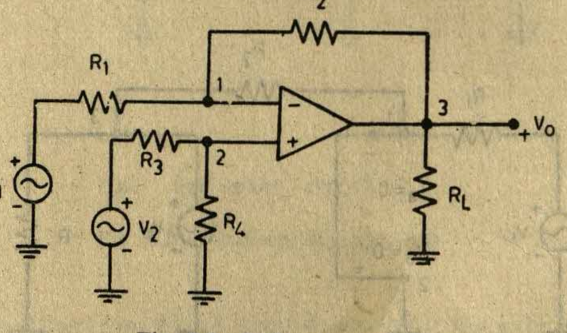


Fig. 8.4 Difference Amplifier

$$V_{O1} = V_1 \left(-\frac{R_2}{R_1} \right) \tag{8.5}$$

Next, considering V_2 alone as present

$$V_{O2} = V_2 \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \tag{8.6}$$

Combining eq. (8.5) and (8.6), we obtain

$$V_O = V_{O1} + V_{O2} = -V_1 \left(\frac{R_2}{R_1} \right) + V_2 \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right)$$

$$\text{or} \quad V_O = \frac{R_2}{R_1} \left[-V_1 + \frac{\left(1 + \frac{R_1}{R_2} \right)}{\left(1 + \frac{R_3}{R_4} \right)} V_2 \right] \tag{8.7}$$

In eq. (8.7), if $\frac{R_3}{R_4} = \frac{R_1}{R_2}$, then

$$V_O = \frac{R_2}{R_1} \left(V_2 - V_1 \right) \tag{8.8}$$

The eq. (8.8) shows that we obtain the difference of $(V_2 - V_1)$ at the output though multiplied by a factor of $\frac{R_2}{R_1}$. Thus, the amplifier is a difference amplifier. The source impedances of V_1 and V_2 are included in R_1 and R_3 respectively.

The derivations of the noninverting, inverting and difference amplifiers in eq. (8.2), (8.4) and (8.8) assume that R_1 and R_2 are resistances. In fact, it is not necessary to assume this and R_1 and R_2 may be complex impedances. The gain equation for an inverting amplifier will then be

$$G_v(s) = -\frac{Z_2(s)}{Z_1(s)}$$

and $G_v(s) = 1 + \frac{Z_2(s)}{Z_1(s)}$ for a non-inverting amplifier.

Example 8.2.1

A difference amplifier having a voltage gain of 50 is required. Calculate the values of the different resistances. How much is the non-inverting gain of this amplifier ? If the input signals V_1 and V_2 are equal, what is the output ?

The differential gain is given by eq. (8.8) as

$$G_{vd} = \frac{R_2}{R_1} = 50 \text{ as required,}$$

$$\text{Assuming } R_2 = 47 \text{ K}\Omega$$

$$R_1 = 940\,\Omega$$

$$\text{From eq (8.7), } \frac{R_3}{R_4} = \frac{R_1}{R_2}$$

$$\text{or } \frac{R_2}{R_1} = \frac{R_4}{R_3} = 50$$

Therefore, $R_4 = 47\text{ K}\Omega$ and $R_3 = 940\,\Omega$

$$\text{Now non-inverting gain} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)$$

$$= \left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{R_3}{R_4}}\right) = 51 \times \frac{50}{51} = 50$$

The output $V_O = 0$ when $V_1 = V_2$.

8.2.4 THE SUMMING AMPLIFIER

Op-amp can be used to add two or more signals as shown in Fig. 8.5. We can calculate the output by finding I_a and then equating it to zero. Thus

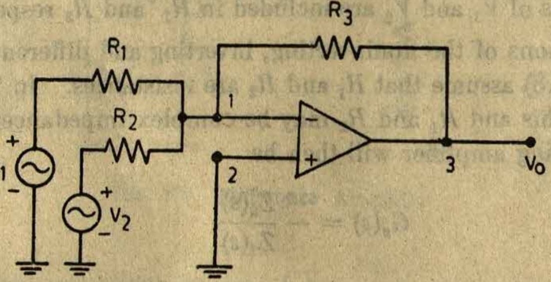


Fig. 8.5 Summing Amplifier

$$I_a = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_O}{R_3} = 0$$

Hence

$$V_O = -\left(\frac{R_3}{R_1}\right)V_1 + \left(-\frac{R_3}{R_2}\right)V_2$$

$$\text{or} \quad V_O = \left[\frac{R_3}{R_1} \cdot V_1 + \frac{R_3}{R_2} V_2 \right] \tag{8.9)(a}$$

If $R_1 = R_2 = R$ then

$$V_o = -\frac{R_3}{R_2}\left[V_1 + V_2 \right] \tag{8.9(b)}$$

We should remember that R_1 and R_2 include the source resistances of V_1 and V_2 respectively. Since there is a virtual short circuit at the input, the sources V_1 and V_2 do not interact with each other. In other words R_2 has no effect on source V_1 and hence the gain associated with R_3 and R_1. Similarly R_1 has no effect on the gain produced due to the source V_2. The output is proportional to the sum of the two signals.

Example 8.2.2

Calculate the output of a summing amplifier where $R_1 = 10\ \text{K}\Omega$, $R_2 = 5\text{k}\Omega$, and $R_3 = 20\ \text{K}\Omega$. The input signals are $V_1 = 0.3 \cos \omega t$ and $V_2 = 0.2 \cos \omega t$.

$$\begin{aligned} \text{The output } V_O &= -\frac{R_3}{R_1} V_1 - \frac{R_3}{R_2} V_2 \\ &= -[2 \times 0.3 \cos \omega t + 4 \times 0.2 \cos \omega t] \\ &= -[0.6 \cos \omega t + 0.8 \cos \omega t] \\ &= -1.4 \cos \omega t. \end{aligned}$$

The op-amp characteristics that we have assumed have been ideal. The actual circuit will have imperfections and the performance will only approach the ideal in a sense. Thus, the actual IC op-amps have a gain between 10^6 to 10^8 instead of infinity. The input—impedance ranges from a few hundred kilo ohms to a few hundred mega-ohms and so on. Before going into these actual characteristics let us first see how these op-amps are assembled or built. The IC op-amps available in the market differ considerably in the type of circuits, transistors and number of stages used. In its most general form the op-amp consists of two stages of differential amplifiers followed by a driver and an output circuit. The input in special cases may use a circuit known as a Darlington pair or an FET in differential amplifier connection, though in ordinary op-amps simple differential amplifiers using BJT are employed. We shall first describe a differential amplifier in the next section.

8.3 Input circuit-differential amplifier

Normally the op-amps are designed to have a differential input because it offers certain advantages of balance and rejection of stray pickup signals etc. The differential amplifier is the first stage of such op-amps. Conceptually the block diagram of the differential amplifier is as shown in Fig. 8.6. It has two input terminals 1 and 2 where signals V_1 and V_2 are connected. There are two output terminals 3 and 4. The output at 3 is V_{01} and the output at 4 is V_{02} both with respect to ground. The differential output also can be taken between 3 and 4 and is designated as V_O.

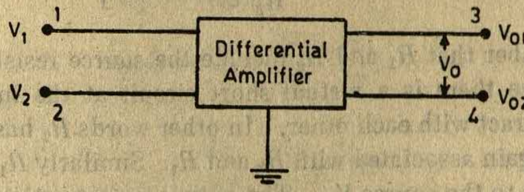


Fig. 8.6 Differental amplifier

In a differential amplifier various connections are possible. We can connect a balanced or double ended signal to the inputs 1 and 2 and take a double ended or balanced output between 3 and 4. On the other hand, we could take a single ended or unbalanced output only say $V_{02} = V_O$—for the same balanced input. Both connections are extensively used. The third possibility is that we use a single ended input—either at 1 or 2—and a single ended output. This configuration also is quite popular. Let us assume that we are interested in a differential amplifier with a balanced input and a single ended output V_G (at V_{02}). In an ideal situation we expect that

$$V_O = A_d (V_1 - V_2) \tag{8.10}$$

where A_d is the differential gain of the amplifier and V_1, V_2 are the input signals. Evidently from eq. (8.10) if we have $V_1 = V_2$, then $V_O = 0$. In other words it means that any signal which is common to both V_1 and V_2 will cancel at the output.

There is a note of caution in using eq. (8.10). The output of the amplifier does not depend only on the difference of V_1 and V_2 but also on their average level. Thus, for instance, the gain of the amplifier will be different in two cases where (i) $V_1 = +25$ mV, $V_2 = -25$ mV and (ii) $V_1 = 625$ mV, $V_2 = 575$ mV. The difference signal in both cases is 50 mV but in the second case the average signal is 600 mV whereas it is zero in the first case. We shall therefore define two signals, one as the difference—mode and the other as the common-mode as

Difference mode signal $= V_d = (V_1 - V_2)$

and Common mode signal $= V_C = \frac{1}{2}(V_1 + V_2)$ (8.11)

We shall write the output V_o of the amplifier in terms of V_d and V_c.

Applying the principle of linear superposition to the circuit of Fig. 8.6, let us assume that V_2 is not there and the terminal 2 is grounded. The output at terminal 4 with respect the ground is say A_1V_1. Similarly, if we assume that V_1

is not there and the terminal 1 is grounded, then the output at terminal 4 is $A_2 V_2$. By the superposition principle we can state that when both V_1 and V_2 are present then

$$V_0 = A_1 V_1 + A_2 V_2 \tag{8.12}$$

Writing V_1 and V_2 in terms of V_d and V_c we obtain, from eq. (8.11),

$$V_1 = V_C + \frac{1}{2} V_d \tag{8.13}$$

and $$V_2 = V_C - \frac{1}{2} V_d$$

Substituting these values in eq. (8.12)

$$V_0 = A_1 \left(V_c + \frac{1}{2} V_d\right) + A_2 \left(V_c - \frac{1}{2} V_d\right)$$

$$= (A_1 + A_2) V_c + \frac{1}{2} (A_1 - A_2) V_d$$

or $$V_0 = A_c V_c + A_d V_d \tag{8.14}$$

where $$A_c = A_1 + A_2$$

and $$A_d = \frac{1}{2} (A_1 - A_2)$$

We can use eq. (8.12) and (8.13) for finding the differential gain A_d and the common-mode gain A_c of any differential amplifier. The output in any differential amplifier will then be given by eq. (8.14). The eq. (8.14) describes a situation when there is a balanced input and an unbalanced output. If a balanced output is taken, then we take the differential output between the terminals 3 and 4.

A common-emitter differential amplifier is shown in Fig. 8.7. The two transistors are assumed to be identical in their characteristics, and the collector resistances are equal to R_C. The d.c.bias is so adjusted that the emitters are at about -0.65 V, the cut-in voltage of the transistor so that the bases can be grounded physically if required and the transistors will be conducting properly even then. We can calculate A_1 and A_2 seperately as has been suggested above. Assuming terminal 2 to be grounded and taking the output at 4, we can draw the equivalent circuit as shown in Fig. 8.8 R_i is the input resistance of the transistor and is approximately equal to βr_e and $g_m \approx \frac{1}{r_e}$. Solving for the circuit in Fig. 8.8

$$V_0 = A_1 V_1$$

Now $$V_0 = g_m V_E R_C = \frac{R_C}{r_e} \cdot V_E \tag{8.15}$$

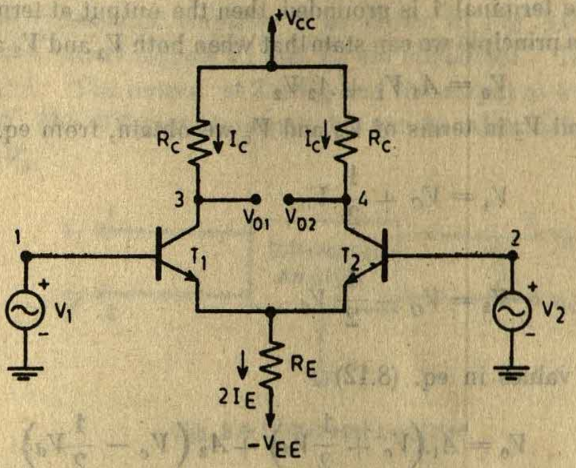


Fig. 8.7 Differential amplifier

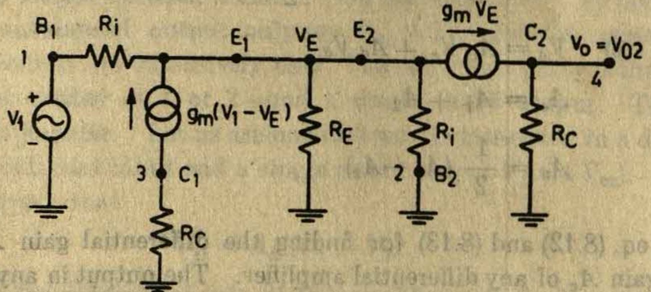


Fig. 8.8 Equivalent circuit of a differential amplifier with V_1 connected

Writing KCL at node V_E we have

$$\frac{V_1}{R_i} + \frac{V_1}{r_e} = V_E\left[\frac{2}{R_i} + \frac{2}{r_e} + \frac{1}{R_E}\right]$$

$$\text{or}\quad V_E = \frac{V_1\left[\dfrac{R_i + r_e}{R_i\, r_e}\right]}{2.\dfrac{R_i + r_e}{R_i\, r_e} + \dfrac{1}{R_E}}.$$

$$\text{or}\quad V_E = \frac{V_1}{2 + \dfrac{R_i\, r_e}{R_E(R_i + r_e)}} \tag{8.16}$$

Substituting the value of V_E from eq. (8.16) into eq. (8.15) we obtain

$$A_1 = \frac{V_0}{V_1} = \frac{R_C / r_e}{2 + \frac{R_i r_e}{R_E(R_i + r_e)}} \tag{8.17}$$

We notice that this is the non-inverting input terminal and gain is $+A_1$. Similarly, if the input is connected at terminal 2 and the terminal 1 is grounded, the output V_0 at terminal 4 can be calculated from the equivalent circuit of Fig. 8.9. Now at the terminal 4, the output V_0 is

$$V_0 = -\frac{V_2 - V_E}{r_e} R_C \tag{8.18}$$

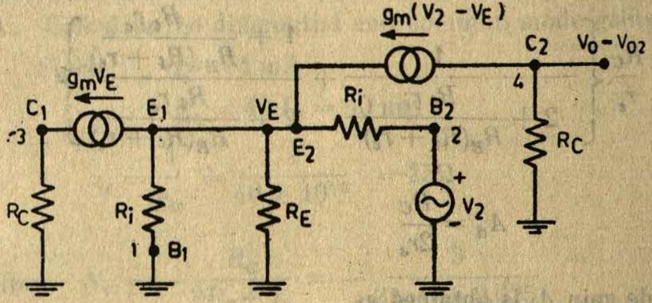


Fig. 8.9 Equivalent circuit of the differential amplifier with V_2 connected

Solving for V_E from Fig. 8.9 by writing the KCL we obtain, as in eq. (8.16),

$$V_2\left(\frac{1}{R_i} + \frac{1}{r_e}\right) = V_E\left(\frac{1}{R_E} + \frac{2}{R_i} + \frac{2}{r_e}\right)$$

$$\text{Hence } V_E = \frac{V_2}{2 + \frac{R_i r_e}{R_E(R_i + r_e)}} \tag{8.19}$$

Substituting the value of V_E from eq. (8.19) in eq. (8.18)

$$V_0 = -\frac{R_c}{r_e}\left[V_2 - \frac{V_2}{2 + \frac{R_i r_e}{R_E(R_i + r_e)}}\right] \tag{8.20}$$

Hence A_2 is obtained from eq. (8.20) as

$$A_2 = \frac{V_o}{V_2} = -\frac{R_C}{r_e}\left[1 - \frac{1}{2 + \frac{R_i r_e}{R_E(R_i + r_e)}}\right]$$

$$\text{or} \quad A_2 = -\frac{R_C}{r_e}\left[\frac{1+\dfrac{R_i r_e}{R_E(R_i+r_e)}}{2+\dfrac{R_i r_e}{R_E(R_i+r_e)}}\right] \tag{8.21}$$

Notice the negative sign in eq. (8.21)

Having calculated A_1 and A_2 in eqs. (8.17) and (8.21) we now can obtain A_d and A_c. Thus

$$A_d = \frac{1}{2}(A_1 - A_2)$$

$$= \frac{1}{2}\left[\frac{R_C}{r_e}\left\{\frac{1}{2+\dfrac{R_i r_e}{R_E(R_i+r_e)}} + \frac{1+\dfrac{R_i r_e}{R_E(R_i+r_e)}}{2+\dfrac{R_i r_e}{R_E(R_i+r_e)}}\right\}\right]$$

$$\text{or} \qquad A_d = \frac{R_C}{2r_e} \tag{8.22}$$

The common mode gain A_c is obtained as

$$A_c = A_1 + A_2$$

$$= \frac{R_c}{r_e}\left[\frac{1}{2+\dfrac{R_i r_e}{R_E(R_i+r_e)}} - \frac{1+\dfrac{R_i r_e}{R_E(R_i+r_e)}}{2+\dfrac{R_i r_e}{R_E(R_i+r_e)}}\right]$$

Simplifying

$$A_c = -\left[\frac{1}{2\,\dfrac{R_E(R_i+r_e)}{R_i r_e}+1}\right]\frac{R_C}{r_e} \tag{8.23}$$

Eq. (8.23) can be simplified further by assuming that R_i $(=\beta r_e) \gg r_e$ and hence $R_i + r_e \approx R_i$. We obtain from eq. (8.23)

$$A_c = -\frac{R_C}{2R_E + r_e}$$

$$\text{or} \qquad A_c \approx -\frac{R_C}{2R_E} \tag{8.24}$$

If the sources have an internal source resistance of R_S then the eq (8.22) and (8.24) will modify to

$$A_d = \frac{1}{2} \cdot \frac{R_C}{r_e + \dfrac{R_S}{\beta}} \tag{8.25}$$

and

$$A_c = -\frac{R_c}{2\,R_E + r_e + \dfrac{R_s}{\beta}} \tag{8.26}$$

Example 8.3.1.

A differential amplifier as shown in Fig. 8.7 has $R_C = 5K\Omega$, $R_E = 6K\Omega$ and $I_C = 1$ mA. Calculate the differential and common mode gains A_d and A_c.

Since $\quad I_C = 1$ mA

$$g_m = 40\,I_C = 40\ \text{m}\mho$$

$$r_e = \frac{1}{g_m} = \frac{1}{40 \times 10^{-3}} = 25\Omega$$

Therefore, $\quad A_c = -\dfrac{R_C}{2R_E + r_e} = -\dfrac{5}{2 \times 6 + 0.025}$

$$= -\frac{5}{12} = -0.417$$

and $\quad A_d = \dfrac{1}{2}\,\dfrac{R_C}{r_e} = \dfrac{1}{2} \times \dfrac{5000}{25} = 100$

In the case where a differential output is taken $(V_{01} - V_{02})$ can be shown to be twice the value of the gain calculated in eq. (8.22.) That is

$$A_d \Big|_{\substack{\text{differential} \\ \text{output}}} = \frac{R_C}{r_e} \tag{8.27}$$

Similarly, if a single ended input, say V_1 is given and a single ended output is taken, then from eq. (8.17)

$$A_1 = \frac{V_0}{V_1} \simeq \frac{R_C}{r_e} \cdot \frac{1}{2 + \dfrac{r_e}{R_E}}$$

Now $r_e \leqslant R_E$ and therefore

$$A_1 \simeq \frac{1}{2}\,\frac{R_C}{r_e} \tag{8.28}$$

8.3.1 Common Mode Rejection Ratio

In a differential amplifier the interest is to amplify the differential signal $V_1 - V_2$ and the output should not be proportional to the level of the signals. In other words, the common mode gain should ideally be zero. If the same signal with the same polarity ($V_1 = V_2$) is applied to both the inputs then A_C should be zero. From eq. (8.24) we see that $A_C = -R_C/2R_E$ and will depend upon the value of R_E. It has to be remembered that in eq. (8.24) we have already assumed that the devices are identical and draw identical currents and that the resistances are equal. This may not be possible in practice. Similarly R_E cannot be made ideally infinite to obtain $A_C = 0$ even if the other conditions are met. All attempts are however made to have an amplifier with a minimum A_C, A figure of merit of the performance of a differential amplifier is defined as the common mode rejection ratio (CMRR) to be

$$\text{CMRR} = \left| \frac{A_d}{A_c} \right| \tag{8.29}$$

Evidently the CMRR should be as high as possible. From eq. (8.22) and (8.24)

$$CMRR = \frac{R_E}{r_e} = g_m R_E \tag{8.30}$$

Example 8.3.2

Calculate the value of CMRR for the differential Amplifier of example 8.3.1.

$$\text{The common mode gain } A_c = -0.417$$

$$\text{The differential gain } A_d = 100$$

$$\text{Therefore, CMRR} = \left| \frac{A_d}{A_c} \right| = \frac{100}{0.417} = 240$$

Alternatively, CMRR $= g_m R_E$

$$= 40 \times 10^{-3} \times 6 \times 10^3 = 240 = 47.6\,dB$$

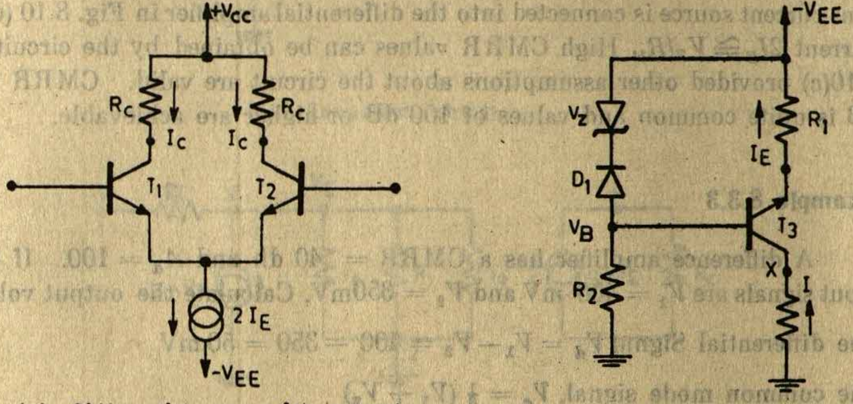
The output V_0 can be written in terms of the differential gain A_d and the CMRR as

$$V_o = A_d V_d + A_c V_c$$

$$V_0 = A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d} \right] \tag{8.31}$$

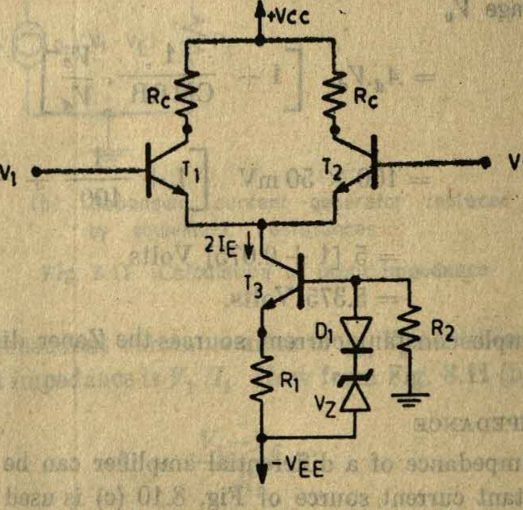
From eq. (8.31) it is seen that, if $V_o = A_d V_d$ is the desired output of the amplifier, then CMRR should ideally be infinite, or as large as possible. To obtain a large value of CMRR we must have R_E very large in eq. (8.30). It is not possible to connect physically a very large resistance in the emitter of Fig. 8.7 for a given V_{EE} and I_C.

An effect of large resistance can be produced electrically by connecting a constant current source at the emitter. We know that a constant current source has a very high internal impedance. This constant current source draws the current of $2I_E$ or $(I_{E1}+I_{E2})$ and is connected as shown in Fig. 8.10(a). A constant current source is shown in Fig. 8.10(b). Disregarding the diode D_1 for a moment, the



(a) Differential amp with current source

(b) Constant current source



(c) Actual circuit of the amplifier

Fig. 8.10 Differential amplifier circuit.

Zener diode and R_2 combination will give a fixed voltage V_B at the base and hence $(V_B\text{-}V_{BE})$ at the emitter of the transistor. The current I_E will, therefore, be fixed for a given R_1 since the voltage across it is fixed. Now the current I will be constant because I_E is constant. The diode D_1 is connected in order to compensate for the temperature variations of the base-emitter diode of the transistor T_3. When T_3 is a silicon transistor then the diode D_1 also is a silicon diode.

The point X in Fig. 8.10(b) can assume any voltage depending upon the value of R as long as the transistor does not get saturated. The main point to note is that the current I through R will remain reasonably constant. The effective output impedance of this circuit at the point X, therefore, is very high. The constant current source is connected into the differential amplifier in Fig. 8.10 (c). The current $2I_E \cong V_Z/R_1$. High CMRR values can be obtained by the circuit of Fig. 8.10(c) provided other assumptions about the circuit are valid. CMRR of 60-80 dB is quite common and values of 100 dB or higher are achievable.

Example 8.3.3

A difference amplifier has a CMRR = 40 db and $A_d = 100$. If the two input signals are $V_1 = 400$ mV and $V_2 = 350$mV, Calculate the output voltage V_0.

The differential Signal $V_d = V_1 - V_2 = 400 - 350 = 50$ mV

The common mode signal, $V_c = \frac{1}{2}(V_1 + V_2)$

$$= \tfrac{1}{2}(400 + 350) = 375 \text{ mV}$$

The output voltage V_0

$$= A_d . V_d \left[1 + \frac{1}{\text{CMRR}} \cdot \frac{V_c}{V_d}\right]$$

$$= 100 \times 50 \text{ mV} \left[1 + \frac{1}{100} + \frac{375}{50}\right]$$

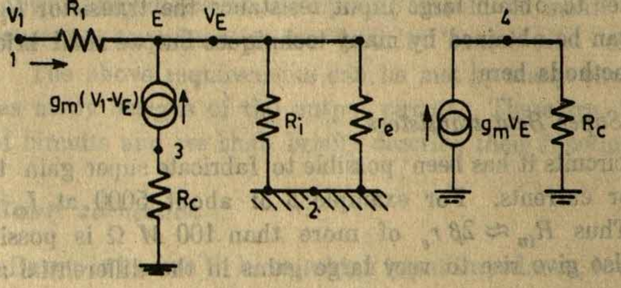
$$= 5\ [1 + 0.075] \text{ Volts}$$

$$= 5.375 \text{ Volts.}$$

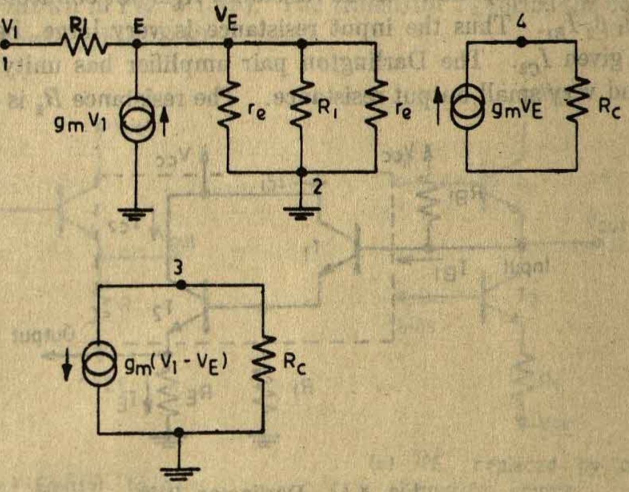
Sometimes in simple constant current sources the Zener diode is replaced by a resistance.

8.3.2 INPUT IMPEDANCE

The input impedance of a differential amplifier can be calculated from Fig. 8.8. If the constant current source of Fig. 8.10 (c) is used then the emitters are floating and the input impedance can be obtained from Fig. 8.11 simply. The circuit in Fig. 8.11 (a) can be simplified to the one shown in (b). The current coming in at node E is $g_m (V_1 - V_E)$ and going out at node 3 is $g_m (V_1 - V_E)$. Hence the nodes have been seperated though the currents are the same. Similarly the node 4 and E have also been seperated. The current $g_m V_E$ going out from the node E will be the same if instead a resistance r_e is connected to ground from the node E.



(a) Equivalent circuit



(b) Dependent current generator replaced by equivalent resistances.

Fig. 8.11 Calculation of input impedance

Therefore, the two dependent current sources of $g_m V_E$ have been replaced by r_e at the nodes. The input impedance is V_1/I_1. Now from Fig. 8.11 (b), the current I_1 is

$$I_1 = \frac{V_1 - V_E}{R_i} \tag{8.32}$$

where $$V_E \simeq g_m V_1 \cdot \frac{r_e}{2} = \frac{V_1}{2}$$

hence $$\frac{V_1}{I_1} = R_{in} \approx 2 R_i \tag{8.33}$$

In order to obtain large input resistance the transistor R_i has to be large. A large R_i can be obtained by many techniques but we shall briefly describe three important methods here

(*i*) *Use of Super Beta transistors*

In IC circuits it has been possible to fabricate super gain transistors at very low collector currents. For example β of about 5000 at I_C of 1 μA has been obtained. Thus $R_{in} \approx 2\beta r_e$ of more than 100 $M\ \Omega$ is possible. Super gain transistors also give rise to very large gains in the differential amplifiers.

(*ii*) *Use of Darlington Pair amplifier*

A CC-CC pair amplifier is shown in Fig. 8.12. This pair is also known as Darlington (pair) amplifier. If the resistance R_1 is not connected then $I_{C2} \simeq \beta I_{C1}$ and $I_{C2} = \beta_1 \beta_2 I_{B1}$. Thus the input resistance is very large because I_{B1} is very small for a given I_{C2}. The Darlington pair amplifier has unity gain, large input resistance and very small output resistance. The resistance R_1 is connected to leak off some of the excessive I_{E1} from the transistor T_2 Darlington pairs are used in place of the transistors T_1 and T_2 in Fig. 8.7.

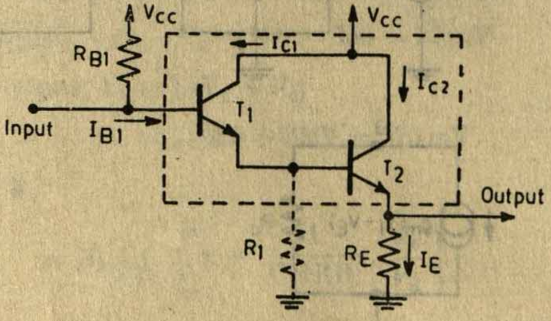


Fig. 8.12 Darlington Pair

(*iii*) *Use of* FET/MOSFET

The differential amplifier may use-FET as the active device and obtain large input impedance.

Normally the differential amplifier forms the input of the op-amp. The two inputs (1) and (2) of Fig. 8.7, therefore are the inverting and non-inverting leads of the op-amp. Input (1) is the non-inverting lead—eq. (8.17), and the input (2) is the inverting lead—eq.(8.21) of the amplifier.

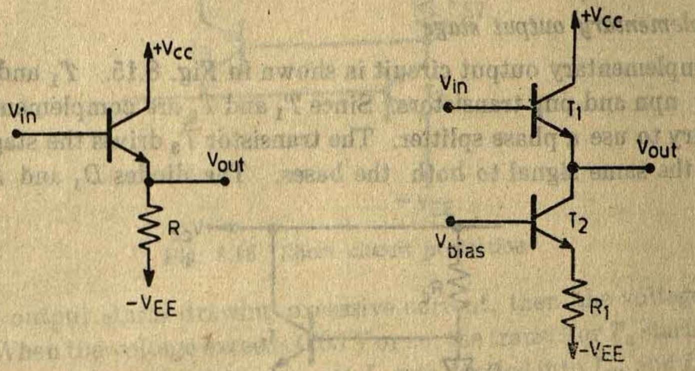
8.4 Output Circuit of Op-amp

Since the op-amps are d.c. coupled and are used to amplify signals even at very low frequencies including d.c., it is required that the $V_{out} = 0$ (d.c.) when

$V_{in} = 0$. The output impedance of the op-amp should be small. Sometimes it is also desired that this impedance is low both in 'source' and 'sinking' current flow directions. The above requirements can be met by many circuits and therefore there are as many designs of the output circuit. There are, however, three broad classes of circuits and we shall briefly describe their functions.

(i) *Emitter follower connection*

Emitter follower is known to have a high input impedance, low output impedance and a large current gain. For linear IC op-amps where the power required is small, the emitter follower is used to advantage. The circuit of an emitter follower is shown in Fig. 8.13 (a). The resistance R_E may be replaced by a constant current load as shown in Fig. 8.13(b). The transistor T_2 forms the constant current source as described in Fig. 8.10.



(a) Emitter follower

(b) RE replaced by constant current source

Fig. 8.13 Emitter follower output circuit

(ii) *Totem Pole Connection*

A totem pole output circuit is shown in Fig.8.14, Since the transistor T_1 sits over the top of transistor T_2, it is called a totem pole configuration. The transistor T_3 is the phase splitter. The signals at the collector and the emitter of T_3 are equal and in opposite phase. The bases of T_1 and T_2 are thus driven in opposite phase. As base of T_1 swings positive, T_1 acts as a 'source' of current flow and supplies current to R_L. T_2 is nearly cut off. Similarly when the signal swings negative, T_1 gets almost cut-off and T_2 'sinks' current from R_L. For a large positive swing T_1 will saturate and T_2 will be cut off leaving $V_{out} \simeq V_{CC}$. On the other hand, for a large negative swing T_2 will saturate and T_1 will cut off leaving $V_{out} \simeq -V_{EE}$. Thus the maximum swing possible at the output is from V_{CC} to $-V_{EE}$. Finally it must be remembered that negative feedback is applied across the output stage of this type of connection to stabilise the operation.

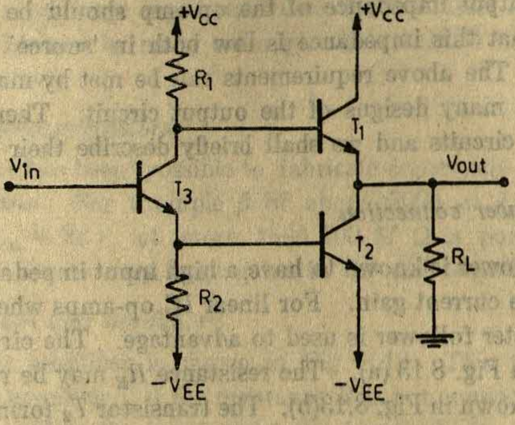


Fig. 8.14 Totem Pole output stage

(iii) Complementary output stage

A complementary output circuit is shown in Fig. 8.15. T_1 and T_2 are complementary npn and pnp transistors. Since T_1 and T_2 are complementary it is now not necessary to use a phase splitter. The transistor T_3 drives the stages T_1 and T_2 by feeding the same signal to both the bases. The diodes D_1 and D_2 provide a biasing so that T_1 and T_2 conduct in the quiescent conditions. As before the T_1 'sources' and T_2 'sinks' the current. Feedback for stability may or may not be used in these circuits. The complementary output stage described here is also used extensively in audio power amplifiers where the loudspeaker is connected in place of R_L. Depending upon the ratings of T_1 and T_2 tens of watts of power is obtained from this circuit.

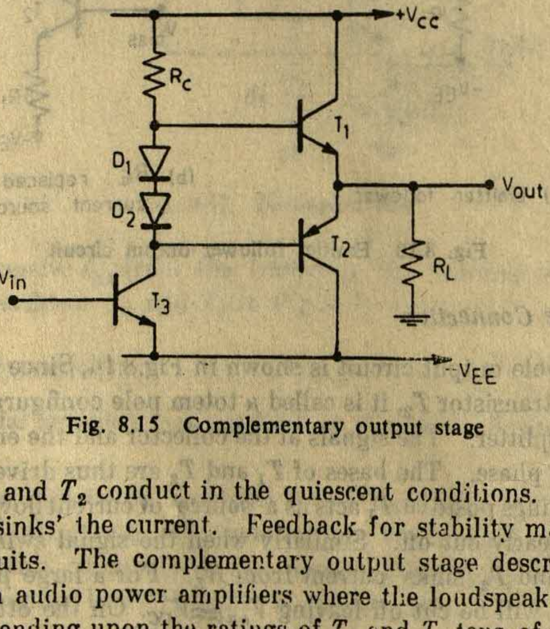


Fig. 8.15 Complementary output stage

In actual IC op-amps variations of these basic circuits may be used. While integrating the circuit in a small chip it is found easier to deposit a transistor than a large resistance and large capacitance. Biasing, constant current sources etc. therefore, look different in an IC amplifier though basically the functions remain the same.

In the circuit of Fig. 8.15, there is no current limiting resistance in the emitter of T_1. A short circuit protection or effect of current limitation is achieved by a modification of the circuit of Fig. 8.15 to one as shown in Fig. 8.16.

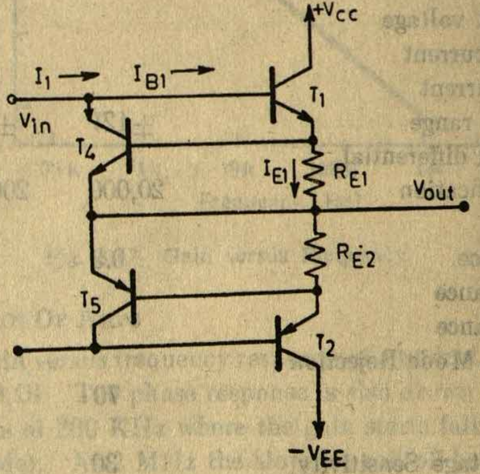


Fig. 8.16 Short circuit protection

If the output starts drawing excessive current, then the voltage across R_{E1} increases. When the voltage exceeds 0.65 V or so, the transistor T_4 starts conducting drawing a current I_{C4}. The drive current I_1 gets divided into I_{B1} and I_{C4} and hence the I_{E1} is limited. The action of T_5 and R_{E2} are similar.

8.5 Actual Op-Amps

We have so far discussed an ideal op-amp and some of the input and output circuits which are used to realise the op-amp. It is obvious that no practical circuit can be ideal and there will be some important deviations from the ideal and also notable imperfections in the op-amps available. Detailed specifications of a commercially available simple op-amp are given in Table 8.1

Table 8.1 Specifications of μA 741 Op-amp. Absolute maximum ratings over operating free air temperature range

1. V_{CC} Supply voltage	+ 18 V
2. V_{EE} Supply voltage	— 18 V
3. Differential input voltage	± 30 V
4. Input voltage (either input)	± 15 V
5. Voltage between either off-set null terminal (N_1 or N_2) and-V_{EE}	± 0.5 V
6. Duration of output short circuit	Unlimited
7. Temperature range (free air)	0 — 70°C
8. Continuous total power dissipation at 25°C	500 mW

B. *Electrical characteristics at* 25°C

$$V_{CC} = +15V$$

$$V_{EE} = -15V$$

	Min	Typical	Max	
1. V_{IO} Input offset voltage		1	6	mV
2. I_{IO} Input offset current		20	200	nA
3. I_{IB} Input bias current		80	500	nA
4. V_I Input voltage range	$\pm 12V$	$\pm 13V$		
5. A_{VD} Large-Signal differential voltage amplification ($R_L \geqslant 2K\Omega$)	20,000	200,000		
6. R_i Input resistance	0.3	2		M
7. R_O Output resistance		75		Ω
8. C_i Input capacitance		1.4		pf
9. CMRR Common Mode Rejection Ratio	70	90		dB
10. $\dfrac{\Delta V_{IO}}{\Delta V_{CC}}$ Supply voltage Sensitivity	30	150	150	μV/V
11. I_{OS} Short circuit output current		± 25	± 40	mA
12. I_{CC} Supply current		1.7	2.8	mA
13. P_D Power dissipation		50	80	mW
14. t_r rise time ($R_L = 2K\Omega$ $C_L = 100\,pf$)			0.3	μsec
15. Overshoot		5		percent
16. Slew rate at unity gain ($R_L = 2K\Omega$ $C_L = 100$ pf)		0.5		V/μs

Two additional data are given in the form of a graph. They are CMRR vs. frequency and A_{VD} vs. frequency. Above about 100 Hz, the CMRR falls at the rate of about 20 dB/decade change of frequency. Thus, starting with a value of 75 dB at say 1 KHz, it goes down to 55 db at 10 KHz and becomes 18 dB approximately at 1 MHz.

The open loop large signal differential gain also decreases at the rate of 6 dB/octave or 20 dB/decade as shown in Fig. 8.17. $A_{VD} = 1$ at 1 MHz for μ A741 op-amp. This particular op-amp is also internally compensated, that is, if a large amount of negative feedback is given, the op-amp will not oscillate. Many op-amps do require external compensation and let us see why is it so.

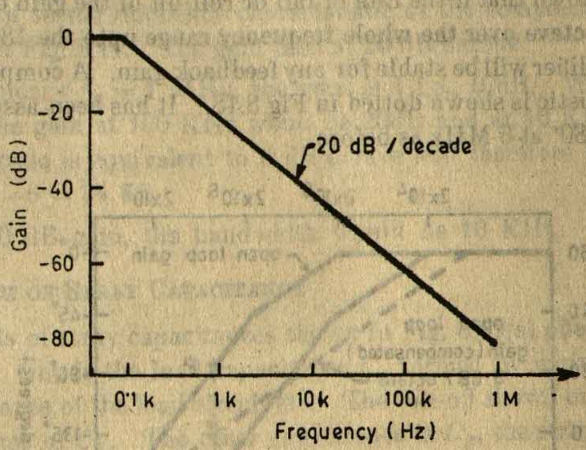


Fig. 8.17 Gain versus Frequency

8.5.1 COMPENSATION IN OP-AMPS

The open loop gain versus frequency response of a typical uncompensated op-amp is shown in Fig. 8.18. The phase response is also drawn on the same graph. The first break point is at 200 KHz where the gain starts falling at the rate of 6 dB/octave (20 dB/decade). At 2 MHz the slope or roll-off becomes 12 dB/octave (40 dB/decade) and at 20 MHz it is 18 dB per octave. The phase changes at 0.2, 2 and 20 MHz are — 45°,135° — and — 225° respectively.

In a negative feedback connection, there is already an inversion from the input to the output at the low frequencies and the phase change is 180°. As the frequency increases the op-amp produces an extra phase shift which only has been shown in Fig. 8.18. Thus at the frequency of, say, f_C the additional phase shift of the op-amp itself is —180°. The feedback signal will become in phase with the input at f_C and an effective positive feedback will be produced. If the gain of the amplifier is more than unity at f_C the circuit will oscillate and become unstable. For the feedback amplifier to be stable it is essential that the loop gain is less than unity when the total phase change in the circuit is 0° or 360°. Loop gain is defined as the ratio of the open-loop gain to the closed-loop gain.

In the Fig. 8.18, the phase change of 180° occurs at $f_C = 6$ MHz when the open-loop gain is about 20 dB. As a general rule the op-amp will oscillate if the chosen closed-loop gain is equal to or less than the open-loop gain at the 180° phase shift point. In the example above, therefore, the op-amp circuit will be unstable if a closed loop gain of 20 dB or less is used. If the closed loop gain is chosen to be more than 20 dB the circuit will remain stable. A frequency plot of the type shown in Fig. 8.18 indicates the maximum amount of feedback that can be used in the op-amp. The amplifier gain with feed-back is selected to be larger than the open-loop gain at 180° phase shift point.

It has been shown that if the rate of fall or roll-off of the gain characteristics is limited to 6 db/octave over the whole frequency range upto the 180° phase shift point, then the amplifier will be stable for any feedback gain. A compensated open-loop gain characteristic is shown dotted in Fig 8.18. It has been assumed that the phase changes by 180° at 6 MHz as before.

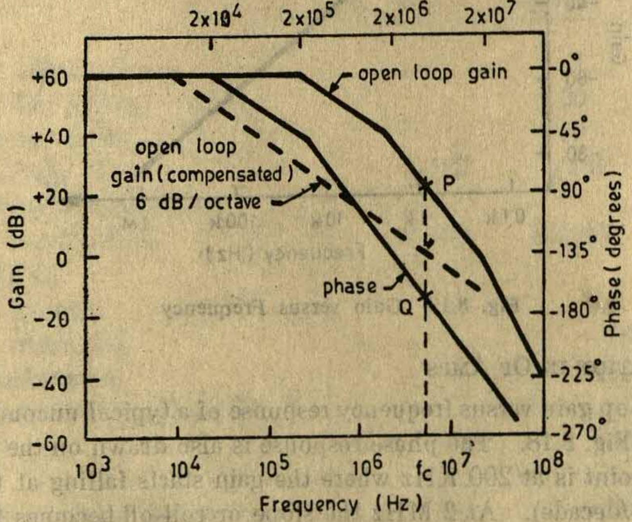


Fig. 8.18 Open loop gain and phase response with frequency of an operational amplifier.

Actually the basic requirement of the frequency compensating network is to keep the roll-off of the loop gain from exceeding 12 dB/octave when the loop gain is near or approaches unity. The gain and phase versus frequency behaviour will be subject to the variations due to temperature drift or individual variations from unit to unit. A certain amount of margin in both phase and gain is selected while designing the compensating network to ensure that the circuit will not oscillate in the worst case. A phase margin of 30° to 45° and a gain margin of 10 dB is quite common. It will, thus, mean that f_C is chosen to be a frequency where the phase change is $-135°$ instead of $-180°$. This will give a phase margin of 45°.

A discussion of the compensating technique used to obtain a roll-off of 6 dB/octave throughout the frequency band of interest is beyond the scope of this book. Manufacturers normally specify the external compensation to be used if the op-amp is not internally compensated.

Example 8.5.1

An op-amp has an open loop gain of 10^5 and a unity gain-bandwidth of 1 MHz. To prevent oscillation, the amplifier is internally compensated so as to give a roll-off of 20 dB/decade. If the amplifier is to have a bandwidth of 20 KHz, what is the available gain? What would be the bandwidth of the amplifier if a gain of 40 dB is required?

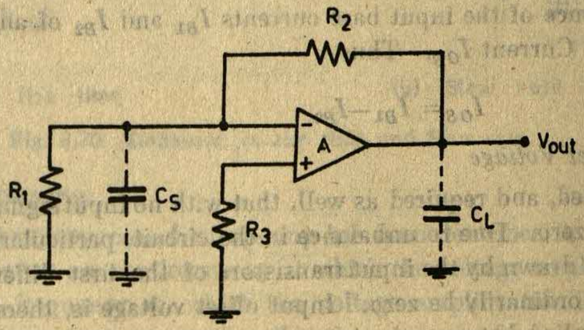
The gain versus frequency characteristic of the compensated op-amp would be like that in Fig. 8.17. The gain falls at 20 dB/decade.

At frequency $f_T = 1$ MHz, the gain is 1 i.e., 0 dB. With a roll-off of 20 dB/decade, the gain at 100 KHz woud be 20dB and at 10 KHz it would be 40 dB. 20 dB decade is equivalent to 6 dB/octave and therefore the gain at 20 KHz would be 40−6 = 34 dB.

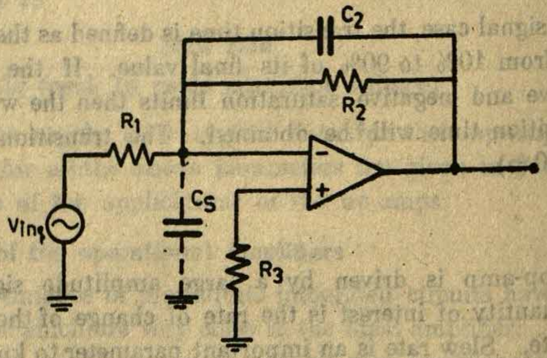
With 40 dB gain, the bandwidth would be 10 KHz.

8.5.2 Effect of Stray Capacitance

Two sets of stray capacitances shown in Fig. 8.19(a) effect the behaviour of the op-amp. One is the load capacitance C_L formed by wiring capacitances and input capacitance of the load circuit etc. The roll-off shown in Fig. 8.18 is effected by the presence of C_L. The other capacitance is C_S, the stray capacitance at the inverting input. The effect of this C_S is compensated by a lead capacitor C_2 connected across R_2 as shown in Fig. 8.19 (b). The value of C_2 is so adjusted that



(a) Stray capacitances C_L and C_S



(b) Lead compensation

Fig. 8.19 Compensation of stray Capacitances.

$R_1C_S = R_2C_2$ or $C_2 = (R_1/R_2)\ C_S$ Normally a C_2 larger than the value indicated above can also be used but the amplifier bandwidth will become less in such a case.

8.5.3 OTHER PARAMETERS OF THE OP-AMPS

Before we go into the applications of the op-amps we shall mention some of their other important parameters.

(*i*) *Input Bias Current*

The average of the input base currents I_{B1} and I_{B2} of the op-amp is called the Input Bias Current I_{BIAS}. Thus

$$I_{BIAS} = \frac{I_{B1} + I_{B2}}{2} \tag{8.34}$$

(*ii*) *Input Offset Current*

The difference of the input base currents I_{B1} and I_{B2} of an op-amp is called the Input Offset Current I_{OS}. Thus

$$I_{OS} = I_{B1} - I_{B2} \tag{8.35}$$

(*iii*) *Input Offset Voltage*

It is expected, and required as well, that with no input signal, the d.c. voltage at the output is zero. Due to unbalance in the circuit, particularly because of the unequal currents drawn by the input transistors of the first differential amplifier, the V_O will not ordinarily be zero. Input offset voltage is, therefore, the voltage that must be applied between the input terminals to obtain $V_O = 0$

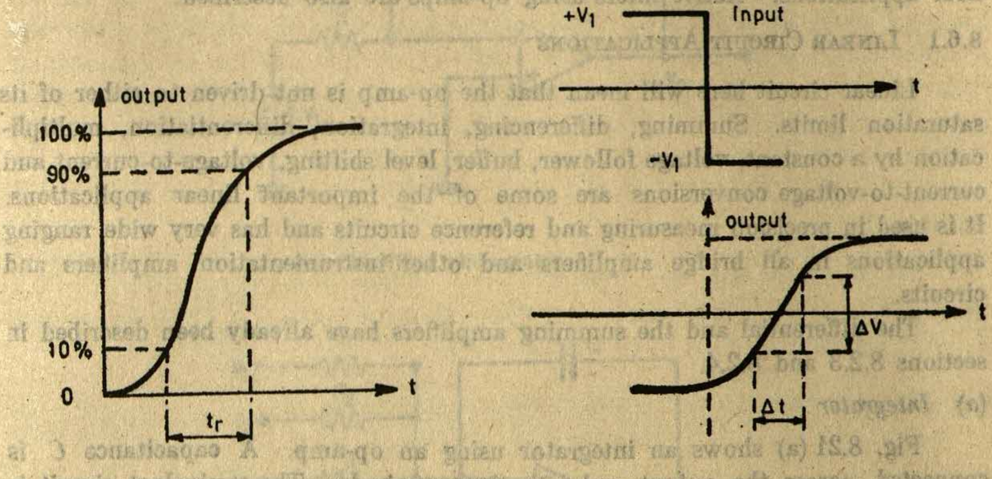
(*iv*) *Transition time*

For a small signal case, the transition time is defined as the time taken for the output to rise from 10% to 90% of its final value. If the op-amp is driven between its positive and negative saturation limits then the worst or the largest value of the transition time will be obtained. The transition or rise time t_r is shown in Fig. 8.20 (a)

(*v*) *Slew rate*

When the op-amp is driven by a large amplitude signal of a step or a pulse type, the quantity of interest is the rate of change of the output with time called the Slew rate. Slew rate is an important parameter to know when a square wave signal is connected to the input of the op-amp. Slew rate is defined as the internally limited rate of change of the output voltage $\Delta V/\Delta t$ when a large amplitude step function is applied to its input as shown in Fig. 8.20 (b). Slew rate is specified in terms of $V/\mu\text{sec}$. Fast amplifiers have slew rates of the order of

1500 V/μsec whereas amplifiers meant for low frequency work may have slew rates of 0.1 V/μsec. To conclude, therefore, we can say that slew rate tells us how fast the amplifier output can change from one voltage level to another.



(a) Transtion or rise time (b) Slew rate

Fig. 8.20 Definition of rise time and Slew rate.

(*vi*) *Frequency response*

The frequency response of an op-amp has been described in Fig. 8.17. Two important parameters are the frequency at which the voltage amplification reduces by 3 db and the frequency at which the voltage amplification is unity or 0 dB. There is a third frequency parameter called the maximum frequency of full output swing. This is the frequency where we expect the response to be limited by the slew rate. It is defined as

$$f_{o\,(max)} = \frac{\text{Slew rate}}{2\pi\ (\text{peak to peak saturation voltage})} \tag{8.36}$$

Manufacturers supply these typical data for their op-amps. Thus for the μA 741 the figures for all the above parameters are given in Table 8.1. We shall now take up some of the applications of the op-amps.

8.6 Applications of the operational Amplifiers

Advanced techniques of monolithic integrated circuits have made it possible to realise amplifiers which are very close to the ideal amplifier. The low cost and high quality of these amplifiers makes possible easy implementation of equipment and systems which were not possible with the discrete circuit amplifiers. Other than linear circuits, the op-amps have also been used in nonlinear circuits like wave shaping, multivibrators, and trigger circuits etc. Circuit application notes are supplied by the manufacturers or compiled by others in book form to help the users design circuits conveniently. In this section we shall briefly describe some of the common usage and applications of op-amps. The list by its nature cannot be exhaustive and is simply illustrative. We shall take up both linear and nonlinear applications. Active filters using op-amps are also described.

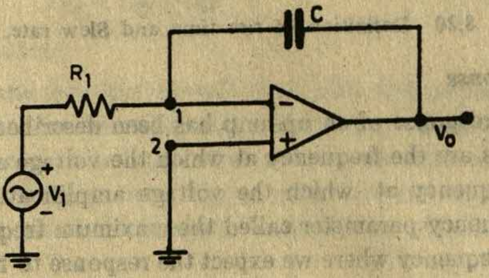
8.6.1 LINEAR CIRCUIT APPLICATIONS

Linear circuit here will mean that the op-amp is not driven to either of its saturation limits. Summing, differencing, integration, differentiation, multiplication by a constant, voltage follower, buffer, level shifting, voltage-to-current and current-to-voltage conversions are some of the important linear applications. It is used in precision measuring and reference circuits and has very wide ranging applications in all bridge amplifiers and other instrumentation amplifiers and circuits.

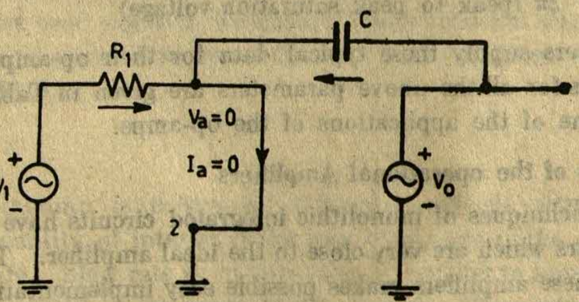
The differential and the summing amplifiers have already been described in sections 8.2.3 and 8.2.4.

(a) Integrator

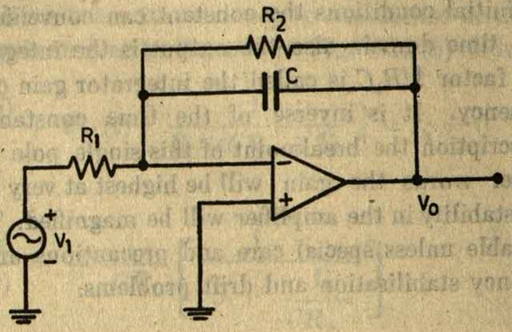
Fig. 8.21 (a) shows an integrator using an op-amp. A capacitance C is connected across the output and inverting terminals. The equivalent circuit is



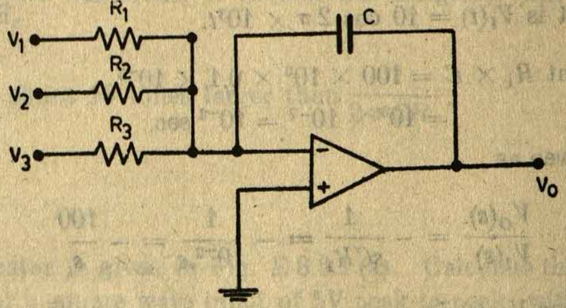
(a) Simple integrator



(b) Equivalent circuit



(c) Modified integrator



(d) Summer integrator

Fig. 8.21 Integrator Circuits

shown in Fig. 8.21 (b). Analysing the circuit by assuming an ideal amplifier with $A = \infty$ we have

$$I_a = \frac{V_1\,(s)}{R_1} + \frac{V_o\,(s)}{(1/sC)} = o$$

hence

$$\frac{V_O(s)}{V_1\,(s)} = -\,\frac{1}{sCR_1} \tag{8.37}$$

This is an integrator.

Taking the inverse Laplace Transform

$$V_O(t) = -\,\frac{1}{R_1\,C}\int_0^T V_1\,\mathrm{dt} + \text{Constant} \tag{8.38}$$

Depending on the initial conditions the constant can conveniently be assumed to be zero. Thus, in time domain also the output is the integrated version of the input signal. The factor $1/R_1C$ is called the integrator gain constant and has the dimension of frequency. It is inverse of the time constant R_1C. In the frequency domain description the breakpoint of this single pole circuit is at the zero frequency. In other words the gain will be highest at very low frequencies and thus any drift or instability in the amplifier will be magnified. The circuit therefore may not be very stable unless special care and precautions are taken to reduce the very low frequency stabilisation and drift problems.

Example 8.6.1

An integrator has the resistance $R_1 = 100K\Omega$ and the capacitor $C = 0.1$ microfared. Obtain the transfer function of the integrator. Find the output $V_O(t)$ if the input is $V_i(t) = 10 \cos 2\pi \times 10^3 t$.

The time constant $R_1 \times C = 100 \times 10^3 \times 0.1 \times 10^{-6}$

$$= 10^5 \times 10^{-7} = 10^{-2} \text{ sec.}$$

The transfer is given as

$$\frac{V_O(s)}{V_1(s)} = -\frac{1}{sCR_1} = -\frac{1}{10^{-2}.s} = -\frac{100}{s}$$

The output voltage $V_O(t)$ is

$$V_O(t) = -\frac{1}{R_1C}\int_0^T V_1(t).\,dt + \text{Constant}$$

$$= -10^2\int_0^T 10 \cos wt.\,dt \qquad \text{assuming constant} = 0$$

$$= -10^2 \times 10\frac{\sin \omega t}{\omega}$$

$$= \frac{-10^3}{\omega}\sin \omega t$$

$$= -\frac{10^3}{2\pi \times 10^3}\sin \omega t$$

or $V_O(t) = -0.159 \sin \omega t$

If it is not absolutely essential to integrate at very low frequencies, the circuit of Fig. 8.21 (a) can be modified to that of Fig. 8.21 (c). Inclusion of R_2 across

C stabilises the amplifier hence its tendency to destabilise or drift is reduced considerably. An analysis similar to the one in Fig. 8.21 (b) shows that

$$\frac{V_1(S)}{R_1} + V_O(s)\left[\frac{1}{R_2/(sCR_2+1)}\right] = I_a = 0$$

Hence

$$\frac{V_o(s)}{V_1(s)} = -\frac{1}{CR_1}\left[\frac{1}{S + \frac{1}{CR_2}}\right] \tag{8.39}$$

Comparing eq. (8.39) with (8.37) we see that the pole at the origin or d.c. is shifted to a frequency $\frac{1}{CR_2}$. As a rule of thumb, this integrator will perform well at input frequencies about 10 times larger than $\frac{1}{2\pi CR_2}$.

Example 8.6.2

A practical integrator is given in Fig. E 8.6.1 (a). Calculate the breakpoint and find the output for a square wave input of 5V peak-to-peak with 1 KHz repetition frequency. What should be the value of R_3 ?

The breakpoint is calculated as

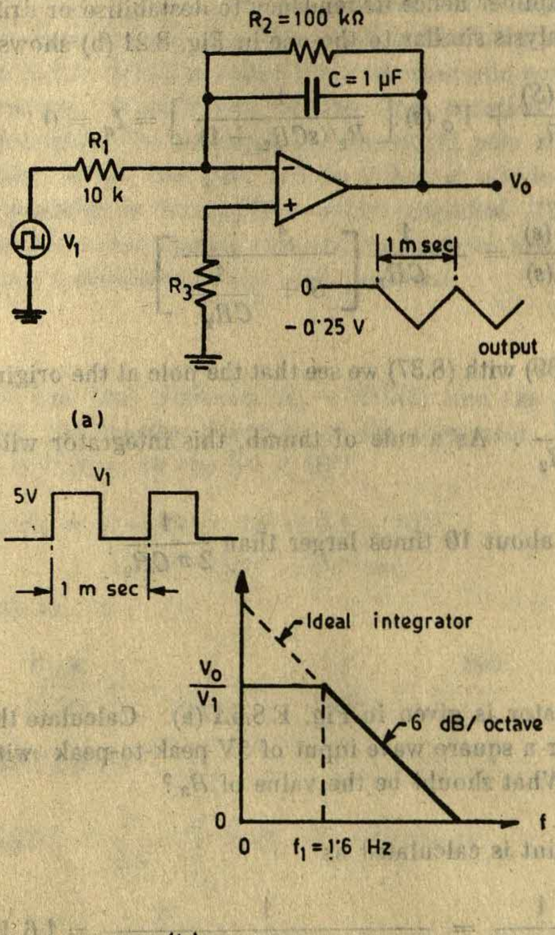
$$\frac{1}{2\pi CR_2} = \frac{1}{2\pi \times 1 \times 10^{-6} \times 0.1 \times 10^6} = 1.6 \text{ Hz}$$

The frequency response of this integrator is shown in Fig. E 8.61(b). The ideal integrator of Fig. 8.21 (a) has a break point at d.c. and is shown dotted in this figure. Thus, this integrator will integrate at frequencies upto 20 Hz.

For the square wave input, the time period T is 1 m sec. It is assumed that the input changes abruptly to 5V and remains so for $T/2$ sec. At sufficiently higher frequencies, higher than 1.6 Hz, the eq. (8.39) can be approximated as

$$\frac{V_O(s)}{V_1(s)} \approx -\frac{1}{sCR_1}$$

$$\text{hence } V_O(t) = -\frac{1}{R_1C}\int_0^T V_1(t)\, dt + \text{const}$$



(a)

(b)

Fig. E 8.6.1

For the values given, therefore

$$V_O(T/2) = -\frac{1}{0.01 \times 10^6 \times 1 \times 10^6} \int_0^{T/2} 5 \, dt.$$

$$= -500 \ (T/2)$$

$$= -0.25 \text{ Volts.}$$

The output will rise linearly by 0.25 V in ½ msec and in the next ½ msec it will decrease by 0.25 V. Hence the output will be an integrated version of the input signal.

For minimum error in the input bias current, it is good to make R_3 equal to the parallel combination of R_2 and R_1. Thus $R_3 = 9.1$ KΩ.

The circuit in Fig. 8.21 (d) is a summing integrator. The output can be easily calculated as

$$V_O(t) = -\int_0^t \left[\frac{1}{CR_1}V_1 + \frac{1}{CR_2}V_2 + \frac{1}{CR_3}V_3\right] dt + V_O(0)$$

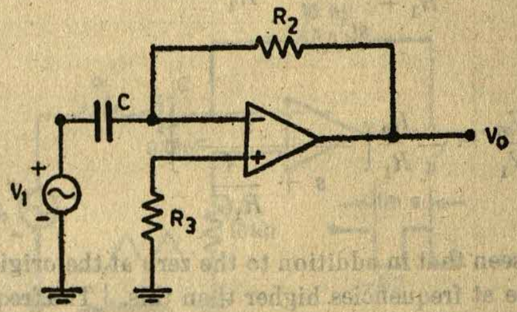
or

$$V_O(t) = -\frac{1}{C}\int_0^t \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) dt + V_O(0) \qquad (8.40)$$

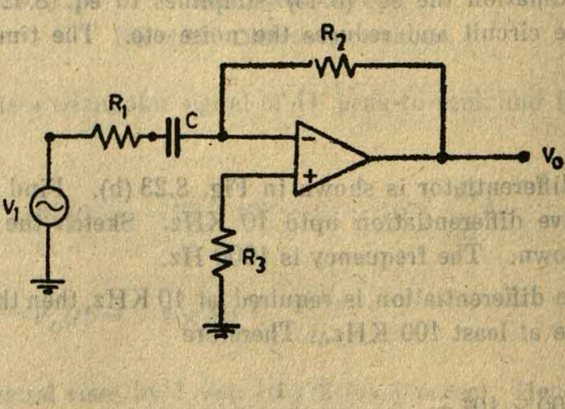
where $V_O(0)$ is the initial voltage on the capacitance at $t = 0$. While designing and operating this circuit, care should be taken to see that the output does not exceed the ratings.

(*b*) *Differentiator*

The differentiator circuit is shown in Fig. 8.22(a)



(a) Ideal circuit



(b) Practical circuit

Fig. 8.22 Differentiator

The analysis of the circuit gives

$$\frac{V_1(s)}{1/sC} = -\frac{V_O(s)}{R_2}$$

or
$$\frac{V_O(s)}{V_1(s)} = -sC.\ R_2 \tag{8.41}$$

and
$$V_O(t) = -R_2C.\ \frac{dV_1}{dt} \tag{8.42}$$

Thus the input signal is differentiated at the output. This circuit suffers from a major drawback of accentuating or amplifying high frequency noise signals. A practical differentitor is shown in Fig. 8.22 (b). Here

$$\frac{V_1}{R_1 + \frac{1}{sC}} = -\frac{V_O}{R_2}$$

Rewriting

$$\frac{V_O}{V_1} = -\frac{R_2}{R_1}\left[\frac{s}{s + \frac{1}{R_1C}}\right] \tag{8.43}$$

From eq. (8.43) it is seen that in addition to the zero at the origin, a pole at $1/R_1C$ levels off the response at frequencies higher than this. The frequency response is shown in Fig. 8.23(a). The frequency $1/2\pi R_1C$ is normally kept much higher (about 10 times) than the frequency of the signal to be differentiated.
Under this approximation the eq. (8.43) simplifies to eq. (8.42). The pole at $1/R_1C$ stabilises the circuit and reduces the noise etc. The time constant is as before R_2C.

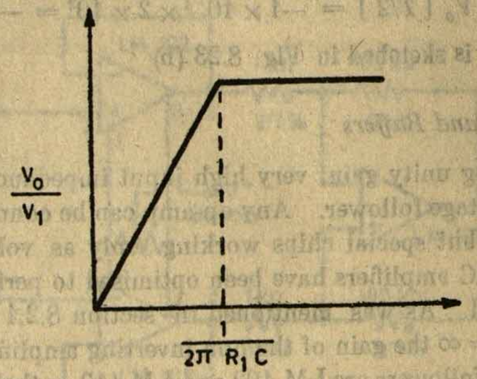
Example 8.6.3

A practical differentiator is shown in Fig. 8.23 (b). Find the value of R_1 to give an effective differentiation upto 10 KHz. Sketch the response for a triangular input shown. The frequency is 1000 Hz.

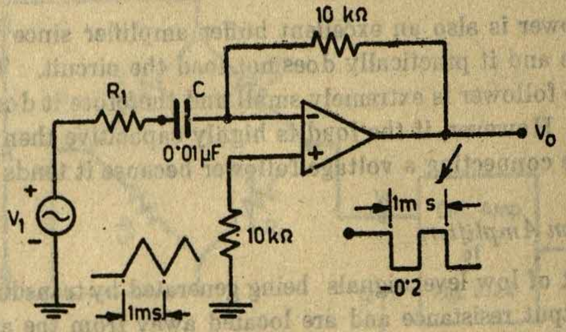
If an effective differentiation is required at 10 KHz, then the break point at $1/2\pi R_1C$ should be at least 100 KHz. Therefore

$$100 \times 10^3 = \frac{1}{2\pi R_1 \times 0.01 \times 10^{-6}}$$

or $R_1 \simeq 160$ ohms



(a) Frequency response



(b) Actual circuit

Fig. 8.23 Differentiator circuit.

The input signal is a triangular signal of $1V$ peak-to-peak and frequency 1 KHz. From eq. (8.42).

$$V_O(t) = -10 \times 10^3 \times .01 \times 10^{-6}. \frac{dV_1}{dt}$$

or
$$V_O(t) = -1 \times 10^{-4}. \quad \frac{dV_1}{dt}$$

Now the input signal rises by 1 volt in $T/2$ $(= \frac{1}{2}$ m.sec) Hence

$$\frac{dV_1}{dt} = \frac{1}{0.5 \times 10^{-3}} = 2 \times 10^3$$

Thus $V_o\,[T/2] = -1 \times 10^{-4} \times 2 \times 10^3 = -0.2$ Volts

The response is sketched in Fig. 8.23 (b)

(*c*) *Voltage Followers and Buffers*

An op-amp having unity gain, very high input impedance and large bandwidth is known as a voltage follower. Any op-amp can be connected in a voltage-follower configuration but special chips working only as voltage followers are also available. These IC amplifiers have been optimised to perform the function of voltage follower well. As was mentioned in section 8.2.1 and eq. (8.2) that if either $R_2 = 0$ or $R_1 = \infty$ the gain of the non-inverting amplifier is unity. Some of the common voltage followers are LM 102 and LM 110 or their equivalents. For example the input bias current in LM 110 is 10 nA with a slew rate of 40 V/μsec. and a bandwidth of 20 MHz. The input resistance of LM 110 = 10^{12} ohms, and output resistance = 0.75 ohm. Voltage followers having bandwidths of 200 MHz and more have been marketed.

Voltage follower is also an excellent buffer amplifier since its input impedance is very large and it practically does not load the circuit. The output impedance of a voltage follower is extremely small and therefore it does not get loaded by other circuits. However, if the load is highly capacitive then the designer has to be careful while connecting a voltage follower because it tends to oscillate.

(*d*) *Instrumentation Amplifiers*

Measurement of low level signals being generated by transducers, which have normally high output resistance and are located away from the amplifier circuits, cannot be performed by single input—single output op-amps. It is essential to use differential amplifiers with high CMRR, adequate gain and input impedance. Instrumentation amplifiers carefully designed, wired and used can perform these measurement functions adequately. A typical differential instrumentation amplifier with voltage followers in the input circuit is shown in Fig. 8.24. The output of the voltage followers LM102 are fed to LM107 which is the operational amplifier giving the gain.

The differential amplifier is often used to amplify the output of a bridge circuit. Thus the amplifier of Fig. 8.24 could be connected across a bridge circuit as shown in Fig. 8.25. The unbalanced signal across the detector arm of the bridge is conneted to the differential amplifier. The Wheatstone bridge is balanced when

$$R_1 R_4 = R_2 . R_3 \tag{8.44}$$

or $$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

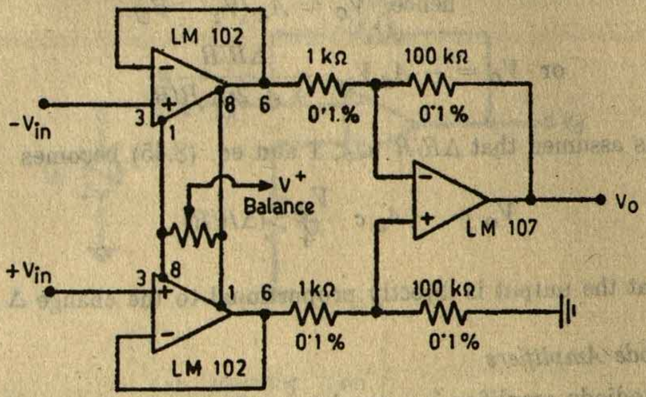


Fig. 8.24 Instrumentation Amplifier

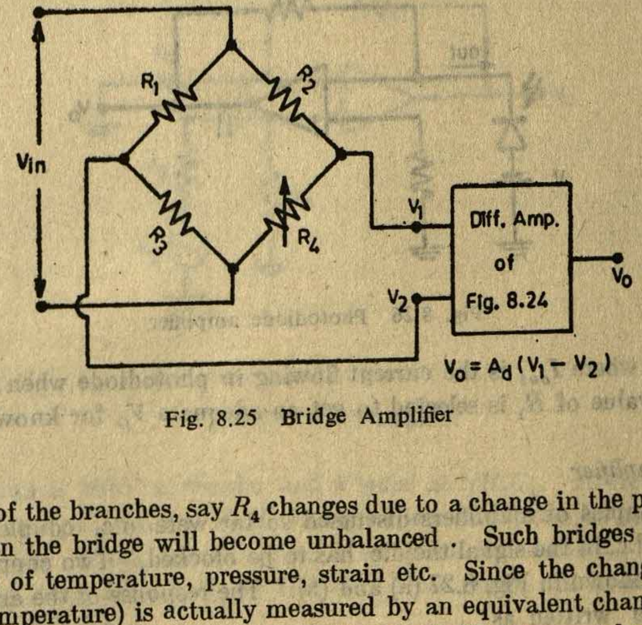


Fig. 8.25 Bridge Amplifier

Now, if any of the branches, say R_4 changes due to a change in the parameter being measured then the bridge will become unbalanced . Such bridges are used in the measurement of temperature, pressure, strain etc. Since the change in the parameter (say temperature) is actually measured by an equivalent change in the resistance R_4, the bridge, therefore, measures the ($\Delta R_4/R_4$) accurately.

If we assume, in the circuit of Fig. 8.25, that $R_1 = R_2 = R_3 = R_4 = R$ then

$$V_1 = \frac{V_{in}\,(R + \Delta R)}{2R + \Delta R}$$

$$\text{and} \quad V_2 = V_{in} \cdot \frac{1}{2}$$

$$\text{hence} \quad V_O = A_d\,(V_1 - V_2)$$

$$\text{or} \quad V_O = -\,A_d\,V_{in}\cdot\frac{\Delta R/R}{4 + 2\,\Delta\,R/R} \tag{8.45}$$

It is assumed that $\Delta R/R << 1$ and eq. (8.45) becomes

$$V_O = -\,A_d\,c\,\frac{V_{in}}{4}\,(\Delta R/R) \tag{8.46}$$

It is seen that the output is directly proportional to the change $\Delta\,R$.

(*c*) *Photodiode Amplifiers*

A photodiode amplifier is a good example of current to voltage conversion. A simple circuit of a photodiode amplifier is shown in Fig. 8.26. The output

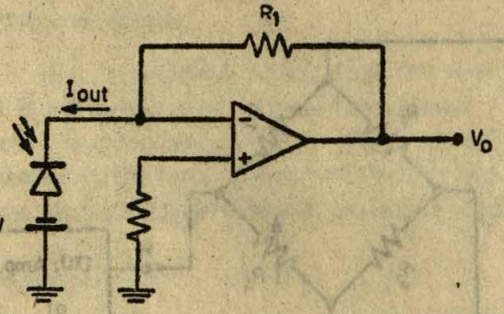


Fig. 8.26 Photodiode amplifier

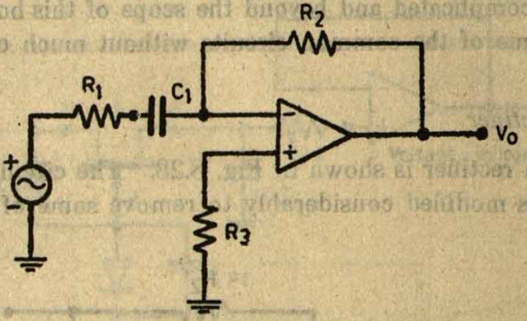
$V_O = R_1\,I_{out}$ where I_{out} is the current flowing in photodiode when light shines on it. Suitable value of R_1 is selected to get an adequate V_O for known I_{out}.

(*f*) *A. C. Amplifier*

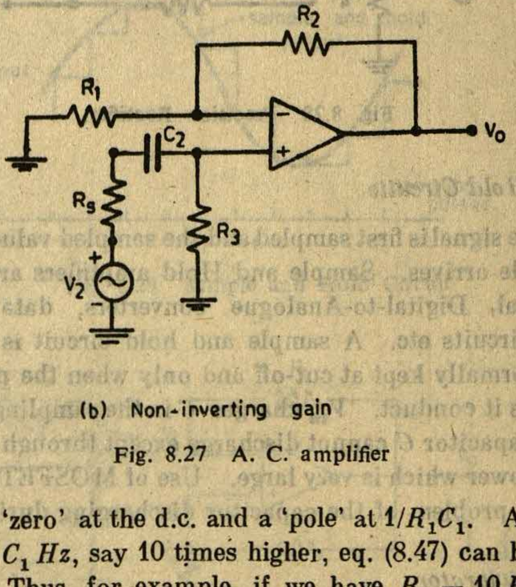
The examples of amplifiers discussed so far were d.c. coupled. Whenever there is a net d.c. in the signal the d.c. has to be blocked. Two connections of a.c. amplifiers are shown in Fig. 8.27 (a) and (b). The response of the amplifier in Fig. 8.27 (a) can be written as

$$\frac{V_O\,(s)}{R_2} + \frac{V_1\,(s)}{R_1 + \dfrac{1}{sC_1}} = 0$$

$$\text{or} \quad \frac{V_O\,(s)}{V_1\,(s)} = -\,\frac{R_2}{R_1}\cdot\left[\frac{s}{s + \dfrac{1}{R_1\,C_1}}\right] \tag{8.47}$$



(a) Inverting gain



(b) Non-inverting gain

Fig. 8.27 A. C. amplifier

Eq. (8.47) shows a 'zero' at the d.c. and a 'pole' at $1/R_1C_1$. At frequencies much higher than $1/2\pi\ R_1\ C_1\ Hz$, say 10 times higher, eq. (8.47) can be approximated as $V_O/V_1 = -R_2/R_1$. Thus, for example, if we have $R_1 = 10\,K\Omega$, $R_2 = 100\,K\,\Omega$, and $C_1 = 0.1\mu f$, then $1/2\pi\ R_1\ C_1 \approx 160$ Hz. This gives the lower 3db break-point at about 160 Hz.

Similarly the lower 3 db breakpoint in the case of the non-inverting configuration of Fig. 8.27 (b) is $1/2\pi\ (R_S+R_3)\ C_2$ where R_s is the source resistance of V_2. Above this frequency the gain will be $(1+R_2/R_1)$ as before.

8.6.2 NON-LINEAR CIRCUIT APPLICATIONS

Like the linear circuits, the op-amps have large number of applications in nonlinear circuits also. But unlike the linear circuits, the analysis of the non-linear circuits is more complicated and beyond the scope of this book. We shall, therefore, describe some of the common circuits without much comment.

(*a*) *Precision rectifier*

A precision rectifier is shown in Fig. 8.28. The circuit suffers from many drawbacks and is modified considerably to remove some of them.

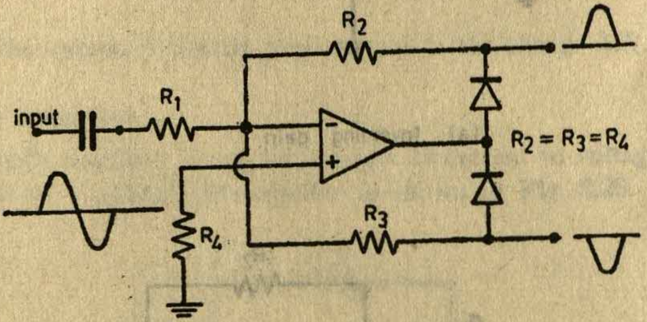


Fig. 8.28 Precision Rectifier

(*b*) *Sample and Hold Circuits*

The analogue signal is first sampled and the sampled value is held in a capacitor till the next sample arrives. Sample and Hold amplifiers are used extensively in Analogue-to-Digital, Digital-to-Analogue converters, data multiplexing, and pulse stretching circuits etc. A sample and hold circuit is shown in Fig. 8.29. The FET T_1 is normally kept at cut-off and only when the positive going sample pulse arrives does it conduct. V_{in} charges C in the sampling interval. Once the T_1 is cut-off, the capacitor C cannot discharge except through the input impedance of the voltage follower which is very large. Use of MOSFETs of high input impedance reduces the problem of the capacitor discharging during the hold period.

(*c*) *Astable Multivibrator*

Astable multivibrator denotes a circuit which oscillates between two states on its own, at rates governed by the RC combination in the circuit. It is a free running circuit and produces a square wave signal at the output. A free runing or astable multivibrator is shown in Fig. 8.30.

The voltage V_2 is

$$V_2 = \alpha V_O$$

$$\text{or} \quad V_2 = \frac{R_3}{R_2 + R_3} V_O \tag{8.48}$$

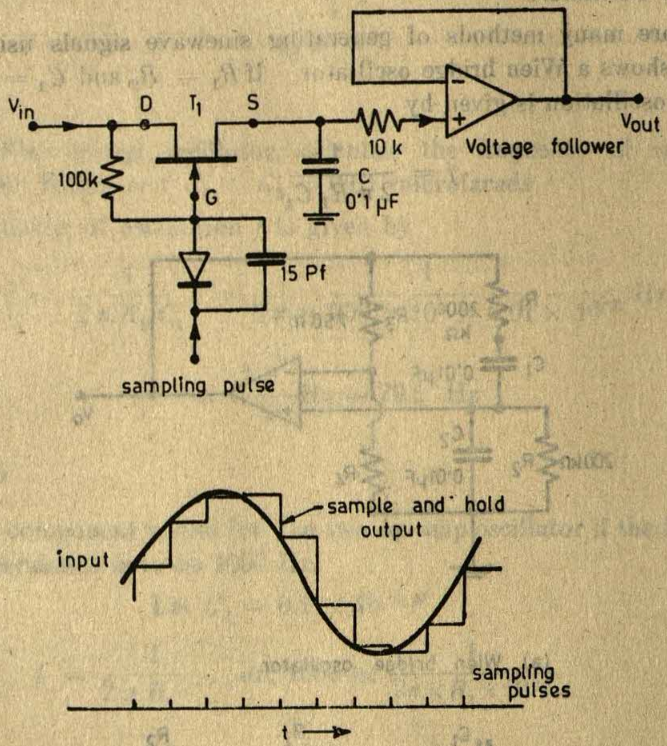


Fig. 8.29 Sample and Hold Circuit

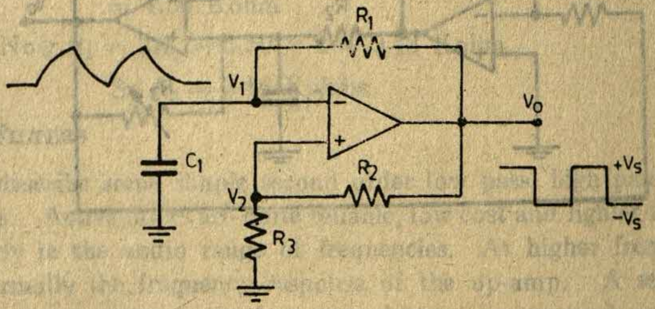


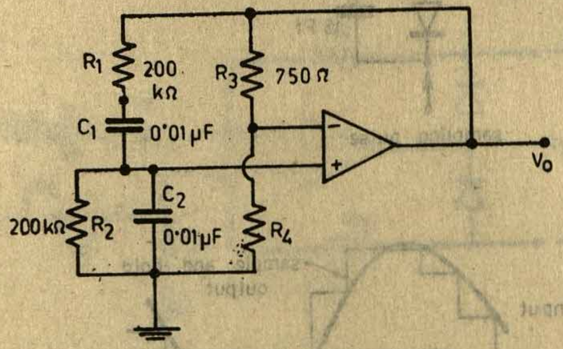
Fig. 8.30 Astable or Free running Multivibrator

Assuming that the output of the op-amp saturates at $\pm V_S$ volts, whenever V_1 becomes equal to or exceeds $\pm \alpha V_S$ the op-amp switches to the other state. The voltage across C_1 is either charging or discharging exponentially. The frequency of the square wave output is restricted to about 5 KHz, though for frequencies lower than these the circuit behaves very well. If α is chosen as 0.473 then the time period of the square wave is $T = 2 R_1 C_1$.

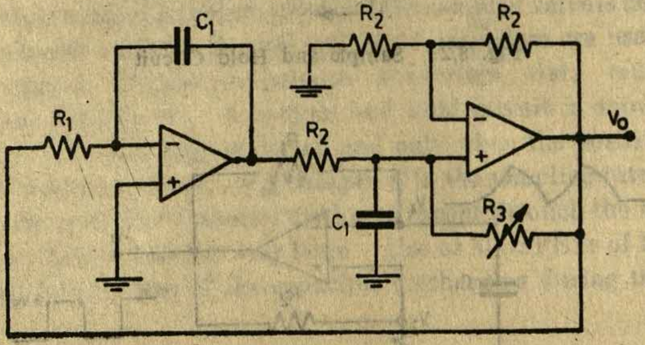
(*d*) *Sinewave Oscillators*

There are many methods of generating sinewave signals using op-amps. Fig. 8.31 (a) shows a Wien bridge oscillator. If $R_1 = R_2$ and $C_1 = C_2$, then the frequency of oscillation is given by

$$f = \frac{1}{2\pi R_1 C_1} \tag{8.49}$$



(a) Wien bridge oscillator



(b) Two op-amp oscillator

Fig. 8.31 Sinewave oscillators

The resistance R_4 is a lamp or some other non-linear resistance which changes in magnitude (increases) as the signal voltage across it increases. As V_0 increases the R_4 increases and more negative feedback is given thereby reducing the amplitude. In the circuit of Fig. 8.31 (b), normally, $R_2 = 2R_1$ and $R_3 = R_2$ and is kept adjustable for regeneration. The frequency of oscillation is

$$f = \frac{1}{2\pi R_1 C_1}$$

Example 8.6.4

For a Wien bridge oscillator, calculate the frequency of oscillation if $R_1 = R_2 = 200$ Kohm and $C_1 = C_2 = 0.01$ microfarads

The frequency of oscillation f is given by

$$f = \frac{1}{2\,\pi R_1 C_1} = \frac{1}{2\,\pi \times 200 \times 10^3 \times 0.01 \times 10^{-6}} \text{ Hz}$$

$$= \frac{10^3}{4\pi} \text{Hz} = 79.5 \text{ Hz}$$

Example 8.6.5

Find the component values for the two op-amp oscillator if the frequency of the sinewave generated is to be 1000 Hz.

$$\text{Let } C_1 = 0.1 \times 10^{-6} F$$

$$\text{Now} \quad f = \frac{1}{2\,\pi R_1 C_1}, \text{ or, } 1000 = \frac{1}{2\pi \times R_1 \times 10^{-7}}$$

$$\text{or} \quad R_1 = \frac{10^7}{2\,\pi \times 10^3} = \frac{10^4}{2\,\pi} = \frac{5}{\pi}$$

$$= 1.59 \text{ Kohm}$$

$$\text{Now } R_1 = 2R_2 = 1.59 \times 2 = 3.18 \text{ Kohm}$$

$$\text{So } R_3 = 3.18 \text{ Kohms}$$

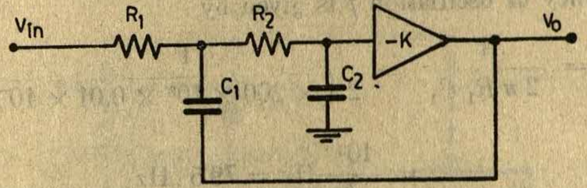
8.6.3 ACTIVE FILTERS

We shall describe some simple second order low pass, high pass and band-pass active filters. Active filters are quite reliable, low cost and lighter than passive filters particularly in the audio range of frequencies. At higher frequencies the limitation is normally the frequency response of the op-amp. A second order filter will have two capacitors in the frequency determining network and will have a response which falls at the rate of 12 dB/octave or 40 dB/decade. A noninverting lowpass filter is shown in Fig. 8.32 (a). Among the popular active filters K is either 1 or 2. Fig. 8.32 (b) shows a low pass filter with A=K=1. The resistances are kept equal. For a Butterworth maximally flat filter the values of C_1 and C_2 are obtained as

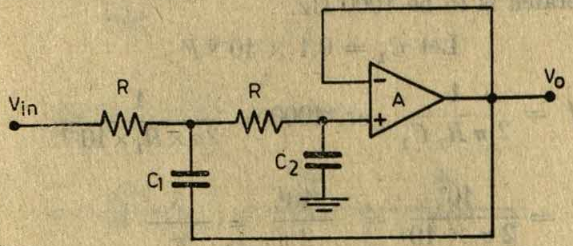
$$C_1 = \frac{1.414}{\omega_C R} \tag{8.49}$$

$$C_2 = \frac{0.707}{\omega_C\, R} \tag{8.50}$$

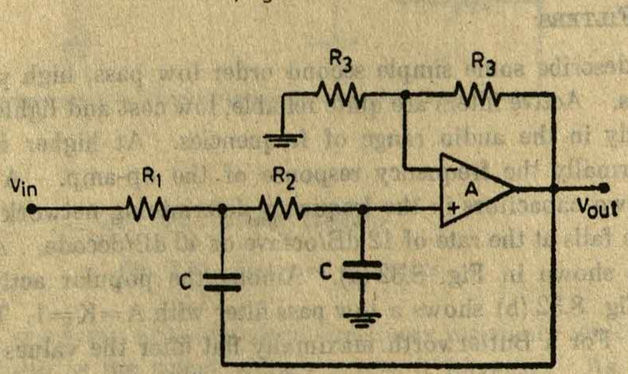
Here $\omega_C = 2\pi \times f_C$ is the cut-off frequency of the filter. Thus, if it is desired to have a cut-off frequency of 3.4 KHz, then a good choice will be to have $R = 33\text{K}\Omega$ and $C_1 = 2000\text{pF}$ and $C_2 = 1000\text{pF}$.



(a) General configuration



(b) Unity gain K = 1 filter



(c) Equal 'C' filter with K = 2

Fig. 8.32 Low pass filter

In the second configuration shown in Fig. 8.32 (c), the gain is 2 and the values of the resistances are

$$R_1 = \frac{0.707}{\omega_C\, C} \tag{8.51}$$

$$R_2 = \frac{1.414}{\omega_C\, C} \tag{8.52}$$

In a practical circuit R_3 can be 10 Kohm. For a cut-off frequency of 3.4 KHz, if we have $C = 2000$ pF, then $R_1 = 56$ Kohm and $R_2 = 112$ Kohm from eq. (8.57) and (8.52). These circuits have low sensitivities.

A second order highpass filter is shown in Fig. 8.33. Analysis shows that if the gain of the amplifier is unity and $C_1 = C_2$, then

$$R_1 = \frac{.707}{\omega_C\, C} \tag{8.53}$$

$$\text{and} \quad R_2 = \frac{1.414}{\omega_C\, C} \tag{8.54}$$

where w_C is the cut-off frequency of the filter.

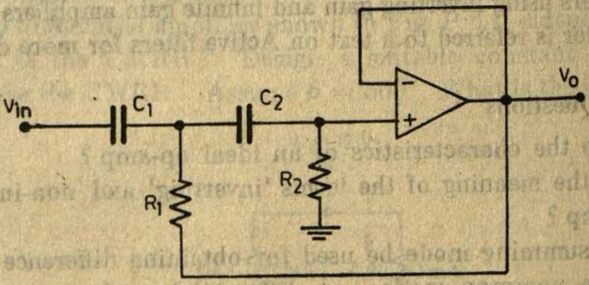


Fig. 8.33 High Pass filter

Finally a band pass filter is shown in Fig. 8.34. The gain of the amplifier is adjusted to be 2, therefore $R_4 = R_5$ Various values can be realised using combination of the resistances and capacitances. For example,

(i) $Q = 2$

and if $C_1 = C_2 = C$ then

$$R_2 = \frac{0.7403}{\omega_C\, C} \tag{8.55}$$

$$R_3 = \frac{2.3508}{\omega_C\, C} \tag{8.56}$$

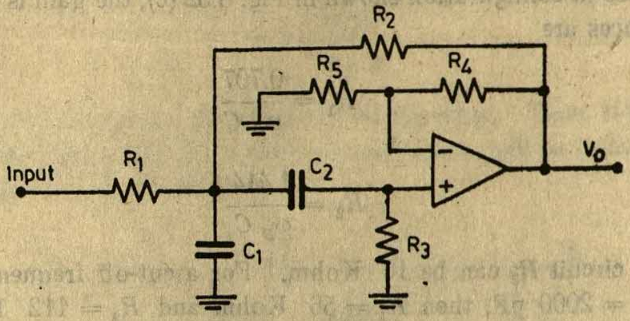


Fig. 8.34 Band Pass Filter

(ii) $Q = 5, \quad C_1 = C_2 = C,$

$$R_2 = \frac{0.6344}{\omega_C\, C} \tag{8.57}$$

$$R_3 = \frac{2.576}{\omega_C\, C} \tag{8.58}$$

where ω_C is the centre frequency of the Bandpass filter.

Active filters using inverting gain and infinite gain amplifiers are also designed used. The reader is referred to a text on Active filters for more details.

Review Questions

8.1 What are the characteristics of an ideal op-amp ?

8.2 What is the meaning of the terms 'inverting' and 'non-inverting' inputs of an op-amp ?

8.3 Can the summing mode be used for obtaining difference of two signals ?

8.4 What are common mode and differential mode gains in a differential amplifier ?

8.5 Define CMRR. How can it be increased ?

8.6 What is equivalent source resistance of a constant current source ?

8.7 What is the function of the Zener diode in the constant-current source ?

8.8 How can the input impedance of a differential amplifier be increased ?

8.9 What is a totem pole connection ? What is its advantage ?

8.10 What is the essential difference between the complementary output and totem-pole output connection ?

8.11 What is the roll-off characteristic of an actual op-amp ?

8.12 Why do you need compensation in an op-amp ?

8.13 What is lead compensation in an op-amp ?

8.14 What is 'slew rate' of an op-amp ? Distinguish between slew rate and transition time.

8.15 What will be the output of a differentiator to a square wave signal?

8.16 What are voltage followers?

8.17 What is a bridge amplifier and how does the circuit measure physical parameters like temperature, pressure etc.?

8.18 What is a "sample and hold" circuit?

8.19 How can an op-amp be used as a.c. amplifier?

8.20 Can an op-amp be used to generate square waves and sine waves?

8.21 Can a unity gain amplifier be used in a lowpass filter?

Problems

P 8.1 A signal of amplitude 1 volt and internal source resistance of 10 K Ω is to be amplified to obtain +5 and −5V. Suggest suitable circuits and calculate the values of the resistances.

P 8.2 Two signals $V_1 = 2 \sin 1000\,t$ and $V_2 = 1.5 \sin 1500t$ are to be added using a summer amplifier. The output voltage swing allowable is ±15 volts. Calculate the values of the summing network in an op-amp adder.

P 8.3 Two signals $V_1 = 5 \sin 1000t$ and $V_2 = 4 \cos 2000t$ volts are to be differenced. Suggest a suitable circuit and calculate the values of the resistances if the gain is 10. What are the frequency components present in the difference signal?

P 8.4 In the differential amplifier shown in Fig. P 8.1, calculate the A_d and A_c. What is the CMRR? Design a suitable constant current source to increase the CMRR. Assume $\beta = 500$. What is the input impedance?

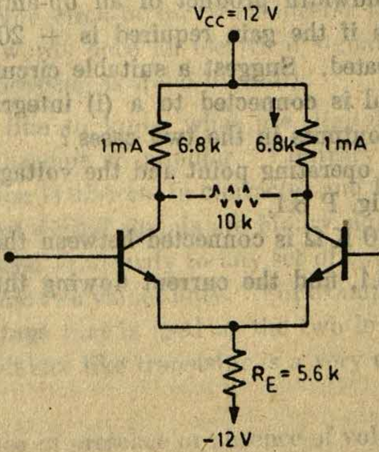


Fig. P 8.1

P 8.5 In an experimental set-up we find that at the input of the amplifier $V_1 = 0.5 \sin 314t + 0.02 \sin 2000t$ and $V_2 = 0.5 \sin 314t$. The differential gain of the amplifier is 200 and the CMRR is 60 dB. What will be the output signal. Make suitable approximations (Note : 0.5 sin 314t is the unwanted 50 Hz pick-up).

P 8.6 A differential amplifier using FET is shown in Fig. P 8.2, calculate suitable values of R_D and R_S so that $I_{D1} = I_{D2} = 0.5$ mA. It is given that $g_m = 1.2$ mA/volts. Find the A_d, A_c, CMRR and the input impedance. Derive the equations.

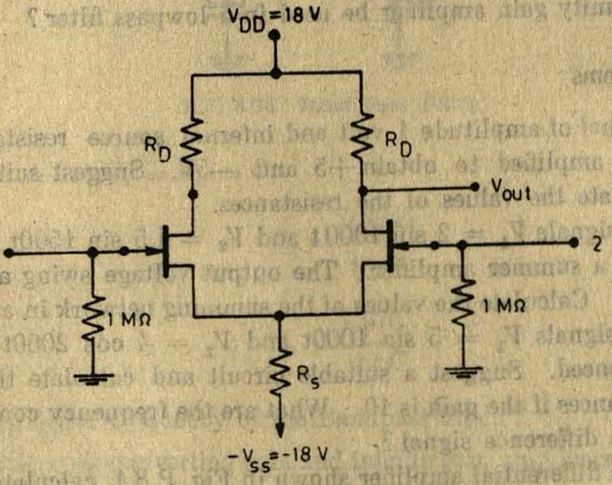


Fig. P 8.2

P 8.7 The unity gain-bandwidth product of an op-amp is 1.5 MHz. What will the bandwidth if the gain required is + 20dB ? The op-amp is internally compensated. Suggest a suitable circuit.

P 8.8 A sine wave signal is connected to a (i) integrator (ii) differentiator. What will be the outputs in the two cases ?

P 8.9 Find the quiescent operating point and the voltages at the base, emitter and collector in Fig. P 8.1.

P 8.10 If a resistance of 10 K Ω is connected between the collectors as shown dotted in Fig. P 8.1, find the current flowing through it.

9

Logic and Digital Circuits

9.0 Introduction

So far we have discussed linear circuits where the signals have a continuous range of values and the electronic circuit is basically used to amplify these signals. Quite a large amount of processing including display of these signals is carried out using linear circuits. With the advent of digital computers and later microprocessors the emphasis has shifted considerably to digital processing, including control and display. In fact the robot revolution is going to change the whole concept of the industrial activity and possibly the quality of human life. The real signals in the world are analogue and will remain so. The electronic circuits interact with them through transducers. The digital circuits, on the other hand, interface with the linear circuits (or transducers) through analogue to digital converters. In other words once an electrical signal is converted into a digital format, all further processing is done digitally.

Now we would like to know what are digital circuits and why has the digital representation become so popular. Contrary to analogue representation, the digital representation is discrete in character and has only a few discrete levels of signal. The simplest digital signals are binary signals having two levels. The two levels may be defined arbitrarily to any set of two values of voltages, but the signal is confined to these two values only. For example, it may be just a 'presence' or an 'absence' of voltage that is used as the two level signal. An 'on' and 'off' state of an electronic device like transistor is a very convenient way of setting up the binary signals.

Extending the idea of presence or absence of voltages to saying that a certain statement is 'true' or 'false' takes us directly into the realm of logic. A combination of 'true' or 'false' statements when the variable has only two possible values had been studied a long time ago by mathematicians and Boolean algebra was defined more than a century back. In fact this has provided the main frame of the development of logic circuits. Functions of two variables where each variable has two possible values and hence four possible combinations in all have been studied in detail. They have been used extensively to define complex logic statements. We shall study six of the possible sixteen combinations of logic statements. They are AND, OR, NOT, NAND, NOR and EX-OR. In fact Boolean algebra defines theorems which are used to simplify the logical statements. We shall describe here logical functions and circuits which implement these logical functions.

Once we have come to the realisation of using two state (value) functions for expressing logical ideas, the number system suitable for such a situation will be the binary number system. We have included here a very brief review of the binary number system. All the arithmetic operations can be performed in this representation and thus logic circuits in certain combinations will perform the arithmetic operations. Finally in the chapter we have described circuits which implement the logic circuits. Out of a multitude of techniques and systems we have only chosen the TTL (Transistor-Transistor-Logic) and the CMOS (Complementary Metal- oxide-Semiconductor FET) circuits for description here. Both these techniques have resulted in large scale integration of circuits on a small silicon chip and made the computer revolution possible.

9.1 Functions of Binary Variables

We have seen that binary representation or a two state description of logical statements is capable of being implemented easily by electronic circuits resulting in computing, processing and display of information bearing signals. The binary variable has only two states, and a combination of two binary variables gives rise to four possiblities. We shall discuss here only the combinational functions where the output state is decided by a combination of the two input states. Out of the sixteen possible combinations of input and output states we shall only study six functions.

Although a large number of symbols have been used to represent the status of the binary variable, like 'true' and 'false', 'on 'and 'off', 'positive' and 'negative', 'high' and 'low' etc. the symbol '1' and '0' has become quite popular. Thus if a logical statement *X* is 'true' we say that *X* has a value equal to '1'. Similarly if the statement is 'false', the variable *X* is equal to '0'. There is no numerical significance to '1' and '0' but there is only a logical significance attached to it. Each of the combinations of the input variables will give an output depending on the function used. The statement of the input and output is presented in a tabular form and is called the truth table. We shall illustrate these ideas with specific examples of the functions involved.

9.1.1 AND FUNCTION

Let us consider first a statement which is made up of two simple logical statements. "Ram is twenty years old AND Ram can vote". The binary variable *A* is assigned to the statement 'Ram is twenty years old'. The variable

B is assigned to the statement 'Ram can vote'. These two statements are joined together by '*AND*'. Thus *A* may be 'true' or 'false' and similarly *B* may be 'true' or 'false'. We are interested in a situation when '*A* AND *B*' is 'true'. The possibilities are listed below in a tabular form in Table 9.1.

Table 9.1

A	*B*	*A AND B = C*
True	True	True
True	False	False
False	True	False
False	False	False

We shall designate the output or the outcome of the combination function '*A AND B*' as *C*. We see that *C* is true only if *A* is true AND *B* is 'true'. The original statement therefore reads

$$C = A \text{ } AND \text{ } B \tag{9.1.1}$$

Symbolically the *AND* function has been represented by symbols like '.', '*X*', '∩' etc. We shall use the dot symbol for the *AND* functions. Thus eq. 9.1.1 will be written as

$$C = A.B = AB \tag{9.1.2}$$

We should remember that eq. 9.1.2 is only a symbolic language and no multiplication is intended. As we mentioned earlier, it is convenient to write 1 and 0 instead of true and false. Thus, the truth table for AND function is written down as in Table 9.2.

Table 9.2 Truth Table for AND Function

A	B	C = A.B
1	1	1
1	0	0
0	1	0
0	0	0

We have been emphasising so far only the logical significance of these statements but we should not lose sight of the fact that electronic circuits have implemented circuits which follow these functions. These circuits are called logic circuits. The AND function is implemented by an AND circuit or AND gate. The symbol used to represent this logical AND gate is shown in Fig. 9.1.

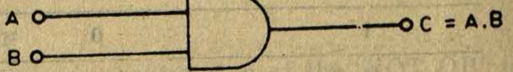


Fig. 9.1 AND Gate

It is not necessary that there be only two inputs to the gate in Fig. 9.1. There can be 3 or 4 or *n* number of inputs with one output subject to the condition that the output is 1 when every one of the input is 1. In other words, all the inputs must be simultaneously 'true' if the output is 'true'. AND gate is also known as the 'coincidence' gate.

9.1.2 OR FUNCTION

Consider the statement that 'Ram is twenty years old OR' 'Ram can vote'. In terms of variables A and B, we find that the statement is 'true' if *A* OR *B* is 'true'. The truth table for the *OR* function is given in Table 9.3.

Table 9.3 Truth Table for OR function

A	B	$C = A + B$
1	1	1
1	0	1
0	1	1
0	0	0

Symbolically the OR function has been represented by symbols like '+' 'U' etc. We shall use '+' symbol for representing OR function. Thus

$$C = A + B \tag{9.1.3}$$

Here also no addition is intended by eq. 9.1.3. The symbol for the 'OR' gate is shown in Fig. 9.2.

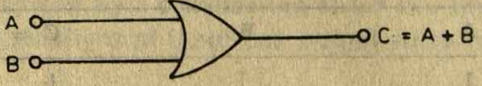


Fig. 9.2 OR Gate

The output of OR equals 0 only when all the inputs to the gate are 0.

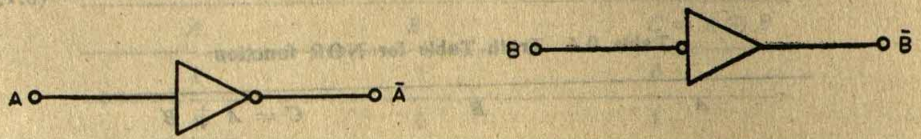
9.1.3 NOT FUNCTION

Let us take the statement "Ram is NOT twenty years old". This statement is 'true' only if the statement, symbolised by A, 'Ram is twenty years old' is 'false'. That is if *A* is '1' then NOT *A* is '0'. If *A* is '0' then 'NOT *A*' is '1'. The truth table for the NOT function is shown in Table 9.4.

Table 9.4 Truth Table for NOT A

A	$\bar{A} = NOT\ A$
1	0
0	1

Symbolically the NOT function is represented by putting a bar over the variable. Thus NOT A = $\bar{A}$. In circuits the NOT function is indicated by two symbols shown in Fig. 9.3. The symbol in Fig. 9.3 (a) is self explanatory. By placing a small circle at the end of the line as at the input of the variable *B* as shown in Fig 9.3 (b), we indicate the inversion or the NOT operation.



(a) Not

(b) Inversion

Fig. 9.3 NOT Gate

9.1.4 NAND FUNCTION

The NAND function is a contraction of the function 'NOT AND', i.e., NOT $(A.B)$. The function equals O when all the input variables equal 1. In other words if any of the input is O, the output is 1. The truth table for the NAND function is given in Table 9.5. The symbol used for NAND operation is '↑'. Thus.

$$C = A \text{ NAND } B$$

$$\text{or} \quad C = A \uparrow B \qquad (9.1.4)$$

The symbol for the NAND gate is shown in Fig. 9.4. The small circle at the output represents the NOT operation.

Table 9.5 Truth Table for NAND function

		$C = A \uparrow B$ or $C = \overline{A, B}$
1	1	0
1	0	1
0	1	1
0	0	1

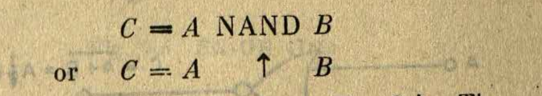


Fig. 9.4 NAND Gate

9.1.5 NOR FUNCTION

The NOR function is a contraction of the 'NOT OR' function i.e. NOT $(A + B)$. The function equals 1 when all the inputs are 0, or if any of the inputs is 1 the output is 0. The truth table for the NOR function is given in table 9.6. The symbol for the NOR operation is ' ↓ '. Thus

$$C = A \text{ NOR } B = (\overline{A + B})$$

$$\text{or} \quad C = A \downarrow B \tag{9.1.5}$$

Table 9.6 Truth Table for NOR function

A	B	$C = A \downarrow B$ or $C = (\overline{A + B})$
1	1	0
1	0	0
0	1	0
0	0	1

The symbol for the NOR gate is shown in Fig. 9.5. The small circle at the output indicates the NOT operation.

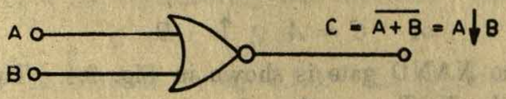


Fig. 9.5 NOR Gate

Although there appears to be nothing new in the NAND and NOR gates but these gates are commercially available in MSI and LSI circuits in large numbers and cheaply. In the beginning when ICs started competing commercially in the market, it was seen that the NAND gates were most easily realised in TTL circuits. Since the NAND gate could be used to synthesise all other logic circuits, it has become quite economical to use only NAND gates. Similarly in some other logic circuits like the ECL (Emitter Coupled Logic) it was easier to realise a NOR gate. Since many gates can be packed into a small chip the concept of using NAND or NOR only for all realisations has been quite popular. With the large availability of AND, OR gates etc now, the use of NAND or NOR gates exclusively may not be very economical.

9.1.6 Ex-NOR Function

The exclusive-OR function is different from the OR function described in the earlier section in the sense that the usual OR function is redefined as Inclusive-OR. The function is 1 whenever the two input variables are dissimilar. In other words the output assumes 1 state if one and only one input state becomes 1.

The truth table for Exclusive-OR is given in Table 9.7. The symbol for the EX-OR operation is '⊕',. Thus

$$C = A \oplus B \tag{9.1.6}$$

Table 9.7 Truth table for EX-OR function

A	B	$C = A \oplus B$
1	1	0
1	0	1
0	1	1
0	0	0

The symbol for the EX-OR gate is shown in Fig. 9.6. The EX-OR function is also known as an 'anticoincidence' function, that is the output is 1 when the two inputs do not coincide.

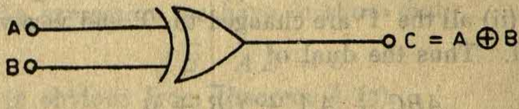


Fig. 9.6 EX-OR Gate

9.2 Boolean Theorems

We have studied some of the logical functions of two variables like AND, OR and EX-OR functions. The variables assume only two states conveniently defined as '1' and '0'. The Boolean Algebra tells us that for binary variables the following holds

$$\begin{array}{cc} \text{OR} & \text{AND} \\ \hline 1 + 1 = 1 & 1.1 = 1 \\ 1 + 0 = 1 & 1.0 = 0 \\ 0 + 1 = 1 & 0.1 = 0 \\ 0 + 0 = 0 & 0.0 = 0 \\ \hline \end{array} \tag{9.2.1}$$

$$\text{and} \quad \bar{1} = 0 ; \quad \bar{0} = 1 \tag{9.2.2}$$

Boolean algebra like other algebras consists of a set of symbols and a set of rules to manipulate these symbols. Thus this algebra has only two symbols '0' and '1' and eq. 9.2.1 and 9.2.2 define some of the rules of manipulating these symbols. There are some more postulates and theorems in Boolean algebra. We may wonder at the usefulness of such odd kind of arithmetic but we find the Boolean algebra is employed to manipulate a given logic function in such a way that the final expression can be easily implemented in hardware. Thus logical circuits can realise any complicated logical expression. This is the cornerstone of the great computer revolution.

Before taking up the theorems of the Boolean algebra we would like to reemphasise that the *AND*, *OR* and the *NOT* functions are the basic building blocks of what follows. We shall define some commonly used terms like equivalence, complement and dual.

Two logical expressions are 'equivalent' if one expression equals '1' when the other expression equals '1' and it equals '0' when the other equals '0'. The expressions are 'complements' of each other when one expression equals '1' only when the other equals '0' and vice versa. Complement of an expression is obtained if (i) all the '+' signs are changed to '.' and vice versa, (ii) all the '1's are changed to '0' and vice versa and (iii) all the variables are inverted or complemented. Thus, for example, the complement of

$$ABC + A.1 + C\bar{B} + 0$$

$$\text{is } (\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} + 0) \cdot (\bar{C} + B) \cdot 1 \tag{9.2.3}$$

Dual of an expression is obtained if (i) all the '+' signs are changed to '.' and vice versa and (ii) all the '1' are changed to '0' and vice versa. The variables are left undisturbed. Thus the dual of

$$ABC + A.1 + C\bar{B} + 0$$

$$\text{is } (A + B + C) \cdot (A + 0) \cdot (C + \bar{B}) \cdot 1 \tag{9.2.4}$$

The OR and AND expressions in eq. 9.2.1 are duals of each other.

The theorems of Boolean algebra are derived from the postulates given in eq. (9.2.1) and (9.2.2). We shall have A and B to be the logical variables assuming states of '1' and '0'. Since we are using the signs of addition and multiplication for OR and AND functions, we shall equivalently call these operations as addition and multiplication without really assigning the significance of the arithmetic operations. Thus we can conveniently say that $1 + 1 = 1$ (one plus one equals one). Proof of the theorems is not explicitly given but any theorem can easily be proved by substituting all possible values of the variable in the expression and seeing that the conditions are satisfied. This is particularly easy for Boolean algebra since the variable has only two possible values. Thus the following identities can be written down

1. (a) $0.A = 0$ 1. (b) $1 + A = 1$ (9.2.5)
2. (a) $1.A = A$ 2. (b) $0 + A = A$ (9.2.6)
3. (a) $A.A. = A$ 3. (b) $A + A = A$ (9.2.7)
4. (a) $A.\bar{A}. = 0$ 4. (b) $A + \bar{A} = 1$ (9.2.8)

Taking eq. (9.2.5) we see that both the theorems 1(a) and 1 (b) are true if we give A the two values of 0 and 1. The theorem states that "anything multiplied by 0 equals 0 and 1 plus anything equals 1". In fact the theorems 1 (a) and

1 (b) are duals of each other. It can be shown that whatever theorem is true its dual is also true. Thus, we need prove only one of them.

Similarly the theorem 2 states that "multiplication by 1 or addition of 0 does not change the expression". The theorem 3 states "multiplication by itself and addition to itself does not change the expression". The theorem 4 says that "multiplication of an expression by its complement makes it equal to zero and addition of an expression to its complement equals 1" We shall solve some examples to demonstrate the usefulness of these theorems in simplifying expressions.

Example 9.2.1

Simplify and show that

(a) $A.A.B = AB$ (theorem 3 (a)).

(b) $A.\bar{A}.B = 0$ (theorem 4 (a))

(c) $A + \bar{B} + A\bar{B} = 1$

Taking dual of the expression we have to show that

$$A\bar{B} \cdot \bar{A}B = 0$$

This is obvious from theorem 4 (a).

(d) $(A + B)\ (B + C)\ (C + A) = AB + BC + CA$

Solving $(AB + AC + BB + BC)\ (C + A)$

$= ABC + AAB + ACC + AAC + BC + BA + BC + BCA$

$= ABC + ABC + AB + AB + AC + AC + BC + BC$

$= AB + BC + AC(B + 1) = AB + BC + AC.$

We have in solving the last expression above used ordinary laws of algebra like the associative, the commutative and distributive laws. These laws hold in Boolean algebra also and are simply stated as

Associative laws

5 (a) $(AB)\ C = A\ (BC)$ (9.2.9)

5 (b) $(A + B) + C = A + (B + C)$ (9.2.10)

Commutative Laws

6 (a) $AB = BA$ (9.2.11)

6 (b) $A + B = B + A$ (9.2.12)

Distributive Laws

7 (a) $A\ (B + C) = A\ B + AC$ (9.2.13)

and its dual

7 (b) $A + BC = (A + B)\ \ (A + C)$ (9.2.14)

Another important theorem known as De Morgan's theorem is stated as

8 (a) $\overline{A.B.C} = \bar{A} + \bar{B} + \bar{C}$ (9.2.15)

8 (b) $\overline{A + B + C + \ldots\ldots\ldots} = \bar{A}\ .\ \bar{B}\ .\ \bar{C}\ .$ (9.2.16)

There are some additional theorems along with their duals which help us in the simplification of Boolean expressions.

9 (a) $AB + A\bar{B} = A$ 9 (b) $(A + B)\ (A + \bar{B}) = A$ (9.2.17)
10 (a) $A + AB = A$ 10 (b) $A\ (A + B) = A$ (9.2.18)
11 (a) $A + \bar{A}B = A + B$ 11 (b) $A\ (\bar{A} + B) = AB$ (9.2.19)
12 (a) $AB + \bar{A}C + BC = AB + \bar{A}C$ (9.2.20)
12 (b) $(A + B)\ (\bar{A} + C)\ (B + C) = (A + B)\ (\bar{A} + C)$
13 (a) $AB + \bar{A}C = (A + C)\ (\bar{A} + B)$ (9.2.21)
13 (b) $(A + B)\ (\bar{A} + C) = AC + \bar{A}B$

We shall illustrate the application of these theorems in some examples here.

Example 9.2.2

(a) $\bar{A}\ B\ \bar{C} + B\ \bar{C}\ \bar{D} + AD$

Applying theorem 13(a) in reverse

$\bar{A}\ B\ \bar{C} + (B\bar{C}\bar{D} + AD) = \bar{A}B\bar{C} + AD + \bar{D}B\bar{C} + AB\bar{C}$

$= AD + B\bar{C}\ (A + \bar{A}) + \bar{D}B\bar{C}$ Using theorem 4(b) and 1 (b) in succession

$= AD + B\bar{C}\ (1 + \bar{D})$

$= AD + B\bar{C}$

(b) simplify $(\bar{A} + B + \bar{C})\ (C + D)\ (\bar{A} + B + \bar{D} + E)$

Let $\bar{A} + B = X$

Then $F = (\bar{A} + B + \bar{C})\ (C + D)\ (\bar{A} + B + \bar{D} + E)$

$= (X + \bar{C})\ (C + D)\ (X + \bar{D} + E)$

Now $(X + \bar{C})\ (X + \bar{D} + E) = X + \bar{C}\ (\bar{D} + E)$

$F = [X + \bar{C}\ (\bar{D} + E)\ ]\ (C + D) = XC + XD + D\bar{C}\ (\bar{D} + E)$

$= X\ (C + D) + \bar{C}DE$

$= (\bar{A} + B)\ (C + D) + CDE$

$= (\bar{A} + B)\ (C + D) + (C + D)\ \bar{C}E = (C + D)\ (A + B + CE)$

Example 9.2.3

Living in Kharagpur you have to catch a plane at Calcutta. To do this you must board the 4 : 30 train to Calcutta, which you can if you obtain a cycle rickshaw for the station and the railway crossing is open, or if you can get a bus in which case you can reach in time even if the railway gate is closed. If the train is on schedule at Calcutta you can reach your flight by boarding a bus, otherwise you have to hire a taxi. You can not afford a taxi at Calcutta, if you hired a cycle rickshaw at Kharagpur. In what situations do you get your plane ?

To solve this problem we introduce and define the variables :

(i) A : You hire a cycle rickshaw at Kharagpur
(ii) B : You board a bus at Kharagpur
(iii) C : You catch the train

(iv) D : The train reaches Calcutta in time
(v) E : You take a bus at Calcutta
(vi) F : You hire a taxi at Calcutta
(vii) G : The level crossing at Kharagpur was open.
(viii) X : You reach the Airport in time

We thus see that

$$
\begin{aligned}
C &= AG + B \\
X &= C\,(DE + \bar{D}F) \\
AF &= 0 \\
X &= (AG + B)\,(DE + \bar{D}F) \\
&= AGDE + B(DE + \bar{D}F)
\end{aligned}
$$

Thus you get to the airport in time if you board a bus $B=1$, $A=0$) at Kharagpur or if you hire a cycle rickshaw ($A=1$, $B=0$) but then the level crossing must be open and the train reach Calcutta in time.

9.3 Binary Numbers

We are accustomed in everyday life with numbers in the decimal system. In the binary systems, since there are two values assigned to any variable, it is convenient to work with a binary number system. In fact there is nothing natural about the decimal system other than that this system has been universally adopted. A number system with any other radix could have been used. Let us examine the decimal system in some detail. We find that we have ten symbols 0, 1, 2, 3, ... 9 to represent all quantities upto 9 and for a longer number we shift the position of the digit. Thus we have positional information in terms of units, tens, hundreds and so on. A simple number like 4375.28 in the decimal system is therefore

$$
\begin{aligned}
&4 \times 10^3 + 3 \times 10^2 + 7 \times 10^1 + 5 \times 10^0 + 2 \times 10^{-1} + 8 \times 10^{-2} \\
&= 4000 + 300 + 70 + 5 + 0.2 + .08 \\
&= 4375.28
\end{aligned}
$$

A number in the octal system (base of 8) is similarly written as 345.24 (octal)

$$
\begin{aligned}
&= 3 \times 8^2 + 4 \times 8^1 + 5 \times 8^0 + 2 \times 8^{-1} + 4 \times 8^{-2} \\
&= 229\frac{20}{64} \text{ (decimal)} \\
&= 229.3125 \text{ (decimal)}
\end{aligned}
$$

All the symbols in the octal system will be less than 8. Thus in the binary system with two symbols 0 and 1, a binary number 1100.11 will be

$$
\begin{aligned}
&1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} \\
&= 8 + 4 + 0 + 0 + \frac{3}{4} \text{ (decimal)} \\
&12.75 \text{ (decimal)}
\end{aligned}
$$

We have in the previous section used '1' to represent a true statement and '0' to represent a false statement. They were logical variables and not numbers. The numbers used here 1 and 0 are arithmetic numbers. However, if we identify the logical '1' with the arithmetic 1 and the logical '0' with the arithmetic 0, then we can use the same logical circuits to solve both the logical and arithmetic problems.

9.3.1 CONVERSION FROM DECIMAL TO BINARY SYSTEM

A convenient method of converting from a decimal to a binary number (number in any other base) is as follows. The decimal number is divided in two parts. The number to the left of the decimal point is handled seperately from the number on the right side of the decimal point.The number to the left of the decimal point is divided by 2 (the base to which the conversion is desired) and the "remainders" are noted for each division. The division proceeds till we reach the quotient 0. The remainders form the number in the new base 2 except that the remainders are read out from the last remainder to the first.

The right hand side of the number—right of the decimal point—is repeatedly multiplied by 2 (new base desired) and the 'Carriers' are recorded for each multiplication. The process continues till we reach 0 as the product. The 'carrier' read out from the first carry to the last represents the binary number (number in the new base) to the right hand side of the decimal point. The process of multiplication may be stopped earlier if we reach the number of digits required to the right of the decimal point before the termination. Let us illustrate the process with an example.

Example 9.3.1

Convert the decimal number 372.875 into a binary number

Left part		Remainders	
2	372	0	
2	186	0	
2	93	1	
2	46	0	
2	23	1	↑
2	11	1	
2	5	1	
2	2	0	
2	1	1	
	0		

Right Part

$$\begin{array}{c|c r} & \text{Carry} & .875 \\ & & \times 2 \\ \cline{3-3} & 1 & .750 \\ & & \times 2 \\ \cline{3-3} & 1 & .500 \\ \downarrow & & \times 2 \\ \cline{3-3} & 1 & .000 \end{array}$$

Hence the binary equivalent of 372.875 is

$$1\,0\,1\,1\,1\,0\,1\,0\,0\,.\,1\,1\,1$$

W can convert it back to decimal to obtain

$$1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 +$$
$$1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$
$$= 372.875$$

In practice, in many situations which are more common than otherwise the binary number to the right of the decimal point does not terminate though the decimal number has a finite number of terms. Arbitrary termination of the binary number after a certain number of digits may have to be used.

9.3.2 BINARY ARITHMETIC

Addition, subtraction, multiplication and division of binary numbers follow the usual arithmetic rules. Actually multiplication can be looked upon as repeated addition (which it actually is) and division can be thought of as a repeated subtraction. Subtraction also is nothing but addition using 1's complement where the carry is disregarded. Thus, a basic adding circuit can perform all the arithmetic operations. We shall show how a logical circuit can perform the addition operation. Let us look into the process of addition by taking two numbers 101 (5) and 100 (4).

$$\begin{array}{r|c c c} \text{Carry} & 1\,0\,1 & = & A \\ & 1\,0\,0 & = & B \\ \hline 1 & 0\,0\,1 & = & C \end{array}$$

There are four possible combinations when we add two binary numbers. We observe that 1 plus 0 and 0 plus 1 both give 1 as output. 0 plus 0 is 0 but 1 plus 1 gives 0 as the output with a carry of 1. If we are to assume for a moment that logical '1'/'0' and arithmetic 1/0 are identical, then the addition process is nothing but an *EX-OR* operation. The truth table of *EX-OR* in Table 9.7 shows that the sum part of the operation is identical. The carry, however, is not generated by this operation. But 'carry' is only required when the bits of *A* and *B* both are 1 (coincident). An *AND* circuit will, therefore, detect the carry. An adding circuit consisting of an *EX-OR* and an *AND* circuit will give both sum and carry information. Such a circuit is called a Half Adder and is shown in Fig. 9.7

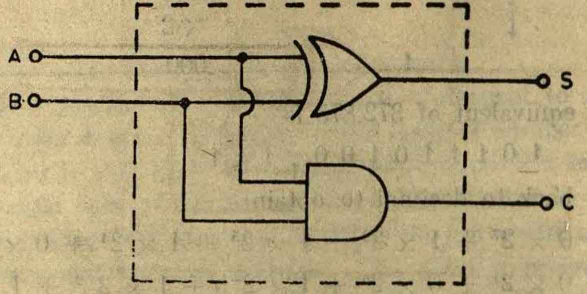


Fig. 9.7 Half Adder

The truth table for an half adder is given in Table 9.8.

Table 9.8 Truth Table for Half Adder

A	B	SUM	CARRY
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

In an actual addition operation we have to add two bits of A and B and also any carry coming from the previous bits. For example in the addition shown below, when the first bits of A and B are added we get a carry of 1. Now when

1 carry bit

$$\begin{array}{rcl} 101 & = & A \\ +\ 001 & = & B \\ \hline 110 & & \end{array}$$

we want to add the second bits of *A* and *B* we have actually three inputs. They are the bits of *A* and *B* and the carry bit. A half adder has only two inputs and, therefore, cannot perform this operation. For adding three bits together we have a Full adder.

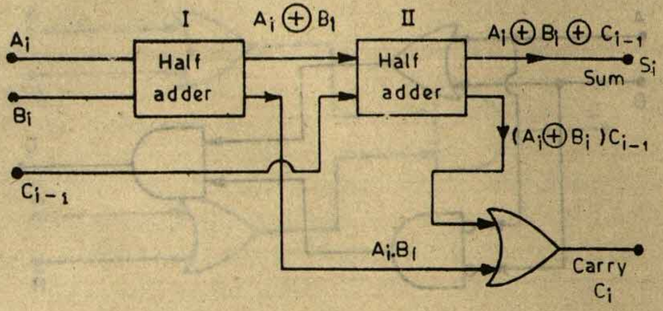


Fig. 9.8 Full Adder

A full adder consists of two half adders and an OR circuit as shown in Fig. 9.8 The sum output S_i represents the sum part $A_i \oplus B_i \oplus C_{i-1}$ of the operation. The carry is obtained from $(A_i\, B_i)$ OR $(A_i \oplus B_i)\, C_{i-1}$. C_{i-1} is the carry from the previous bit as explained. The truth table for the Full Adder is shown in Table 9.9. Actual adders will be discussed in the next chapter.

Table 9.9 Truth Table for Full Adder

C_{i-1}	A_i	B_i	S_i SUM $(A_i \oplus B_i \oplus C_{i-1})$	C_i CARRY $(A_i\, B_i) + (A_i \oplus B_i)\, C_{i-1}$
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0

The block logic circuits shown in Figs. 9.8 and 9.7 are only conceptual blocks. The actual circuits may be different since the *EX-OR* can be realised in many different ways. For example the logic expression for *EX-OR* is written as

$$C = A \oplus B = (A + B)\,(\overline{AB}) \tag{9.3.1}$$

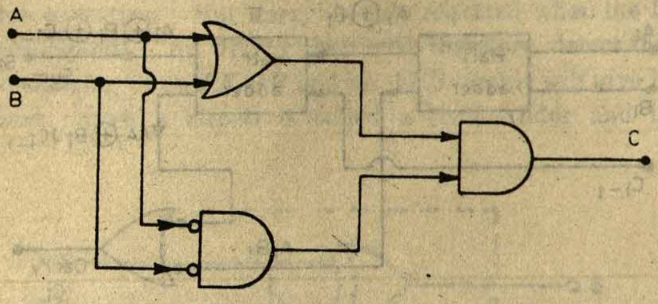
The above expression in different ways looks like the following

$$C = A\overline{B} + B\overline{A} \tag{9.3.2}$$

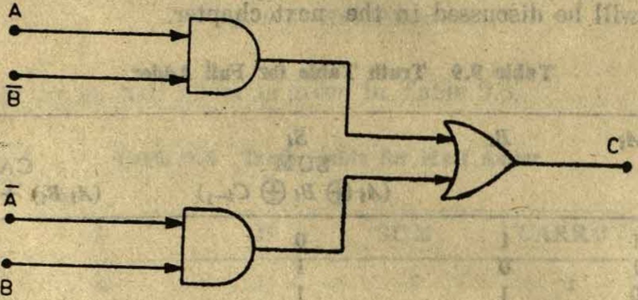
or
$$C = \overline{AB + \overline{A}\,\overline{B}} \tag{9.3.3}$$

or
$$C = (A + B)\,(\overline{A} + \overline{B}) \tag{9.3.4}$$

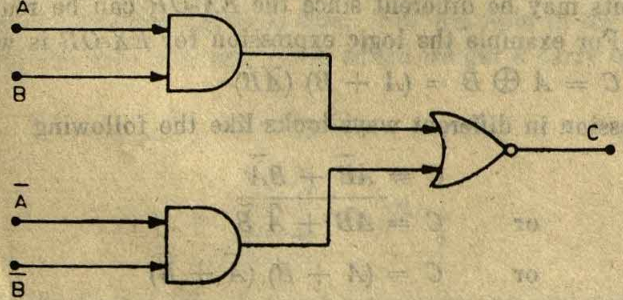
Each of the above equations can be used to realise an *EX-OR* function. Some of the realisations are shown in Fig. 9.9. A realisation of *EX-OR* using NAND gates alone is shown in Fig. 9.9 (e).



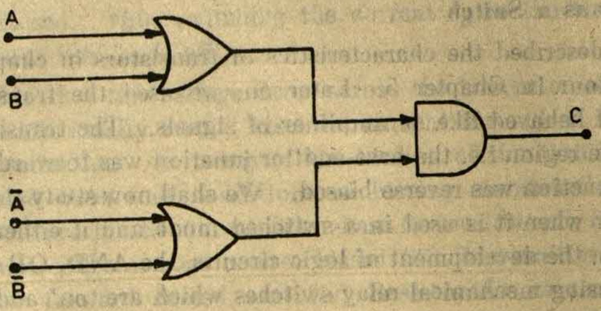
(a) $(A+B).(\overline{AB})$



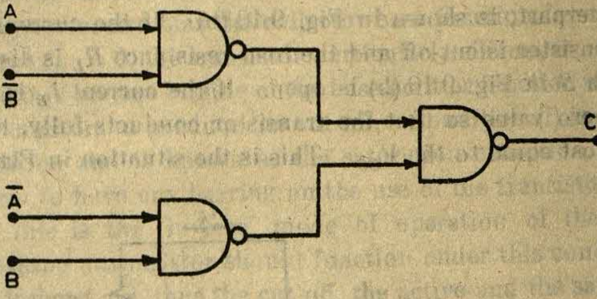
(b) $A.\overline{B} + \overline{A}.B$



(c) $\overline{AB + \overline{A}.\overline{B}}$



(d) $(A + B)(\bar{A} + \bar{B})$



(e) $\overline{\overline{A\bar{B}}\;\overline{\bar{A}B}}$

Fig. 9.9 Ex OR realisations

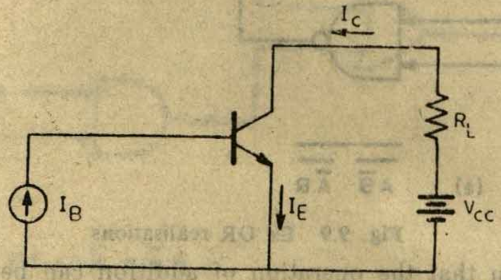
Thus it is seen that the operation of addition can be performed using a combination of AND, OR and NOT logic gate circuits. All other arithmetic operations can, therefore, be performed in hardware using binary numbers and logic circuits.

The question that now arises is how do we make a logic gate in hardware. Starting with switches in series and parallel logic gate circuits have been built using Diode-Transistor Logic (DTL), Resistance-Transistor Logic (RTL), Transistor-Transistor Logic (TTL), Direct-coupled-Transistor Logic (DCTL) Integrated Injection Logic (IIL), Emitter-Coupled-Logic (ECL) and MOS gates among many others. We have selected TTL gates and MOS gates for illustration here. TTL gates are being used extensively in MSI and LSI circuits and are available commercially at very low prices. MOS gates particularly the CMOS gates, on the other hand, form an entirely different approach to the design of logic circuits and are capable of very large scale integration. They deserve a more detailed description. The heart of the TTL and other similar gates is the transistor switch which we shall take up next for study.

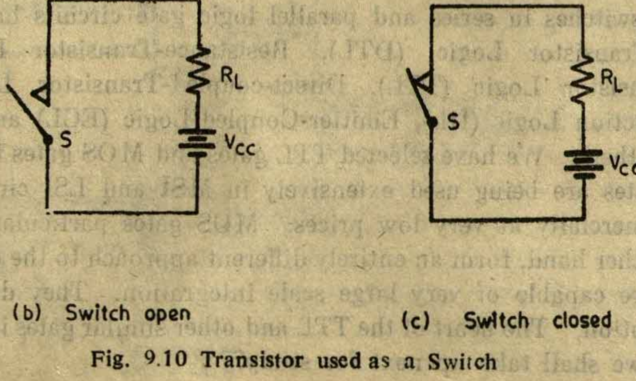
9.4 Transistor as a Switch

We have described the characteristics of transistors in chapter 3 and their terminal behaviour in Chapter 5. Later on, we used the transistors in linear circuits where it behaved like an amplifier of signals. The transistor was all the time in its active region i.e. the base-emitter junction was forward biased and the collector-base junction was reverse biased. We shall now study the characteristics of the transistor when it is used in a switched mode and it either conducts fully or is cut off. In the development of logic circuits, the AND, OR and NOT gates could be built using mechanical relay switches which are 'on' and 'off'. Though such relay circuits are still used, their speed of operation is very low. Transistors used as switches can be made to operate at very high speeds and large number of transistors can be fabricated on small silicon chips.

A circuit arrangement of a transistor switch is shown in Fig. 9.10 (a). Its conceptual counterpart, is shown in Fig. 9.10 (b). If the current I_B is small or zero then the transistor is cut-off and the load resistance R_L is disconnected from V_{CC}. The switch S in Fig. 9.10 (b) is open. If the current I_B is now suddenlly increased from zero value so that the transistor conducts fully, the voltage drop across R_L is almost equal to the V_{CC}. This is the situation in Fig. 9.10 (c) when



(a) Transistor switch



(b) Switch open (c) Switch closed

Fig. 9.10 Transistor used as a Switch

the switch S is closed. Thus switching the current I_B in the transistor circuit makes the transistor 'on' and 'off'.

It is desirable that the voltage drop across the transistor when it is fully conducting be small- ideally zero. Also the current through it be ideally zero when it is not conducting. In terms of the biasing of the transistor with two junctions we would have four conditions of biasing combinations. They are (i) Base-emitter forward biased and collector-base forward biased, (ii) Base-emitter forward biased and collector-base reverse biased (iii) Base-emitter reverse biased and collector-base forward biased and (iv) Base-emitter reverse biased and collector-base reverse biased.

We are familiar with the condition (ii) which is the normal condition of biasing and we say that the transistor is in the 'active region'. Condition (iv) is obviously the 'cut off condition when the transistor does not conduct. Actually it is not necessary to reverse bias the collector-base junction for producing a cut-off. If the current $I_B = 0$, the transistor particularly silicon, is very close to cut-off. Small amount of reverse biasing of the base-emitter junction may be necessary in germanium transistors to produce the cut off. Condition (i) is also a transistor conducting condition and is known as the saturation condition. The condition (iii) does not seem to have any bearing on the use of the transistor in the normal mode. In fact this is the 'inverse' mode of operation of the transistor and theoretically speaking a transistor should function under this conditon also. The three regions of interest are, thus the cut-off, the active and the saturation regions. In the switching mode we do not operate the transistor in the active region. The transistor from the cut off passes into the saturation region via the active region. We shall now describe in detail the cut-off, the saturation and the inverse mode of the transistor.

9.4.1 Transistor at Cut-Off

The cut-off in a transistor is defined by the condition that $I_B = 0$. In actual practice there is always a small reverse saturation current flowing through a reverse biased junction and thus I_C cannot be ideally zero when $I_B = 0$. In an attempt to cut off the transistor in Fig. 9.10 (a), we could first reduce $I_B = 0$ and then, if necessary, reverse bias the base-emitter junction. Let us examine the situation when $I_B = 0$. The voltage V_{BB} is not enough to drive the current I_B as shown in Fig. 9.11. Referring to the eq. (3.2.6) we find that if $I_B = 0$, we have

$$I_C = \beta I_B + I_{CO}\left(\frac{1}{1-\alpha}\right) \tag{3.2.6}$$

or

$$I_C = I_{CO}\left(\frac{1}{1-\alpha}\right) \tag{9.4.1}$$

Such a situation will arise when the voltage V_{BB} is smaller than V_{BE}, the cut-in voltage of the transistor. The value of α may not become zero near cut off

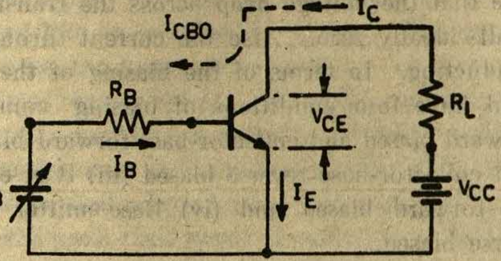


Fig. 9.11 Biasing of transistor Switch

conditions as in the germanium transistor and $I_{CO}/(1-\alpha)$ in eq. 9.4.1 may be quite large. In silicon transistors, however, the value of α approaches zero near cut off and then $I_C = I_{CO}$ when $I_B = 0$. Thus, in silicon transistors zero base current produces a cut off condition. To produce a cut-off in germanium transistors the base-emitter junction has to be reverse biased somewhat and a value of about $0.1V$ is sufficient.

The collector current under cut off conditions ($I_E = 0$) is known as I_{CBO}. This current is larger than I_{CO} because of the additional effect of surface leakage current and avalance multiplication effects in reverse bias junction. The I_{CBO} is temperature dependent and doubles for every 10°C rise in temperature of the junction. This current is of the order of 0.01 μA in silicon transistors and about 1 μA in germanium transistors. This current is dependent on the size and power dissipation capabilities of the transistor and varies over a very wide range of values. To sum up we can say that a silicon transistor is cut off as long as the base-emitter voltage is lower than the cut in voltage of about 0.65 V. For germanium transistors the base-emitter junction has to be reverse biased to reduce the collector current to I_{CO} levels.

9.4.2 TRANSISTOR IN SATURATION

If the voltage V_{BB} in Fig. 9.11 is increased to values above the cut-in level the transistor conducts. As the I_B is increased further the current I_C goes on increasing. We had defined the small signal parameter $\Delta I_C/\Delta I_B$ as β or h_{fe} of the transistor. In switching mode we define another parameter I_C/I_B as the d.c. beta or h_{FE}. This is also known as the d.c. forward transfer ratio or large signal current gain of the transistor. In general, in the active region, the small signal h_{fe} and large signal h_{FE} are almost equal. Coming back to the circuit of Fig. 9.11 as we increase I_B we obtain $h_{FE}\, I_B = I_C$ as the current in the collector circuit. The voltage V_{CE} given by

$$V_{CE} = V_{CC} - I_C R_L \tag{9.4.2}$$

goes on falling as I_C increases. The base-emitter junction is forward biased and the collector-base junction is reverse biased and the transistor is in the active region. As V_{CE} becomes smaller we find that the collector-base junction voltage becomes zero and finally as we continue increasing I_B, the junction becomes forward biased. At this point the base is at a higher positive potential than the collector. This is called "Saturation" of the transistor. Some important observations at this point are as follows :

(i) The voltage V_{CE} is smaller than V_{BE} since the collector-base junction is forward biased. It is of the order of 0.3V for silicon transistors and about 0.1V for germanium transistors. The voltage V_{BE} at saturation is about 0.75 volts for silicon and 0.3V for germanium transistors.

(ii) As the base current is increased further the collector current does not increase any further. In fact we find that

$$I_C < h_{FE} I_B$$

(iii) The minority carriers injected into the base by the forward biased base-emitter junction are in excess of the carriers collected by the now forward biased collector-base junction. We have, therefore, the phenomena of stored charge in the base. If we desire to switch the transistor from saturation to active and then to cut-off regions again we have to allow time for the dispersal of these stored charges in the base. The stored charge in the base region actually sets the limit on the speed of operation of transistors in the switching mode.

Manufacturers normally specify the values of V_{CE} (Saturation), V_{BE} (Saturation), and h_{FE} for various currents and temperature values. These values do not differ widely from one unit to another and therefore, approximate 'rule of thumb' values can be specified as in Table 9.10.

Table 9.10 Saturation and cut off voltages in a Transistor

	V_{CE} (sat)	V_{BE} (sat)	V_{BE} (cutin)	V_{BE} (cutoff)
Silicon	0.3	.75	0.65	0.0
Germanium	0.1	.3	0.2	−0.1

We notice that the voltage across the transistor switches from V_{CC} to V_{CE} (sat) (≈ 0) when the transistor is switched from cut-off to saturation.

9.4.3 INVERSE MODE OF OPERATION OF THE TRANSISTOR

Normally we are not interested in the operation of the transistor in the inverse mode when the collector-base junction is forward biased and the emitter-base junction is reverse biased. Such a situation arises in TTL circuits which we shall describe later. We shall only consider silicon transistors here. Normally the doping of the transistor is so arranged that the normal α ($= \alpha_N$) is larger than 0.98 whereas the inverse α ($= \alpha_I$) is very small being 0.1 or so. The h_{FC}

(d.c. gain) of the inverse mode transistor is thus about 0.1. The biasing of the inverse mode transistor is shown in Fig. 9.12

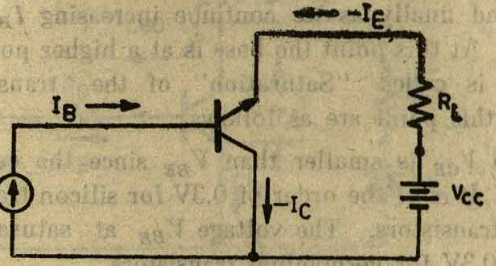


Fig. 9.12 Transistor in the inverse mode

The various currents can be written down as

$$-I_C = -I_E + I_B \tag{9.4.3}$$

$$-I_E = h_{FC} \cdot I_B \tag{9.4.4}$$

We can calculate I_C in terms of I_B by combining eq. (9.4.3) and (9.4.4). Thus

$$I_C = -I_B\,(1 + h_{FC}) \tag{9.4.5}$$

We find that $I_C \approx -I_B$ and $-I_E \ll I_B$.

Example 9.4.1

In a transistor shown in Fig. 9.11, the values are $V_{CC} = 5\text{ V}$, $R_L = 5\text{ K}\,\Omega$, $V_{BB} = 5\text{ V}$ and $h_{FE} = 20$. What value of R_B should be used to keep the transistor in saturation ?

Now

$$I_C = \frac{V_{CC}}{R_L} = \frac{5}{5 \times 10^3} = 1\text{ mA}$$

The voltage at the collector will be about 0.3 V. The base current should be larger than $\dfrac{I_C}{h_{FE}} = \dfrac{1 \times 10^{-3}}{20} = 50\ \mu\text{A}$. If the V_{BE} (sat) is assumed to be 0.75V, then

$$R_B = \frac{V_{BB} - V_{BE\,(Sat)}}{I_B}$$

$$= \frac{5 - 0.75}{50} \times 10^6$$

$$= 85.0\text{ K}\,\Omega.$$

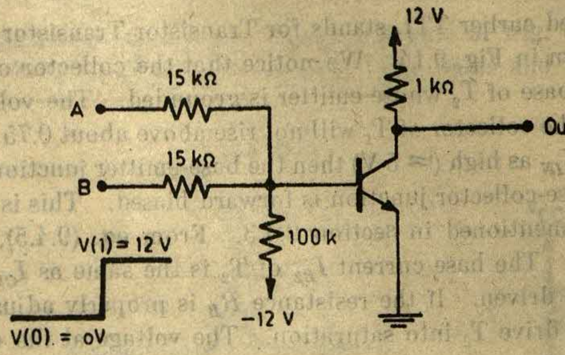
A resistance of 85 K Ω in the base will bring the transistor just into saturation. We should allow a certain factor of safety if we want to ensure that the transistor remains saturated with variations of temperature and h_{FE}. A safety factor of

2 or 3 may be conveniently used and hence R_B should be less than or equal to 40 K Ω.

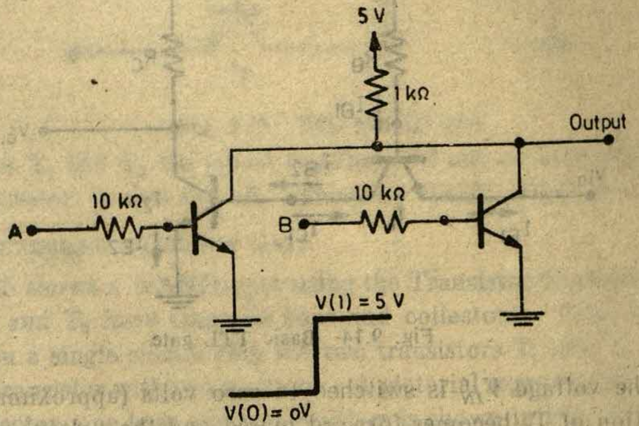
9.4.4 TRANSISTOR SWITCH IN A LOGIC GATE

So far we have discussed the operation of a transistor switch. Before proceeding with a description of logic gates like TTL etc. we shall demonstrate how a switch can be used to generate various logic functions. As mentioned earlier many gate circuits like DTL, RTL etc. have been developed where the transistor switch plays a pivotal role. For demonstration we have two circuits in Fig. 9.13 (a) and (b)

In Fig. 9.13 (a), if both the inputs are zero (logic 0) then only the base voltage is small negative and the transistor is cut off. The output voltage is 12 V. If



(a) One transistor circuit



(b) Two transistor circuit

Fig. 9.13 TWO NOR circuit realisations

any of the inputs goes to 12 V (logic 1) the transistor draws a heavy current and goes into saturation. The output voltage is V_{CE} (sat) $\approx$ 0 volts. This is *NOR* logic and the circuit is a *NOR* gate.

Similarly in Fig. 9.13 (b) if the inputs are at low level (logic 0) then the switches are cut off and the output is high (= 5 V). If any of the inputs becomes high (= 5 V), that particular transistor goes into saturation and the output is almost zero volts. This also, therefore, is a *NOR* gate.

Notice that the transistor goes from saturation to cut off and vice versa, and except for the time take for switching it does not stay in the active region. It is because of this speed of switching that the TTL gates to be described next have become so popular.

9.5 TTL gates

As mentioned earlier TTL stands for Transistor-Transistor logic. The basic TTL gate is shown in Fig. 9.14. We notice that the collector of transistor T_1 is connected to the base of T_2 whose emitter is grounded. The voltage at the base of T_2 and hence the collector of T_1 will not rise above about 0.75 V—the V_{BE} (sat). Now, if we have V_{IN} as high ($\approx$ 5 V) then the base-emitter junction of T_1 is reverse biased and the base-collector junction is forward biased. This is the same inverse mode operation mentioned in section 9.4.3. From eq. (9.4.5), we have $I_{C1} \approx I_{B1}$ with $h_{FC} \leqslant 1$. The base current I_{B2} of T_2 is the same as I_{C1} and hence the base of T_2 will be driven. If the resistance R_B is properly adjusted, this current will be enough to drive T_2 into saturation. The voltage at the collector of T_2 is almost zero volts.

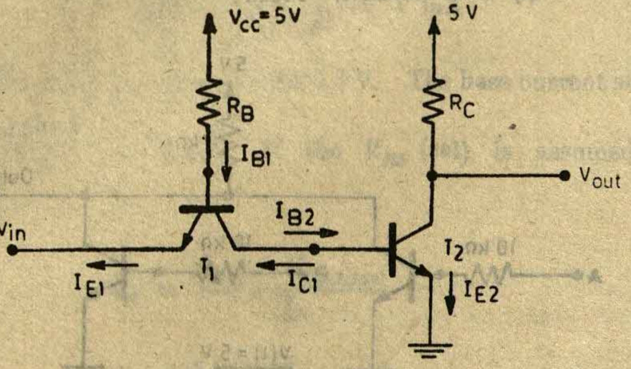


Fig. 9.14 Basic TTL gate

Now the voltage V_{IN} is switched to zero volts (approximately). The base-emitter junction of T_1 becomes forward biased and the voltage at the base of T_1 becomes about 0.75. The collector of T_1 is at about 0.75 V since T_2 was in saturation. Momentarily, therefore, the transistor T_1 is in the active region. The stored charge in the base of T_2 (since T_2 was in saturation) can now flow out as the collector current of T_1. This is the crucial point in the TTL gate. The stored charge is removed as an initial large collector current of another transistor and not allowed to leak away through a large resistance at the base. Unless and until the stored charges are removed the T_2 will not come out of saturation. In this arrangement, therefore, faster action is possible because — $I_{B2} = I_{C1} = h_{FE} \times I_{B1}$. Once T_2 comes out of saturation, it is cut-off and the V_{OUT} goes to $V_{CC} = 5\,V$.

The α_I of T_1 in the TTL gates is made very small by deliberate design and values of $\alpha_I \simeq 0.02$ are quite common. With reference to eq. (9.4.3) and (9.4.5) we can see that the current $I_{C1} = -I_{B1} \times 1.02$ when V_{IN} is high. That is, of the total current I_{B2} $(= I_{C1})$ flowing in the base of T_2 only a small amount is taken from the source connected at the input terminals. The majority of the current about 98 % is supplied by the base circuit of T_1. Thus the circuit of Fig. 9.14 has the additional advantage of taking in a very small current from the drive source.

A logic gate has two inputs. The basic gate of Fig. 9.14 is expanded, as shown in Fig. 9.15, to take in two inputs. The bases and the collectors of the two transistors T_1 and T_2 are joined together. If any or both the two inputs are zero, the transistor T_3 gets cut-off. Thus the circuit shown is a NAND gate.

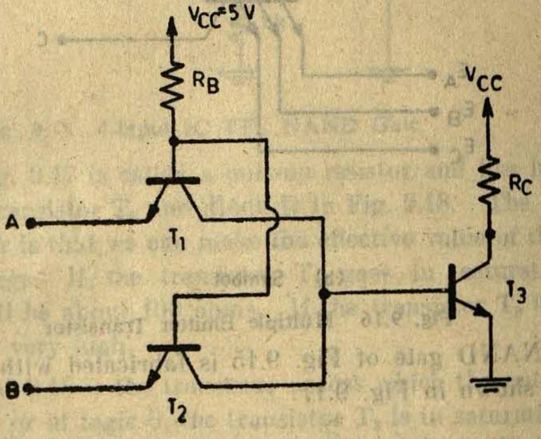
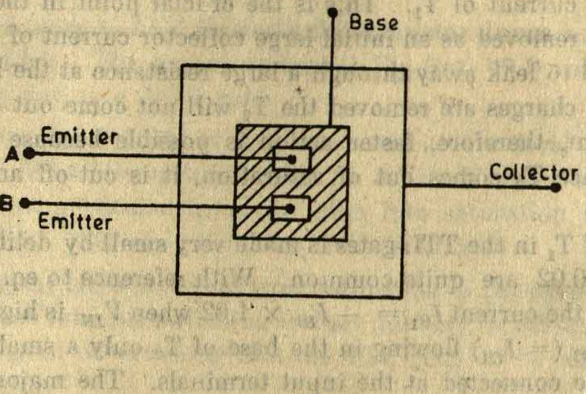


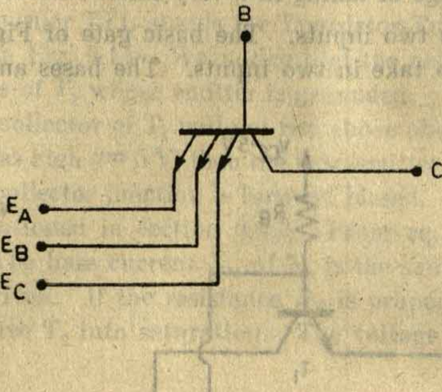
Fig. 9.15 TTL NAND gate

9.5.1 TTL Integrated Circuit Gate

Fig. 9.15 shows a NAND gate using the Transistor-Transistor Logic. The transistor T_1 and T_2 have common base and collectors. Thus while integrating many gates on a single silicon chip the two transistors T_1 and T_2 were integrated into a single transistor with two emitters. A pictorial representation of a transistor with one collector, one base and two emitters is shown in Fig. 9.16 (a). If necessary more emitters can be fabricated on the same base and we would obtain a gate with more than 2 inputs. Fig. 9.16 (b) shows the symbol of a multiple emitter



(a) Method of fabrication



(b) Symbol

Fig. 9.16 Multiple Emitter Transistor

transistor. The NAND gate of Fig. 9.15 is fabricated with a multiple emitter transistor and is shown in Fig. 9.17.

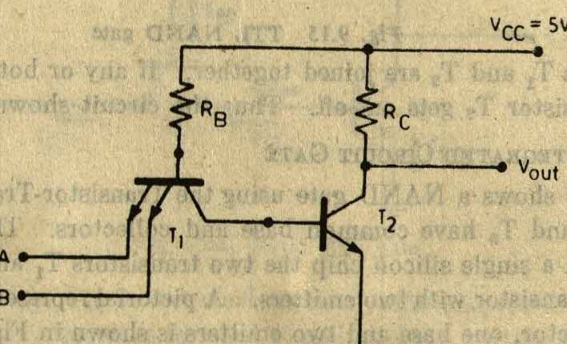


Fig. 9.17 Multiple Emitter NAND circuit

To allow high speed switching and a large fan-out (explained later) the integrated circuit TTL gate is actually fabricated with a totempole pair output circuit. The whole circuit of a typical 4 input IC NAND circuit is shown in Fig. 9.18 with typical values of the resistances used.

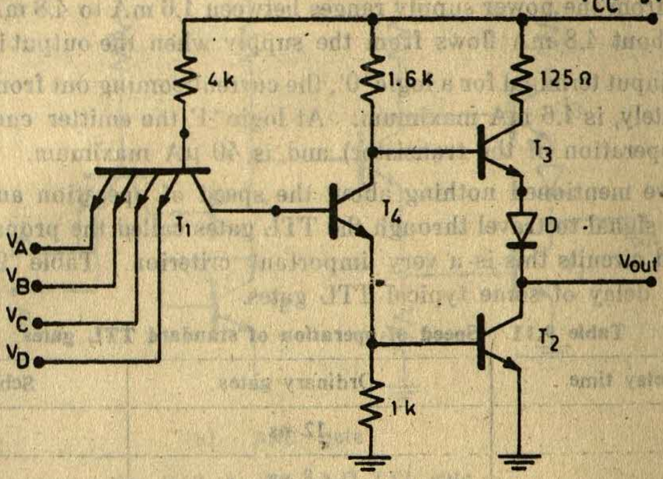


Fig. 9.18 4-input IC TTL NAND Gate

The resistance R_C in Fig. 9.17 is called a pull-up resistor and has been replaced by an active circuit of transistor T_3 and diode D in Fig. 9.18. The advantage of an active pull-up resistor is that we can make the effective value of this resistance very small or very large. If the transistor T_3 goes in saturation then the effective value of R_C will be about 100 ohms. If the transistor T_3 is cut-off, the effective value of R_C is very high.

T_2 of Fig. 9.17 and 9.18 is the transistor across which the output is taken. When the output is low or at logic 0, the transistor T_2 is in saturation and T_3 is cut off. Similarly when the output is high at logic level 1, the T_2 is off and T_3 is in saturation. The phase splitter using the transistor T_4 provides the two drive voltages to T_2 and T_3 in opposite phases. When all inputs are high and the V_{out} is zero, the transistor T_2 is in saturation, and hence the emitter of T_4 is at 0.75 V as expected. Under this condition T_4 will be in saturation and the collector of T_4 will be approximately at 1 volts. Adding the drops across B-E of T_3 and the diode D, we find that this 1 volt cannot drive T_3 and it is cutoff. The diode D prevents T_3 to go into saturation when T_2 is in saturation.

It is necessary for a gate circuit to provide the logic input levels to a number of other such gates. The number of gates driven by a single gate is called the 'fan-out' of that gate. Whenever the logic level is 1, the V_{out} is at V_{CC} and the active pull-up resistor of T_3 and D in Fig. 9.18 has to supply the input currents of the driven gates. Commercial IC gates have a fan-out of 10.

The TTL gate circuits use a V_{CC} of 5 V. The logic 1 is represented by a 'high' voltage and the minimum value of this voltage at the input terminals is 2 volts. The logic 0 is a low voltage and its maximum value is 0.8 V. At the output terminal of the gate typical '1' or 'high' voltage is 3.3 V and the typical '0' or low voltage is 0·22 V. The power dissipation is on an average 10 mwatts. The current from the power supply ranges between 1.6 mA to 4.8 mA. The max. current of about 4.8 mA flows from the supply when the output is at '0' level.

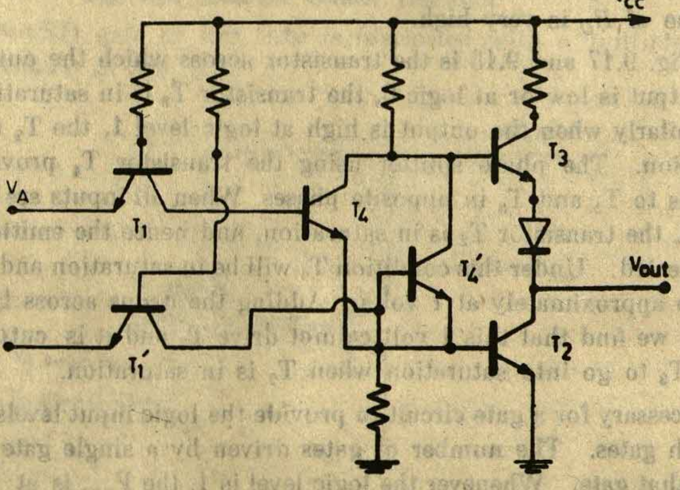
At the input terminal for a logic '0', the current coming out from each emitter tested seperately, is 1.6 mA maximum. At logic '1' the emitter current is going in (inverse operation of the transistor) and is 40 μA maximum.

We have mentioned nothing about the speed of operation and the time it takes for the signal to travel through the TTL gates called the propagation delay. In high speed circuits this is a very important criterion. Table 9.11 lists the propagation delay of some typical TTL gates.

Table 9.11 Speed of operation of standard TTL gates

Propagation delay time	Ordinary gates	Schottky gates
Low to High	12 ns	3 ns
High to Low	8 ns	3 ns

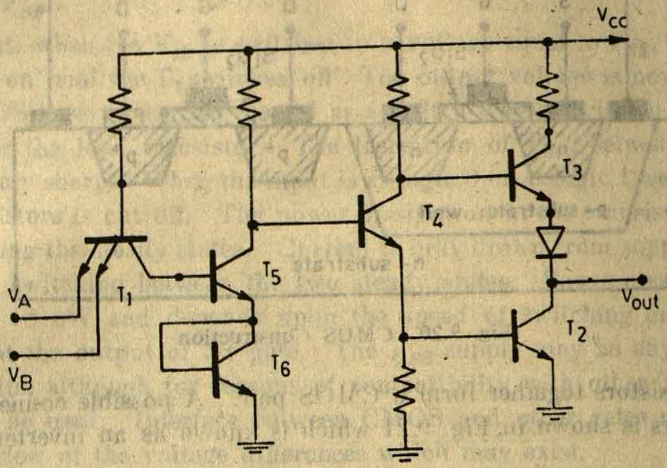
We have so far described only the TTL NAND gate. Ranging from 2 input to 8 input NAND gates are available commercially. TTL technology has also been used to make NOR, OR, AND, and NOT (INVERTER) circuits etc. A NOR and an AND circuit are shown in Fig. 9.19 (a) and (b). The input transistor and the phase splitter of Fig. 9.18 are duplicated in Fig. 9.19 (a) as shown.



(a) NOR gate

Fig. 9.19 (a) An IC NOR Gate

The active pull up and the totem pole output is the same. In the Fig. 9.19 (b) the transistors T_5 and T_6 provide an inversion and thus the circuit is a NOT NAND — i.e., an AND.



(b) AND gate

Fig. 9.19 (b) An AND TTL gate

Schottky diodes and transistors (Section 3.12) have been successfully used in TTL gates to increase the speed of operation. A wide variety of configuration of gates have been marketed but the esssential features of all of them are similar. With improvement in TTL technology large number of gates have been packed in a chip. Other technologies like CMOS have some advantages over TTL which have made them very popular. We shall next describe the CMOS gate.

9.6 CMOS Gates

CMOS stands for Complementary-symmetry Metal-oxide Semi-conductor Field Effect Transistor. CMOS digital logic building blocks have been called the ideal logic circuits. They are characterised by very low power dissipation, high fan-out, large noise immunity and non-critical supply voltage requirements. Their speed of operation, however, is slower than the TTL circuits and the faster CMOS are comparable to the slow TTL circuits. They are available in SSI, MSI and LSI complexity.

Before describing the CMOS gate, we shall briefly explain the construction of a CMOSFET. In section 3.2.3 and particularly in Fig. 3.36 an enhancement mode MOSFET has been described. The CMOSFET consists of a pair of enhancement mode MOSFETS, one a p-channel and another an n-channel type, fabricated together on a n-type substrate. The p-type substrate required for the complementary n-channel MOSFET is obtained by diffusing a p-region into the n-substrate. The construction is shown in Fig. 9.20. Four leads per transistor are brought out.

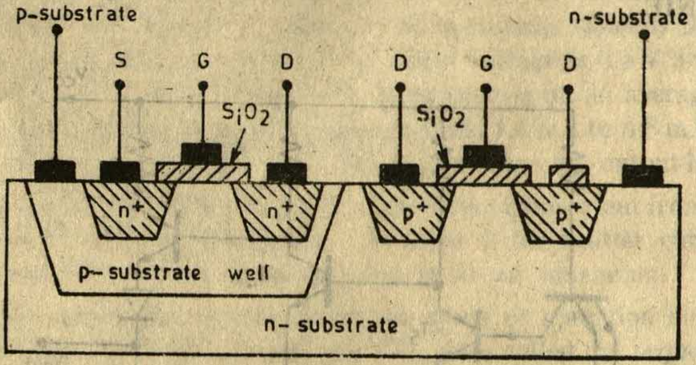


Fig. 9.20 CMOS Construction

The two transistors together form a CMOS pair. A possible connection of the two transistors is shown in Fig. 9.21 which is known as an inverter.

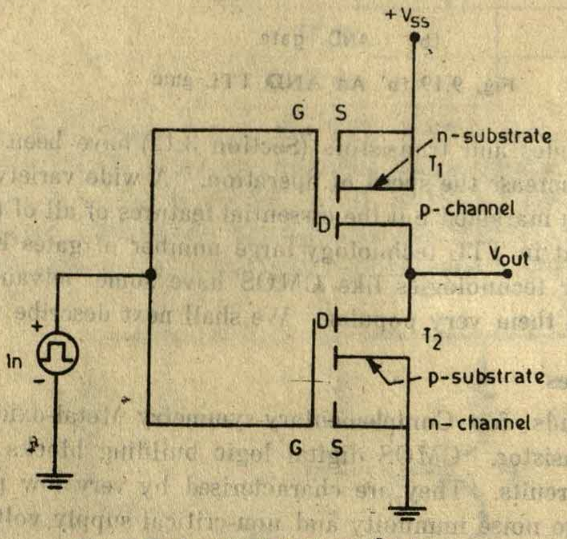


Fig. 9.21 CMOS Inverter

The two drains are tied together and one 'source' is connected to a positive supply voltage with the other 'source' being connected to the ground. The substrate terminals are tied with the source terminals. The two gates are also connected together. Since the transistors are enhancement type (Fig. 3.36 (b)) the *n*-channel MOSFET will conduct when the voltage at the gate is above the threshold and the *p*-channel MOSFET will conduct when the gate voltage is below the threshold. This threshold is dependent upon V_{SS} and is in the range of 2 to 6 volts for a V_{SS} variation of 6 to 15 V — being low for the smaller V_{SS}. If the V_{IN} is low ($\simeq$ 0 V), then the n-channel transistor is 'off'. But the p channel MOSFET is 'on' because the gate voltage of zero volts is lower than the threshold. Since the p-channel MOSFET is in saturation, the output voltage V_{out} is practically equal to V_{SS}.

Next, when the V_{IN} is switched to a voltage equal to V_{SS}, the transistor T_2 switches 'on' and the T_1 switches 'off'. The output voltage is now normally zero. The CMOS inverter can be viewed as a switch where T_2 is the driver transistor and T_1 is the load transistor. The transition of V_{out} between V_{SS} and zero volts is very sharp. When the input is at logic 0 or at logic 1 we find that one of the transistors is cut off. The power dissipation in the transistors is thus negligible during the steady states. Current is only drawn from supply V_{SS} when the circuit is switching between the two steady states. Power dissipation is of the order of 10 nW and depends upon the speed of switching and the capacitive loading at the output of the gate. The V_{SS} supply may be anything between 5 to 15 volts, although for reasons of compatibility with other TTL gate circuits 5 V may be used. Interface between CMOS and other gates must be carefully used in view of the voltage differences which may exist.

9.6.1 CMOS NAND AND NOR CIRCUITS

A conventional 2 input NAND gate of the CMOS family is shown in Fig. 9.22. It uses two 'INVERTERS' of the type described above. The driver

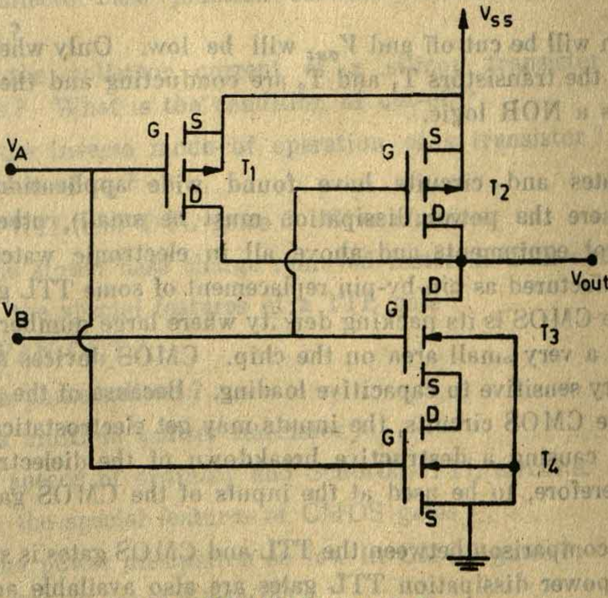


Fig. 9.22 CMOS Nand Gate

transistor T_3 and T_4 are connected in series and the load transistors T_1 and T_2 are connected in parallel. Thus, if any of the inputs V_A or V_B or both are low the T_4, T_3 or both are cut-off. In this position either T_1 or T_2 or both are conducting and hence the output is high. This is a NAND operation. A NOR gate has the two driver transistors in parallel and the load transistors in series as shown in Fig. 9.23. It can be seen that if any or both inputs are high the transistor T_1 or T_2 or both will be cut off and V_{out} will be low. Only when both V_A and V_B are low that the transistors T_1 and T_2 are conducting and the V_{out} is equal to V_{SS}. This is a NOR logic.

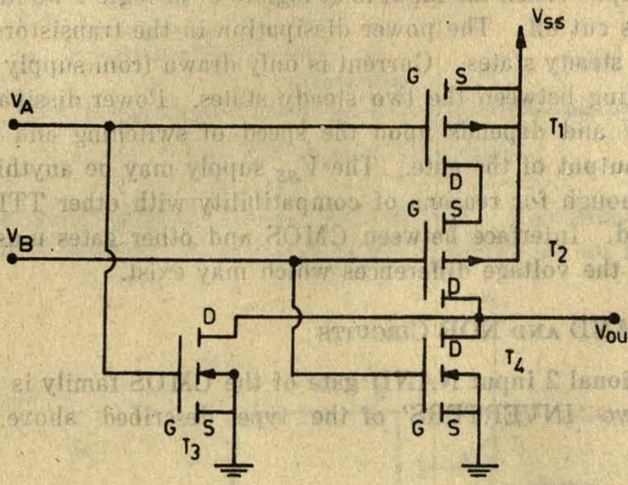


Fig. 9.23 CMOS Nor Gate

CMOS gates and circuits have found wide applications in portable instruments (where the power dissipation must be small), other medical and industrial control equipments and above all in electronic watches. They are sometimes manufactured as pin-by-pin replacement of some TTL gates. Another advantage of the CMOS is its packing density where large number of circuits can be fabricated in a very small area on the chip. CMOS devices are slower than TTL and are very sensitive to capacitive loading. Because of the very high input impedance of the CMOS circuits, the inputs may get electrostatically charged to a high voltage causing a destructive breakdown of the dielectric. Protection circuits have therefore, to be used at the inputs of the CMOS gates.

A table of comparison between the TTL and CMOS gates is shown in Table 9.12. The low power dissipation TTL gates are also available and their power dissipation as well as speed are comparable to CMOS circuits.

Table 9.12 Comparison of TTL and CMOS gates

	Power Dissipation	Propagation Delay	Fanout	Max clock Frequency	Noise Immunity
TTL	10 mW	10 n sec (5 n sec Schottky)	10	35 MHz (45 MHz Schottky)	IV
CMOS	10 nW	20 n sec.	50	16 MHz	4V (V_{SS}= 10V)

Review Questions

9.1 What are the truth tables of AND, OR, NOT, NOR and NAND functions ?

9.2 What are the truth tables of EX-OR and EX-NOR ?

9.3 What are Complementary and Dual functions ?

9.4 What are Boolean functions ?

9.5 Give the associative, commutative and distributive laws in Boolean algebra.

9.6 What is De Morgan's theorem ?

9.7 What is half adder ?

9.8 How is arithmetic operation of addition performed by logic circuits ?

9.9 What is the truth table of a Full Adder.

9.10 Realise an EX-OR using NOR gates only.

9.11 What are the voltages of the base and the collector with respect to the emitter in a transistor in saturation ?

9.12 Is the collector-base junction forward biased when transistor is in saturation ?

9.13 What is the collector current of a silicon transistor under cut-off conditions ? What is the condition of cut-off ?

9.14 What is the inverse mode of operation of a transistor ? What is the normal value of α_1 ?

9.15 What are RTL and DTL gates ? Give circuits.

9.16 Why is the stored base charge removed faster in TTL circuits ?

9.17 What are the special features of a TTL gate ?

9.18 What is FAN-OUT ?

9.19 What is a phase-splitter ?

9.20 What is a multiple emitter transistor ?

9.21 Compare speeds of ordinary and Schottky TTL circuits.

9.22 What are the special features of CMOS gates ?

9.23 Why is the power dissipation so low in CMOS gates ?

9.24 How are CMOS gates fabricated ?

Problems

P 9.1 Simplify the following Boolean Expressions.

(i) $AB\overline{C}D + B\,\overline{C}\,\overline{E} + AE$

(ii) $(\overline{A} + F + \overline{C})\,(\overline{A} + F + G + H)\,(C + G)$

(iii) $\overline{P}QR + AR + QRD + \overline{D}\overline{A}$

(iv) $C\,\overline{A}\,\overline{B} + C\overline{A}\overline{B}D + \overline{B}C$

(v) $\overline{A}B + \overline{B}C + DAC + \overline{E}\overline{C} + \overline{E}DF$

P 9.2 A patient is brought to a hospital for admission. The duty nurse may admit only if the patient is

1. registered for that hospital and is male and suffering from jaundice

or 2. registered for that hospital and is suffering from jaundice and is a student

or 3. not registered for that hospital and is suffering from jaundice and is female.

or 4. male and a student

or 5. suffering from jaundice and is not a student. Write out a logical statement and simplify.

P 9.3 Convert 429.25 into a binary, hexagesimal and octal numbers.

P 9.4 Draw the circuit diagram of a 4 bit Full Adder. The numbers are $A = 1101$ and $B = 1011$.

P 9.5 Subtract $A = 1010$ from $B = 1101$ and show the full scheme of the circuit.

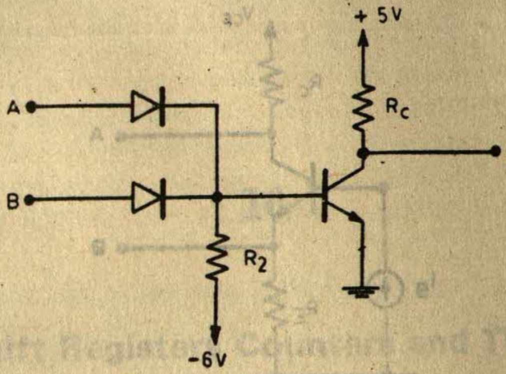
P 9.6 The two inputs A and B are available. Draw the logic circuit of the EX-OR function using only (i) NAND circuits (ii) NOR circuits.

P 9.7 A silicon transistor switch has a collector resistance R_L (in Fig. 9. 10) or 1 K Ω, $V_{cc} = 5$ V, and $h_{FE\,(min)} = 25$. What base current is required to drive the transistor into saturation ? What are the voltages at the collector and the base ? Will the transistor be cut off if the base drive current is zero.

P 9.8 The output of the switch of P.9.7 drives other circuits. Find the maximum current that this circuit can 'Source'. What will happen if the current it drives is more than the maximum calculated ?

P 9.9 What are the characteristics of the transistor in the inverse mode of operation ? Will it provide a gain, either current or voltage ?

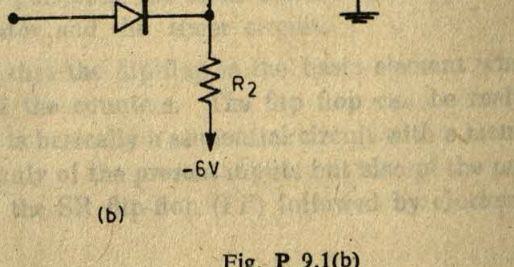
P 9.10 Diode-Transistor-Logic (DTL) circuits are shown in Fig. P 9.1. Show that the circuit (a) is an OR circuit. Calculate suitable values of R_C and R_2 if a source current of 2 mA is required to be available at the output. Given $h_{FE} = 30$.



(a)

Fig. P 9.1(a)

P 9.11 Show that the DTL circuit shown in P 9.1(b) is a NAND circuit. Calculate suitable values of R_C, R_1 and R_2 if $I_C = 5$ mA and $h_{FE} = 20$.



(b)

Fig. P 9.1(b)

P 9.12 A phase splitter circuit is shown in Fig. P 9.2. Show that the two outputs are in opposite phase. What should the value be of R_C and R_E to make the two outputs almost equal ?

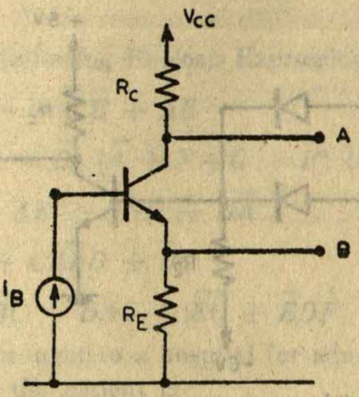


Fig. P9.2

P 9.13 Show how the Diode D in the totem-pole output circuit in Fig. 9.18 prevents the saturation of T_3 when $V_{out} = 0$. Calculate the current through it during the time it does conduct. What are the limits on this current ?

P 9.14 Draw the circuit diagram of a COMS AND circuit.

P 9.15 If a transistor takes time to switch 'off' from the 'on' condition because of the stored base charge then why does it take time to switch 'on' from 'off' when there is no stored base charge condition to satisfy ?

10

Shift Registers Counters and Timers

10.0 Introduction

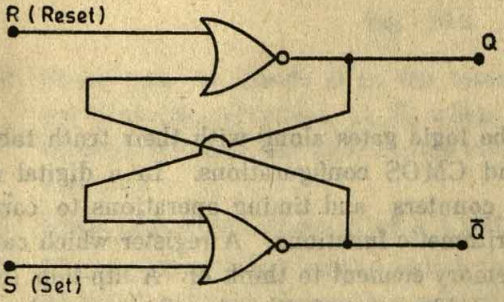
We have so far discussed the logic gates along with their truth table and realisation techniques in TTL and CMOS configurations. In a digital system we do require memory elements, counters and timing operations to carry out and control various binary and arithmetic functions. A register which can store a binary 1 or 0 is the simplest memory element to think of. A flip-flop (bistable multivibrator) which can have two stable states of either 1 or 0 is one such register. We shall in this chapter describe some of the common flip-flops in use and later on show how a cascade of flip-flops forms a register. The binary bits once entered into the register can be shifted to the left or to the right and thus the name of 'shift' register. A combination of flip-flops can be connected as a counter where the state of the flip-flop is directly related to the number of input pulses. Binary or decade counters are invariably used in digital system to count the number of pulses and synchronise arithmetic operations. Finally, we have discussed in this chapter the timing circuits where precise waveforms proportional to time can be generated. In particular we shall discuss the monostable multivibrator, the astable multivibrator and the timer circuit.

We observe that the flip-flop is the basic element which is used in all the shift registers and the counters. The flip flop can be realised using NOR and NAND gates. It is basically a sequential circuit with a memory where the output is a function not only of the present inputs but also of the past circuit states. We shall first discuss the SR flip-flop (FF) followed by clocked FF, the JK, and D flip-flops.

10.1 SR Flip-Flop

A flip-flop as mentioned above is a memory device and has two stable states which are called 1 or 0. The '1' state is also called 'Off' or the 'High' (H) state and the '0' state is called 'on' or the 'Low' (L) state. It has two complementary level outputs called Q and $\bar{Q}$. Whenever Q is at the state 1. the $\bar{Q}$ is at the state '0' and vice versa. A simple S (Set) R (Reset) flipflop using NOR gates is shown in Fig. 10.1. The outputs of the NOR gates are cross coupled to the input. Now, let us assume that S is High and R is low. In a NOR gate if any of the inputs goes to 1, the output goes to '0'. Therefore we get $\bar{Q} = 0$ and hence $Q = 1$. This is also consistent with the cross connection. Thus, if the Set input is High the Q output is High. In other words the FF is set to High by a signal at the S terminal.

Similarly, if the Reset input is High then we can see that the Q is Low and $\bar{Q}$ is High. The FF is thus reset to '0'. The truth table of the SR FF is shown in Fig. 10.1 (b). Here Q_{n+1} represents the state of the FF after the change has been made at the input and, therefore, Q_n represents the state of the FF just before the event. If both S and R are Low, then the FF does not change state and Q_{n+1} is the same as Q_n. The input $S = R = 1$ is not used since the outputs Q and $\bar{Q}$ both will become' 0' — a condition which is contradictory to the assumption that Q and $\bar{Q}$ are complementary. Further, if the input now changes to $S = R = 0$, then the output will be unpredictable. It could either be 1 or 0 with equal ease. In view of these difficulties the situation $S = R = 1$ is not used.



(a) Circuit diagram

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	not used

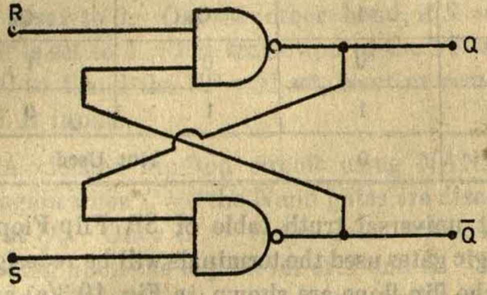
(b) Truth table

Fig. 10.1 SR Flip Flop

To summarise the operation of the SR flip-flop, therefore, we can say that the state of the FF does not change if $S = R = 0$. The FF is 'Set' to High if $S = 1$ and $R = 0$ and conversely, it is 'reset' to Low if $S = 0$ and $R = 1$.The FF retains its state unless it is either Set or Reset again. Thus it behaves like a memory element storing one bit of data.

10.1.1 NAND GATES IN SR FLIP-FLOPS

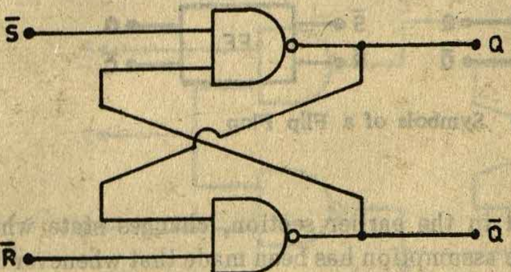
An SR flip-flop using NAND gates is shown in Fig. 10.2 (a). Here also when $S = 0, R = 1$ the FF is reset to Low. Similarly, when $S = 1, R = 0$, the FF is set to 'High'. We should remember that in a NAND gate if any of the inputs goes to Low, the output of the gate becomes High. In other words the gate is 'disabled' when any of the inputs is '0'. It is 'enabled' when both the inputs are 1. The FF does not change state when $S = R = 1$ and becomes indeterminate and inconsistent when $S = R = 0$.



(a) Circuit diagram

S	R	Q_{n+1}
0	0	not used
0	1	0
1	0	1
1	1	Q_n

(b) Truth table



(c) Redefined terminals

$\bar{S}$	$\bar{R}$	Q_{n+1}
0	0	not used
0	1	1
1	0	0
1	1	Q_n

(d) Truth table

Fig. 10.2 SR Flip Flop using NAND gates

Looking at the truth table in Fig. 10.2 (b) we notice that it is not at all consistent with the truth table of FF given in Fig. 10.1 (b). If we choose to define the operation of an SR flip-flop in the manner of Fig. 10.1 (b) as correct then the condition $S = R = 1$ is unusable. In the SR flip-flop of Fig. 10.2 (a) the condition $S = R = 0$ is unusable. In order to make the terminology consistent the terminals of the NAND flip-flop are redesignated as shown in Fig. 10.2 (c). The truth table of this FF is given in Fig. 10.2 (d). Whenever $\bar{S} = 1$ and $\bar{R} = 0$ the FF is reset and when $\bar{S} = 0$, $\bar{R} = 1$ the FF is 'set' to 1.

Now, if we imagine two fictitions inputs S and R whose complements are $\bar{S}$ and $\bar{R}$ respectively then, whenever $S = 0, R = 1$ ($\bar{S} = 1, \bar{R} = 0$) the FF is reset to 0. Similarly when $S = 1$ $R = 0$ ($\bar{S} = 0, \bar{R} = 1$) the FF is set to 1. This condition is the same as given in Fig. 10.1 (b) and 10.2 (b). The difference now, however, is that whenever the fictitious inputs $S = R = 1$ ($\bar{S} = \bar{R} = 0$) the flip-flop states are unusable. This is again consistent with our earlier definition of the FF. The truth table will therefore, be as given in Table 10.1.

Table 10.1 Truth Table of SR Flip Flop

S	R	$\overline{S}$	$\overline{R}$	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	1	1	Q_n	$\overline{Q}_n$
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	Not Used	

We have defined a consistent universal truth table of SR Flip Flop with Table 10.1. Depending upon the logic gates used the terminals will be redesignated The terminals and the symbols of the flip-flops are shown in Fig. 10.3(a) and (b) The truth table of Table 10.1 is applicable in each case.

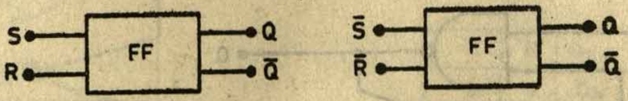


Fig. 10.3 Symbols of a Flip Flop

10.1.2 CLOCKED FLIP-FLOP

The SR flip flop, discussed in the earlier section, changes state whenever the Set/Reset inputs change. The assumption has been made that whenever $S = 0$, $R = 1$, the Q output is reset to Low level, and if $S = 1$, $R = 0$, then the FF is set to a High level. If, on the other hand, $S = 0$, $R = 0$ then the FF does not change state. In a large system where this flip-flop is going to be used, the sequence of arrival of S and R inputs cannot be ensured and the FF may end up in a wrong state. It may produce erroneous signals at the output. A very neat solution is to clock the flip-flop with an external signal in such a way that the FF becomes active for a very short period. Once the logic levels at the input of the FF have assumed steady values, the clock enables the Set/Reset input to be connected to the flip-flop. A clocked flip-flop is shown in Fig. 10.4.

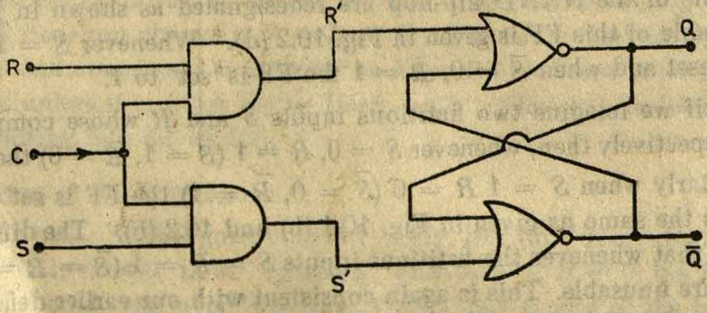
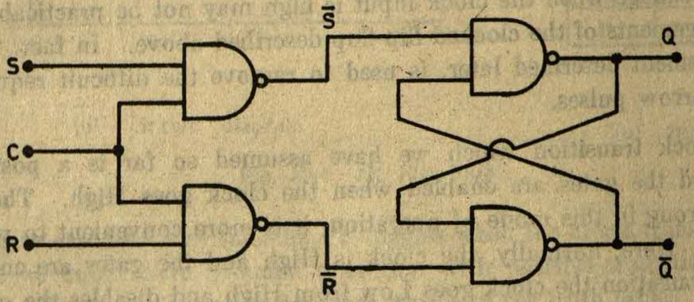


Fig. 10.4 Clocked Flip-Flop

As long as $C = 0$, the output of the two AND circuits are going to be 0. The state of the FF will remain unchanged since $S' = R' = 0$. Now with $C = 1$, the two AND gates are enabled and if $S = 0$, $R = 1$, then $S' = 0$, $R' = 1$ and the FF is reset to 0. On the other hand, if $S = 1$, $R = 0$, then $S' = 1$, $R' = 0$ and the FF is set to 1. The transition of the FF will thus take place when C changes from 0 to 1 and the FF will set, reset or remain unchanged depending upon the S and R inputs.

A clocked flip-flop circuit using NAND gates is shown in Fig. 10.5 (a). Here again when $C=0$ the Nand gates are disabled and $\bar{S}=\bar{R}=1$ maintaining the state at Q_n. Once $C = 1$, the gates are enabled and the output sets or resets depending upon the logic level of S and R. The truth table of a clocked flip-flop is given in Fig. 10.5 (b). The arrow on the rising edge of the clock pulse indicates the instant of the transition.



(a) Circuit diagram

Clock	S	R	Q_{n+1}
	0	0	Q_n
”	1	0	1
”	0	1	0
”	1	1	not used

(b) Truth table

Fig. 10.5 Clocked SR FF using NAND gates

As long as the clock is at the High level the S/R inputs are enabled and connected to the FF. Thus any change in S and R subsequent to the clock transition are coupled to the output of the flip-flop. This is one of the serious draw-backs of the clocked FF of Fig. 10.4 and 10.5. If the width of the clock pulse is now made very narrow, then the gates will be enabled for a very short period and some of the problems of erroneous operation of the FF will be reduced. Thus, it is required that the clock pulses be very narrow in the FF of Fig. 10.4 and 10.5. Such a requirement will mean that the pulse duration be smaller than the propagation delay of the FF. For example any signal at the input of the FF takes some finite time to travel to the output circuit. In a TTL circuit this delay may be typically of the order of 20 nsecs. The positive going transition of C changing from 0 to 1 will thus take 20 nsecs to reach the output terminal. The gates must be disabled by the time the signal reaches the output in order to avoid any false triggering or changes at the S/R inputs which occur later. Such narrow pulses are difficult to produce and manage and, therefore, making the trigger pulses very narrow may not work well.

We come to the conclusion that even such a requirement that the S/R inputs should only change when the clock input is high may not be practicable with the simple arrangements of the clocked flip-flop described above. In fact, the Master-slave arrangement described later, is used to remove the difficult requirement of extremely narrow pulses.

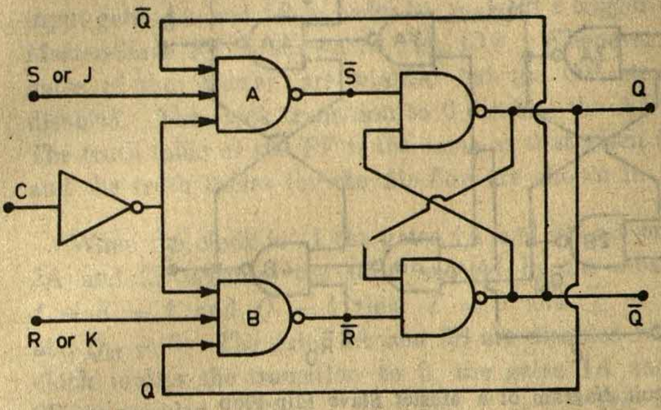
The clock transition which we have assumed so far is a positive going transition and the gates are enabled when the clock goes High. Though there is nothing wrong in this mode of operation, it is more convenient to work in the other mode. Here, normally, the clock is High and the gates are enabled. At the desired transition the clock goes Low from High and disables the gates. The operation of the FF takes place at the negative transition of the clock pulse. As we shall see later, this mode of operation is preferred.

10.1.3 J. K. FLIP-FLOPS

In the SR flip-flops discussed above, the output of the FF is governed solely by the S and R inputs. However, we can arrange the input circuit in such a fashion that the output is governed not only by the S and R inputs but also by the state of the FF. Such a connection is shown in Fig. 10.6 (a) and is called the JK flip-flop.

The outputs Q and $\bar{Q}$ are connected back to the input gates in a cross coupled fashion. Thus, the input to the stearing gate A is J (S), clock and the $\bar{Q}$ output and to the other gate B is K (R), clock and Q output. The truth table of the JK flip-flop is shown in Fig. 10.6 (b). When the C is 1 the NAND gates A and B are disabled, since one of the inputs of the gate is 0. The $\bar{S} = \bar{R} = 1$ and the Q outputs are undisturbed. Now, let us assume that $Q = 1$ and $\bar{Q} = 0$ and that $J = K = 1$. Once the clock C goes to 0 the gates A and B are enabled. Since $\bar{Q} = 0$ the output of the gate A is 1 and the output of the gate B is 0. This means that $\bar{S} = 1$ and $\bar{R} = 0$ and the FF changes state making $Q = 0$ and $\bar{Q} = 1$. If we had assumed that $Q = 0$ and $\bar{Q} = 1$ initially, then $\bar{S} = 0$ and $\bar{R} = 1$ when the clock changes from 1 to 0. The output of the FF will become $Q = 1, \bar{Q} = 0$.

Thus every time the clock changes from 1 to 0 the state of the flip-flop changes irrespective of its previous state. The FF is said to Toggle when J = K = 1.



(a) Circuit diagram

Clock	J	K	Q_{n+1}
⎍	0	0	Q_n
”	0	1	0
”	1	0	1
”	1	1	toggle

(b) Truth table

Fig. 10.6 JK Flip-Flop

We have assumed here that the FF toggles when the clock transition is from 1 to 0 but we could have assumed operation with positive transition of C with equal ease. We can easily verify the other entries of the truth table. For instance if $J = K = 0$, the FF cannot change state since $\overline{S} = \overline{R} = 1$ all the time and $Q_{n+1} = Q_n$. If $J = 0$ and $K = 1$, then, with C changing to 0, the Q will become 0, Similarly when $J = 1, K = 0$, the Q output will change to 1, if it was not already 1, after the clock is applied.

The difficulty of requiring a very narrow trigger pulse to avoid any false triggering is still present in the circuit of Fig. 10.6. The Master—Slave flip-flop to be described next takes care of this problem.

10.1.4 MASTER-SLAVE FLIP-FLOP

We have seen in the flip-flop of Fig. 10.6 that after the clock C goes to 0 and the transition has taken place the gates A and B are still enabled and any subsequent changes at J and K will be passed on to the outputs. To overcome this difficulty we use two clocked flip-flops in tandem called the Master and the Slave. We arrange them in such a fashion that the input data is entered into the Master flip-flop and transferred to Slave flip-flop subsequently on the negative edge of the clock. At this time the Master FF is disabled. The circuit diagram of a simple Master-Slave FF is shown in Fig. 10.7.

The clocks to the Master and Slave flip-flops are complementary to each other. When C is 1, the $\overline{C} = 0$. The Master flip-flop consisting of 2A and 2B

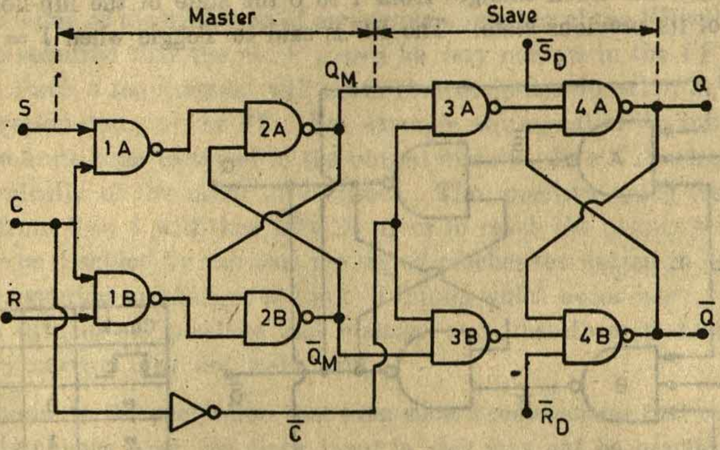


Fig. 10.7 Circuit diagram of a Master Slave Flip-Flop

gates has 1A and 1B as the stearing gates. Similarly the Slave flip-flop has 3A and 3B as the stearing gate and 4A and 4B form the flip flop. The output of the Master is connected directly to the Slave FF. Now if $C = 1$ the gates 1A and 1B are enabled and the gates 3A and 3B are disabled. The Slave FF is not effected by any change in the output of the Master FF. The output Q_M will be decided by the S/R inputs. Thus, if $S = 1$, $R = 0$, then $Q_M = 1$, $\bar{Q}_M = 0$. Similarly, if $S = 0$, $R = 1$, then $Q_M = 0$, $\bar{Q}_M = 1$. Q_M remains unchanged if $S = R = 0$.

When the clock transits from 1 to 0, the gates 3A and 3B are enabled but the Master FF is disabled. Q_M and $\bar{Q}_M$ are frozen and do not depend any more on S/R inputs. If $Q_M = 1$, the final output Q of the Slave FF will be 1 since the output of the gate 3A is 0. Similarly it can be shown that the Slave FF will have the same truth table as that given in Table 10.1.

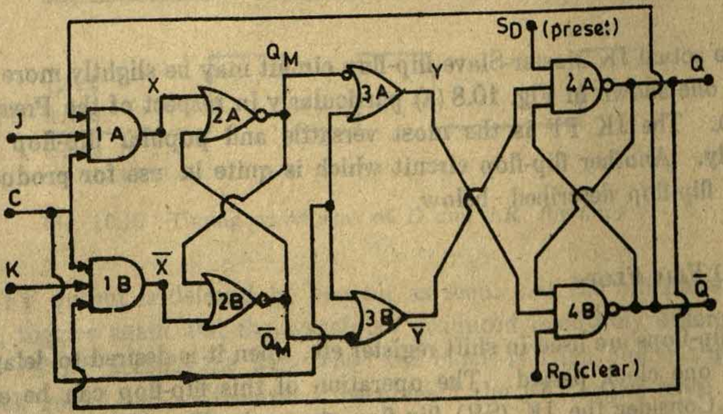
The main advantage of this arrangement is that the data at the inputs is entered into the FF when the clock is 1 and is transferred to the output FF when the clock goes to 0. In the meantime the input FF is disabled and, thus, there is no chance of a false triggering. With such an arrangement it is not necessary to have a very narrow clock pulse. We are also in the happier position of obtaining an output when the input control is changing from an enable to a disable operation thereby making the circuit trouble free.

Two terminals marked $\bar{S}_D$ and $\bar{R}_D$ are also shown in Fig. 10.7. These are direct Set and Reset inputs of the FF and they override all other input and clock conditions. Thus, when $\bar{S}_D = 0$ and $\bar{R}_D = 1$, the FF sets to 1 and when $\bar{S}_D = 1$, $\bar{R}_D = 0$, the FF resets to 0 irrespective of anything else. Normally these terminals are kept at 1 and are used to Set or Reset the FF directly as desired.

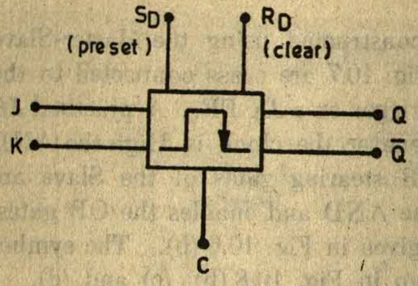
10.1.5 J. K. MASTER-SLAVE FLIP-FLOPS

The JK flip-flop of Fig. 10.6 can be constructed using the Master-Slave principle described above. The Q and $\bar{Q}$ of Fig. 10.7 are cross connected to the input gates 1A and 1B in order to make it a trigger or a JK FF. A practical JK Master-Slave FF is shown in Fig. 10.8. Whenever the clock is High the AND gates of the 'Master' are enabled but the OR stearing gates of the Slave are disabled. The clock transition to 0 disables the AND and enables the OR gates. The truth table of the FF is the same as that given in Fig. 10.6 (b). The symbol and the truth tables for the flip-flop are shown in Fig. 10.8 (b), (c) and (d).

When the clock is 1 the gates 1A and 1B are enabled. The 'Master' FF of 2A and 2B assumes the state selected by the stearing gates. For example, if $J = K = 1$ and $Q = 1$ then $X = 0$ and $\bar{X} = 1$. This will make $Q_M = 1$ and $\bar{Q}_M = 0$. The gates 3A and 3B are disabled when $C = 1$. As soon as the clock makes the transition to 0, the gates 1A and 1B are disabled and 3A and 3B are enabled. Hence $Y = 0$ and $\bar{Y} = 1$. The 'Slave' FF is therefore changed to $Q = 0, \bar{Q} = 1$. A toggling or a change of state will occur as long as $J = K = 1$ and clock transits from 1 to 0. Similarly if $J = 1, K = 0$ and $Q = 0$ then, with $C = 1$ we will have $X = 1, \bar{X} = 0$ and $Q_M = 0, \bar{Q}_M = 1$. Now as C goes to 0, we will get $Y = 1$ and $\bar{Y} = 0$ making $Q = 1$ as required from the truth table. We can verify in a similar fashion the other two entries in the truth table. This table describes the Synchronous operation of the FF. The truth table in Fig. 10.8 (d) describes the Asynchronous operation when the direct Preset and Clear inputs override the clock and the JK inputs. Normally S_D and R_D are kept High. Once R_D goes to 0 the Q output is 0. Similarly if S_D goes to 0, the Q output is set to 1.



(a) Circuit diagram



(b) Symbol

Synchronous

J	K	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	toggle	—
1	0	1	0
0	1	0	1
0	0	Q_n	$\bar{Q}_n$

(c) Truth table

Asynchronous

$\bar{S}_D$	R_D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	not used	
0	1	1	0
1	0	0	1
1	1	Q_n	$\bar{Q}_n$

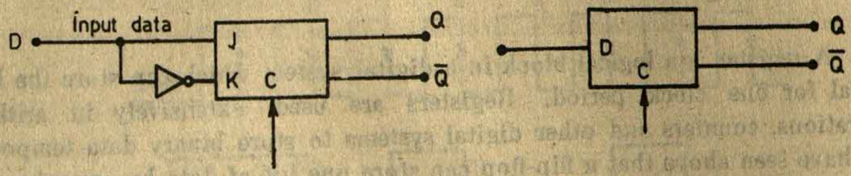
(d) Preset and clear

Fig. 10.8 JK Flip-Flop

The actual JK Master-Slave flip-flop circuit may be slightly more complicated than the one shown in Fig. 10.8 (a) particularly in respect of the Preset and Clear operation. The JK FF is the most versatile and popular flip-flop and is used extensively. Another flip-flop circuit which is quite in use for producing a delay is the D flip-flop described below.

10.1.6 D FLIP-FLOPS

D flip-flops are used in shift register etc. when it is desired to delay the digital signal by one clock period. The operation of this flip-flop can be explained as follows. Consider the JK (SR) flip-flop shown in Fig. 10.9 (a) where the input data signal is connected to J and the inverse of the signal to K. If $D = 0$ then $J = 0$, $K = 1$ and at the negative transition of the clock $Q = 0$, $\bar{Q} = 1$. When



(a) Circuit arrangement (b) Symbol

Fig. 10.9 D Flip-Flop

$D = 1$ we have $J = 1$, $K = 0$ and, therefore, $Q = 1$ if the negative clock transition takes place. Since all the capabilities of the JK FF are not utilised in working as a *D* type, a seperate *D* type FF is also made in *IC* circuits and its symbol is shown in Fig. 10.9 (b). The difference of operation of a JK and a D flip-flop can be explained with the help of the diagram in Fig. 10.10.

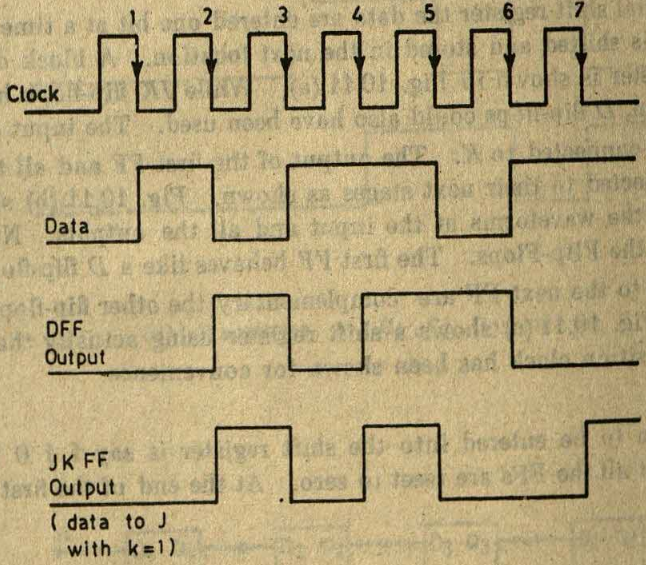


Fig. 10.10 Timing waveforms of D and J.K. flip flops

The *D* FF output is delayed by one bit as seen. At the 5th pulse the *JK* FF, however, toggles again and the waveform produced is entirely different. As we know the *JK* FF accepts the data when the clock is High and changes state when the clock goes Low. Whenever *J* becomes 1 the FF toggles since $K = 1$. The *D* Flip-flop has been shown to operate on the negative transition of the clock but it would operate equally well on the positive edge if so designed. Special purpose *D* FF may be constructed directly without taking recourse to a *JK* construction.

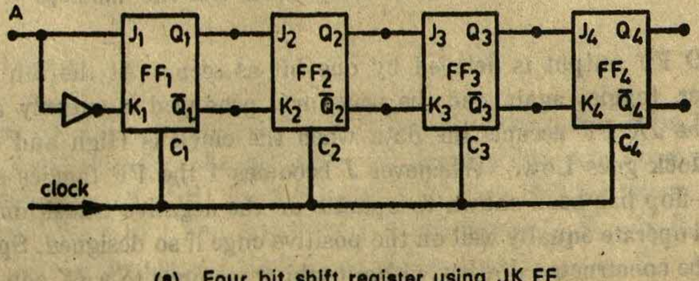
10.2 Shift Registers

A register is a logical block in a digital system which can store the binary signal for one clock period. Registers are used extensively in arithmetic operations, counters and other digital systems to store binary data temporarily. We have seen above that a flip-flop can store one bit of data by assuming either a 1 or a 0 state. The simple single FF, therefore, is a one bit register. If a larger number of bits, say *N*, have to be stored then *N* flip-flops are required. The array of flip-flops with a number of bits stored in them will be a *N* bit register. Sometimes it is required to shift the bits from one flip-flop to another. A register where the bits can be shifted on command is called a Shift register. A shift register may have provisions to (i) enter data serially, parallely or both and (ii) shift the data to the right or to the left.

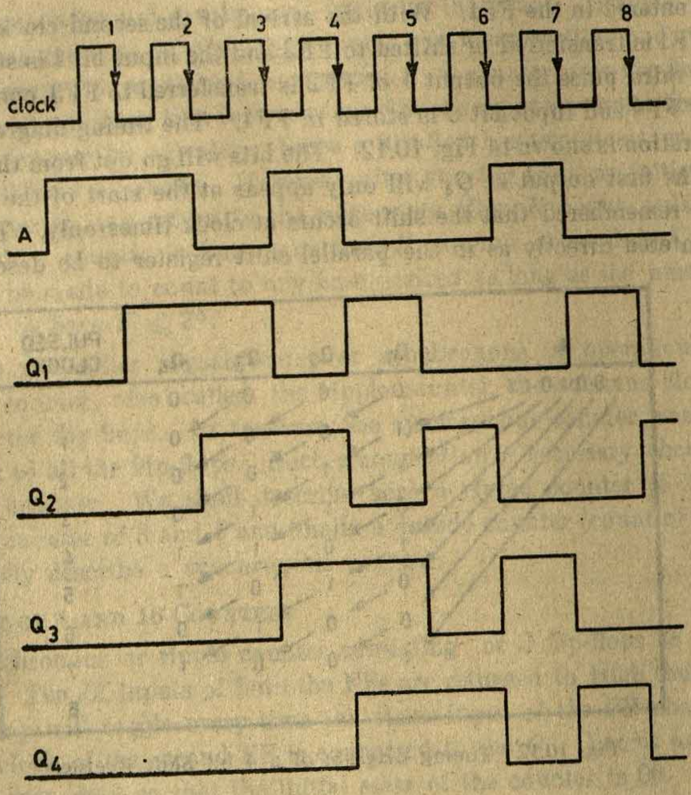
10.2.1 SERIAL SHIFT REGISTER

In a serial shift register the data are entered one bit at a time serially. The previous bit is shifted and stored in the next location. A block diagram of a 4 bit shift register is shown in Fig. 10.11 (a). While *JK* flip-flops have been used for illustration, *D* flip-flops could also have been used. The input *A* is connected to *J* and $\overline{A}$ is connected to *K*. The output of the first FF and all the subsequent FFs are connected to their next stages as shown. Fig. 10.11 (b) shows a timing diagram and the waveforms at the input and all the outputs. Notice the shift of the bits in the Flip-Flops. The first FF behaves like a *D* flip-flop and since *Q* and $\overline{Q}$ inputs to the next FF are complementary the other flip-flops also are like the *D* FF. Fig. 10.11 (c) shows a shift register using actually the *D* FFs only. Negative transition clock has been shown for convenience.

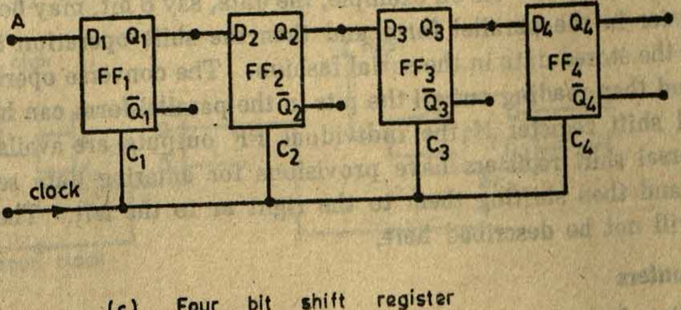
The data to be entered into the shift register is say 1 1 0 1 0 0 1. Let us assume that all the FFs are reset to zero. At the end of the first clock the bit



(a) Four bit shift register using JK FF



(b) Waveforms at Q_1, Q_2, Q_3 and Q_4



(c) Four bit shift register

Fig. 10.11 Four bit shift Register

1 will be entered in the FF1. With the arrival of the second clock transition the bit 1 in FF1 is transferred or shifted to FF2 and the input bit 1 is stored into FF2. After the third pulse the output 1 of FF2 is transferred to FF3, content of FF3 is shifted to FF4 and input bit 0 is stored in FF1. The timing diagram of pulse by pulse operation is shown in Fig. 10.12. The bits will go out from the shift register at Q_4. The first output at Q_4 will only appear at the start of the 4th pulse. It should be remembered that the shift occurs at clock times only. The data could also be entered directly as in the parallel shift register to be described next.

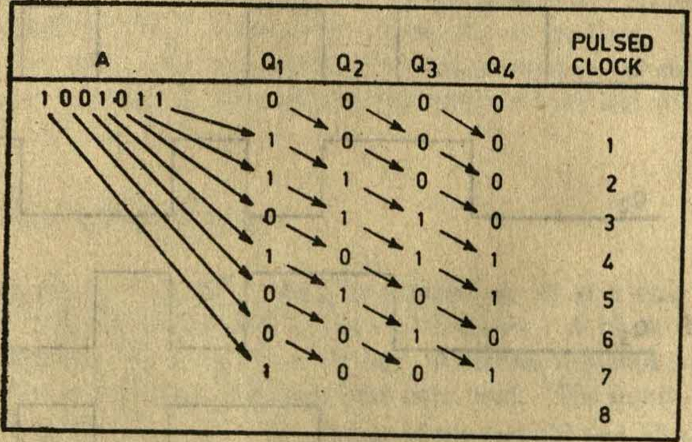


Fig. 10.12 Timing diagram of a 4 bit Shift Register

10.2.2 PARALLEL SHIFT REGISTER

The data can be entered into the shift register directly by using the Direct asynchronous inputs of the flip-flops. As we have seen in Fig. 10.8 (d), the S_D and R_D inputs can be used to enter any desired bit into the FF and hence the shift register can be loaded parallely in one operation. The parallel loading is naturally much faster than the serial loading because in the latter case the bits are entered one by one. The parallel shift registers can be used for conversion of data from parallel to serial form. As an example, the data, say 8 bit, may be loaded into the shift register in the parallel form and then the shift operation is performed to drive out the stored data in the serial fashion. The converse operation of loading serially and then reading out all the pits in the parallel form can be performed by the serial shift register if the individual FF outputs are available. Normally the universal shift registers have provisions for entering data serially and also parallely and then shifting them to the right or to the left. The left-shift shift-register will not be described here.

10.3 Counters

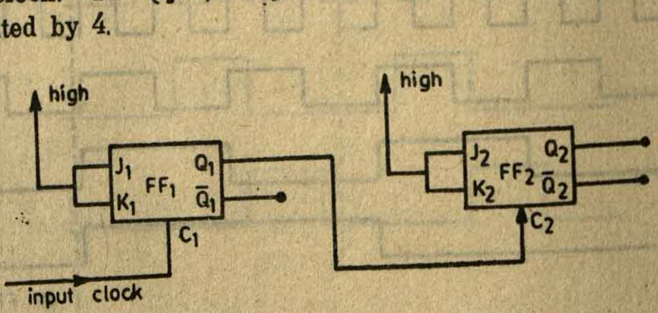
In digital systems possibly the most widely used block is a counter. The counter, as the name suggests, counts the number of discrete events and with the

~~help of proper~~ decoder and display unit indicates the count. If clock pulses of known frequency are counted then the counter can measure time and, thus, can be used to measure frequency and time period. A counter uses flip-flops interconnected in such a fashion that for every cycle of the input waveform the state of the flip-flops advances by one step. Since a flip-flop has two states, an array of N flip-flops will have 2^N states. However, after starting from an initial state of the FFs the counter may return to the same state after K input pulses where $K \leqslant 2^N$. Such a counter is known as base-K counter or modulo-K counter. Counters may be made to count to any base desired as long as the number N of FF is such as to have $K \leqslant 2^N$.

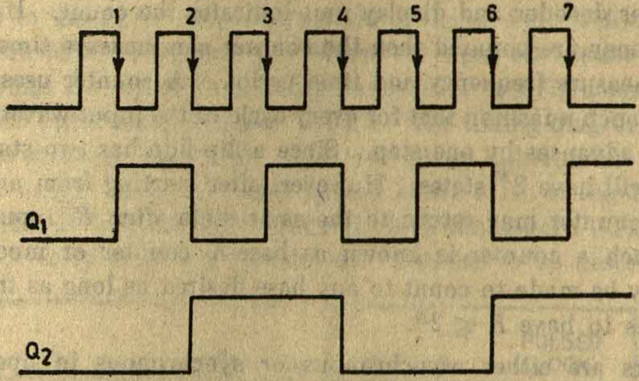
Counters are either asynchronous or synchronous in operation. In the asynchronous counter, also called the ripple counter, the common clock is not applied to all the flip-flops. In contrast, the synchronous counter works with a common clock to all the flip-flops. Such a connection is necessary when we want a high speed counter. We shall describe here a ripple counter of 4 and 16, followed by a counter of 3 and 5 and finally a decade counter (count of 10). We shall also briefly describe a synchronous counter.

10.3.1 COUNT OF 4 AND 16 COUNTERS

An asynchronous or ripple counter consisting of 2 flip-flops is shown in Fig. 10.13 (a). The JK inputs of both the FFs are returned to High thus ensuring that the flip-flop will toggle every time the clock input of the FF changes from 1 to 0. The clock of the second FF is connected to the Q_1. Let us assume that the FFs have been reset so that the initial state of the counter is 00. When the input clock transition takes place,the FF1 will toggle. The timing waveforms are shown in Fig. 10.13 (b). Q_1 changes state from 0 to 1 and $Q2$ will remain undisturbed. At the second clock transition FF1 will toggle again and Q_1 will go to 0. Thus, the clock of FF2 will make a negative transition and it will toggle making $Q_2 = 1$. Third clock will toggle the FF1 only and the fourth clock will toggle FF1 and FF2 both as shown. We obtain one pulse for every four pulses of the input clock. The Q_2 is, thus, a divide by 4 output and the counter is said to have counted by 4.



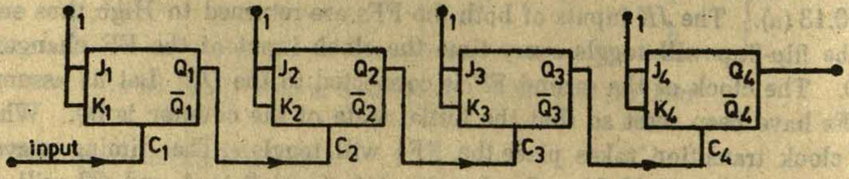
(a) Block diagram



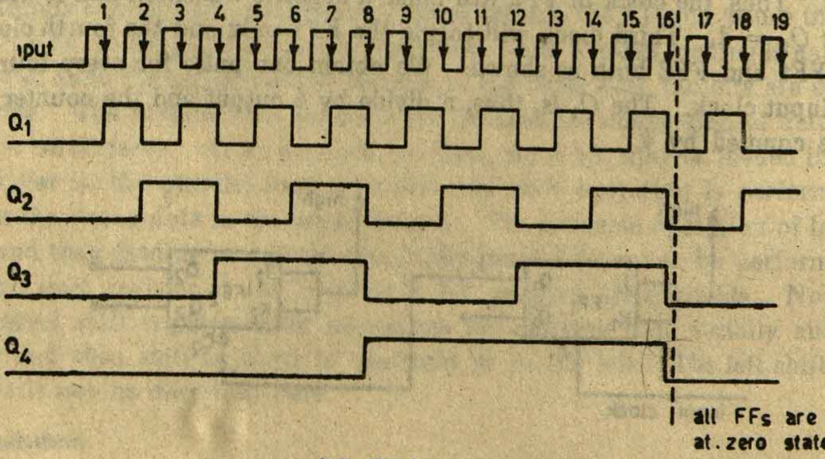
(b) Timing waveform

Fig. 10.13 Count of 4 Ripple counter

The module-4 counter described above can be simply extended to a modulo-16 counter shown in Fig. 10.14 (a). The timing waveform is shown in Fig. 10.14 (b). We shall assume that the initial state of the counter consisting of 4 FFs is 0000.



(a) Block diagram



(b) Timing waveform

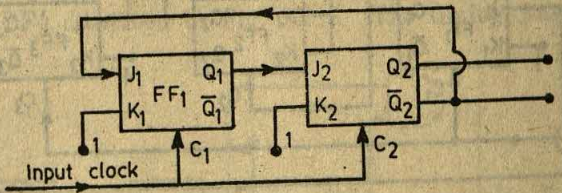
Fig. 10.14 Modulo-16 Counter

The count proceeds after the clock pulses are applied at the input. At the end of 16 pulses, the counter state is again 0000. We see that each FF is a count of 2 circuit and 4 such circuits are in series to give a count of 16. We shall next describe mod-3 and mod-5 counters before taking up the special case of modulo-10 counter.

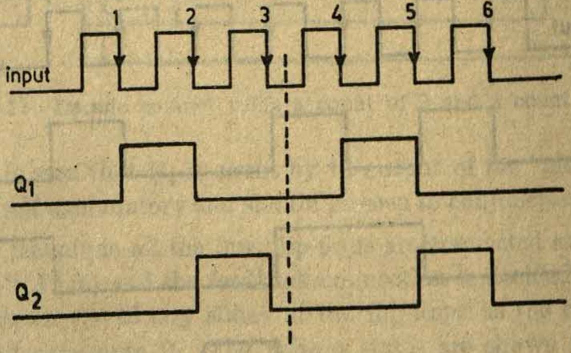
10.3.2 MODULO-3 AND 5 COUNTERS

There are many methods of making a modulo-3 or 5 counter. We shall first describe here the modulo-3 counter whose block diagram is shown in Fig. 10.15 (a). The $\overline{Q}_2$ is connected back to J_1 and Q_1 is connected to J_2 in the two flip-flop-circuit shown.

Let us assume that the state of the FFs is 00. Since $\overline{Q}_2 = 1 = J_1$ the FF_1 will toggle at 1st clock pulse transition. Now since $Q_1 = J_2 = 1$, both the FF1 and FF2 will toggle at the second clock pulse. The FF2 will toggle again at the instant of the 3rd clock pulse. The FFs are again 00 at the end of the three clock pulses



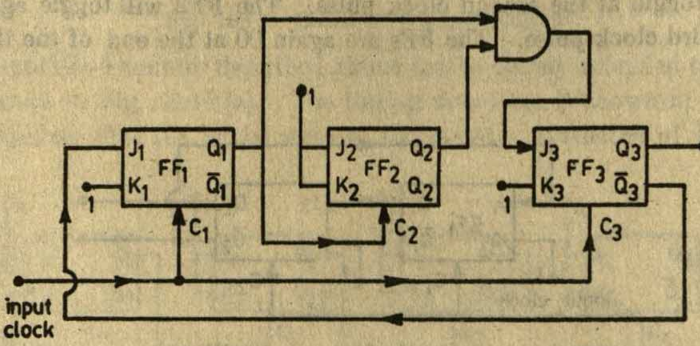
(a) Block diagram



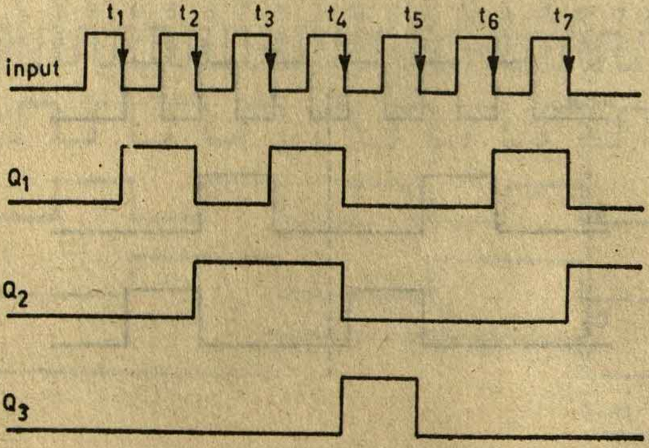
(b) Timing waveform

Fig. 10.15 Module-3 Counter

The module-5 counter shown in Fig. 10.16 (a) is slightly more complicated, Since a decade counter normally uses a count of 2 and a count of 5, modulo-5 counter is widely used. The two flip-flops FF1 and FF2 are clocked directly by the input clock and the clock of FF2 is connected to the Q_1. J_3 is connected to the AND output of Q_1 and Q_2. Every time Q_1 changes from 1 to 0 the FF2 will toggle. Let us assume that Q_1, Q_2 and Q_3 are in the state 000. Referring to Fig. 10.16 (b) at clock t_1 FF1 will toggle because $\overline{Q}_3 = J_1 = 1$. At clock t_2 both FF1 and FF2 will toggle making $Q_1 = 0$ and $Q_2 = 1$. At clock t_3, FF1 will once again toggle and $Q_1 = 1$ but Q_2 and Q_3 are unaffected. At the next clock FF2 and FF1 will toggle again making $Q_1 = Q_2 = 0$. Since prior to the triggering instant we had $Q_1 = Q_2 = 1$. we will get $J_3 = 1$ and hence at clock t_4 FF3 will also toggle making $Q_3 = 1$. Hence $\overline{Q}_3 = 0 = J_1$. At clock t_5



(a) Block diagram



(b) Timing waveform

Fig. 10.16 Module-5 counter

we will have $J_3 = 0$ and the FF3 will change state to $Q_3 = 0$, since $J_3 = 0$, $K_3 = 1$ and FF1 and FF2 unchanged with $Q_1 = Q_2 = 0$. Thus at the end of the 5th clock transition the state of the FF will be 000, the starting state. The output of Q_3 will be a count or divide by 5 of the input clock waveform.

10.3.3 DECADE COUNTER

A counter which counts to the base of 10 is known as a decade counter. Such counters are extremely useful because they help us count in the decimal system. A decoder at the output of this counter indicates the count in the usual decimal number system. The number of flip-flops required in this counter will be 4 since $2^4 > 10$. Many techniques have been used to terminate the count at the end of the 10th pulse in a usual binary counter in order to make it a decade counter. We shall describe here two methods of making a decade counter. In one technique the mod-2 counter in series with a mod-5 counter is used to produce a mod-10 counter. In the other technique a 4 stage binary counter is modified by using feed-back to get a mod-10 counter.

The block diagram of a decade counter is shown in Fig. 10.17. The FF1 is the mod-2 counter whose output is connected to the mod-5 counter consisting of FF2, FF3 and FF4 described in Fig. 10.16. The timing waveform is shown in Fig. 10.18. It is seen that Q_4 is count by 10 output of the "clock" input. The timing diagram is self explanatory and should be seen in conjunction with Fig. 10.16.

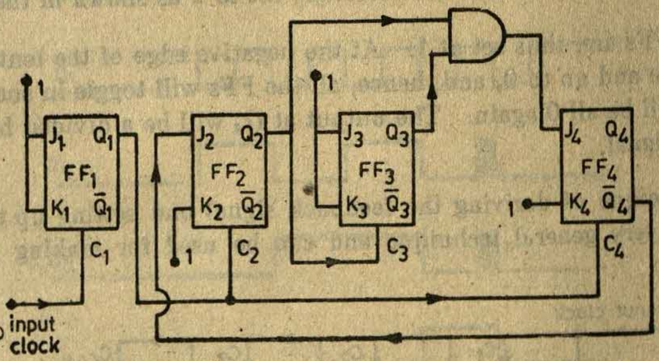


Fig. 10.17 Decade counter using a count of 2 and a count of 5

In the other technique all the four flip-flops are connected as a ripple counter as shown in Fig. 10.19 (a) and the feedback connection is decided in the following way. We write down the binary states of the flip-flops as the count starts from the state 0000 and goes upto 9. The various states are shown in Fig. 10.19 (b). We look at the state of the counter after the 9th pulse and connect the output of all the flip-flops whose Q is 1 to a NAND gate. We also connect the input clock to this NAND gate. The output of the NAND gate is connected to the 'preset' of all the flip-flops whose Q was 0. All the FFs are Master-Slave JK and they

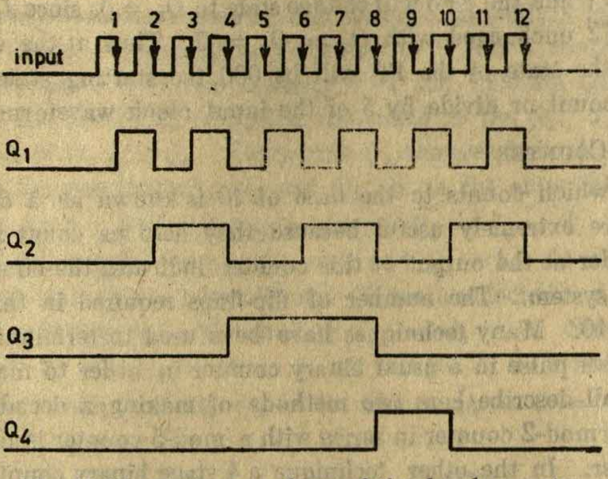
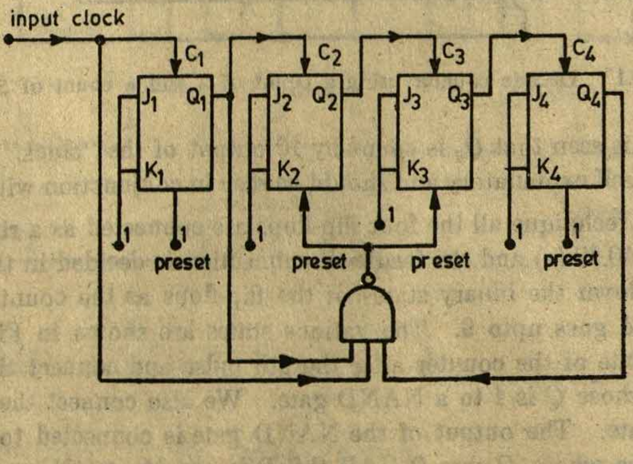


Fig. 10.18 Timing waveform of the decade counter

toggle at the negative edge of the clock pulse. Immediately at the end of the 9th pulse when the clock goes high again, all the three inputs of the NAND gate are 1. The timing diagram is shown in Fig. 10.20. The presets of the FF2 and FF3 go to 0 and these two FFs are forcefully set to 1 as shown in the diagram.

All the FFs are, thus set at 1. At the negative edge of the tenth pulse, the FF1 will toggle and go to 0, and, hence, all the FFs will toggle in succession and output gate will be all 0 again. The output at Q_4 will be a divided by 10 output of the clock signal.

The technique of deriving the feedback signal and setting up the required flip-flops is a very general technique and can be used for making any mod-K



(a) Block diagram

state	Q_4	Q_3	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

(b) Decade counter

Fig. 10.19 Decade Counter

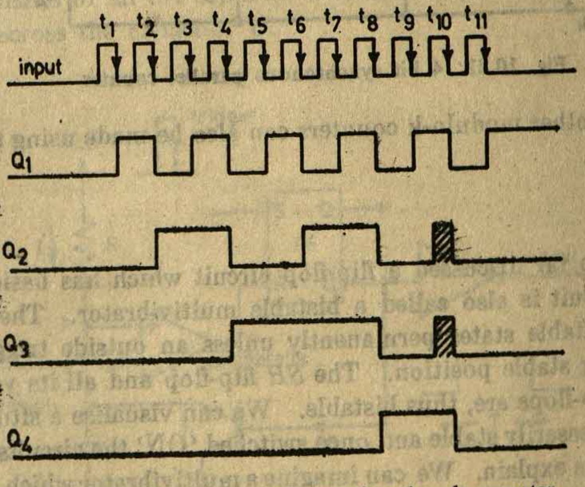


Fig. 10.20 Timing waveform of a decade counter

counter. We must ensure that $2^N > K$ where N is the number of flip-flops required. The feedback is decided by looking at the $(K-1)$ state of the counter.

10.3.4 SYNCHRONOUS COUNTERS

A synchronous counter is an arrangement of flip-flops and gates connected in such a way that all the flip-flops are clocked simultaneously. Such a procedure eliminates the cumulative delays produced in the ripple counters and allows the counters to work at higher speed. The circuit arrangement of a synchronous counter is more complex. We shall describe here one synchronous parallel binary counter briefly.

A four stage binary counter is shown in Fig. 10.21. Instead of the output of one stage rippling through the succeeding stages as in Fig. 10.14 (a), the output of a FF is applied to the input of all succeeding stages. The clocks are all common. The timing waveform will be the same as that of the counter in Fig. 10.14 (b). FF1 will toggle at each clock pulse. The AND gates are only enabled when the Q_1, Q_1Q_2, or $Q_1Q_2Q_3$ are high. Whenever that happens the next FF will toggle at the clock transition.

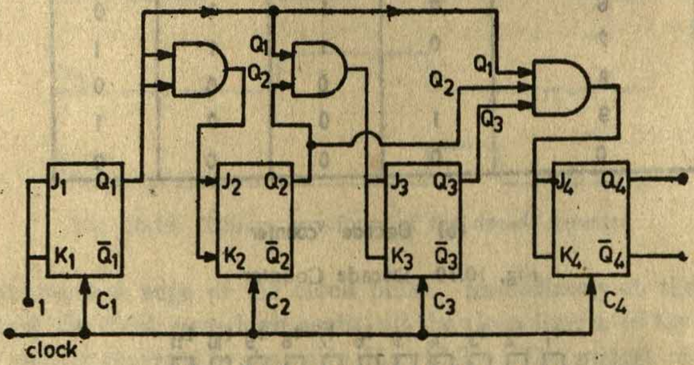


Fig. 10.21 4 bit synchronous parallel counter

Decade or other modulo-k counters can also be made using the synchronous parallel counters.

10.4 Timers

We have so far discussed a flip-flop circuit which has basically two stable states. This circuit is also called a bistable multivibrator. The circuit remains in either of its stable states permanently unless an outside trigger changes its state to the other stable position. The *SR* flip-flop and all its variations of *JK*, trigger and D flip-flops are, thus bistable. We can visualise a situation where the states are not necessarily stable and once switched 'ON' the circuits' states are time dependent. Let us explain. We can imagine a multivibrator which, when triggered, goes to a quasi-stable state and comes back to the original stable state after some time but on its own accord. The time for which the circuit stays in the quasi-stable state can be controlled but the system will inevitably return back to the stable position without any outside help. The circuit has, thus, only one stable position and is called the Monostable multivibrator. It could also happen that the circuit has no stable states but only two quasi-stable states. The circuit cannot remain in any of the states for ever and switches back and forth between the two states. Such a circuit is known as the Astable multivibrator.

Since the operation of both monostable and astable multivibrators are time dependent they have been grouped under the title of timers here. The monostable multivibrator has been given different names because of its action. For instance, the circuit returns back to its original state after a certain time T, and therefore it is called a 'one shot' multivibrator. Since for the time T, it also generates a rectangular pulse of the same duration, it is called the 'gating' circuit. The gate time can be controlled by changing the passive component values. Similarly it is also called a 'delay' circuit because it generates a fast trigger pulse at the output, T seconds after the input trigger. The astable multivibrator on the other hand generates a square wave at its output and behaves like an oscillator. The astable multivibrator does not require any trigger input for its operation. The frequency of oscillation of this multivibrator can again be changed by adjusting voltage or passive component values like R and C.

10.4.1 MONOSTABLE MULTIVIBRATOR

The monostable multivibrator has two states of which one is stable and the other is quasi-stable. When a trigger is applied to the input, the circuit switches to the quasi-stable state and remains there for a time duration of T seconds. It then switches back to the original stable state on its own without any external trigger. A simplified block diagram of a monostable multivibrator is shown in Fig. 10.22. It consists of an SR flip-flop, a comparator, an RC charging circuit and a switch T_1 across the capacitor C.

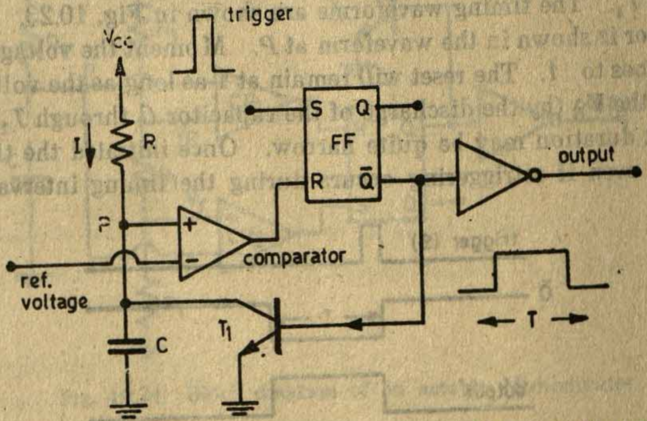


Fig. 10.22 Schematic diagram of a monostable multivibrator

A comparator is a device which provides a fixed d-c voltage, say, V_o if the input signal is larger than a reference voltage V_R. If the input is smaller than the reference voltage, then the output of the comparator is the other fixed level, say, zero volts. Thus, if $V_{in} \geqslant V_R$ then the output is V_o and if $V_{in} < V_R$ then the output is zero. The output voltages of the comparator may be any two fixed *d-c* voltages, though the assumption of V_o and 0 volts is simpler. Since the comparators are very often used with logical gates and flip-flops, the levels of 5 and 0 volts are used in TTL circuits.

Coming back to the circuit of Fig. 10.22 the stable state of the circuit is $Q = 0$ and $\bar{Q} = 1$. Since $\bar{Q}$ is connected to the base of the transistor switch, the transtor T_1 conducts and is in saturation. The collector voltage of T_1 is thus fixed to about 0.2 to 0.3V. The entire current I will therefore flow through R and the transistor. The capacitor is virtually short circuited. One end of the comparator is connected to this junction. Certain *d-c* reference voltage is connected to the other input of the comparator. This reference voltage is the voltage V_R we described above. Hence, only when the input P exceeds V_R, will the output of the comparator be high. The positive and negative signs at the input of the comparator indicate that when the voltage at the positive lead is higher than that at the negative lead, the output of the comparator is high or 5V. It is otherwise low or 0 volts. Since both $S = R = 0$ the state of the flip-flop remains unchanged.

Now, when the trigger signal is applied, the S input goes to 1 ($R = 0$) and the FF is set $Q = 1$, $\bar{Q} = 0$. Moment $\bar{Q}$ goes to zero, the transistor T_1 becomes open circuit and the capacitor starts charging to V_{CC} through the resistance R. The charging of the capacitor is thus exponential with a time constant of RC. The voltage at P starts rising and after a certain time T it will exceed the reference voltage (V_R). The comparator will switch to High and $R = 1$ ($S = 0$). The flip-flop will reset again to $\bar{Q} = 1$, $Q = 0$. The capacitor discharges through the transistor T_1. The timing waveforms are shown in Fig. 10.23. The charging of the capacitor is shown in the waveform at P. Moment the voltage at P crosses V_R the reset goes to 1. The reset will remain at 1 as long as the voltage at P does not go below the V_R (by the discharge of the capacitor C through T_1). The width t_d of the reset duration may be quite narrow. Once initiated the timing interval will complete even if retriggering occurs during the timing interval.

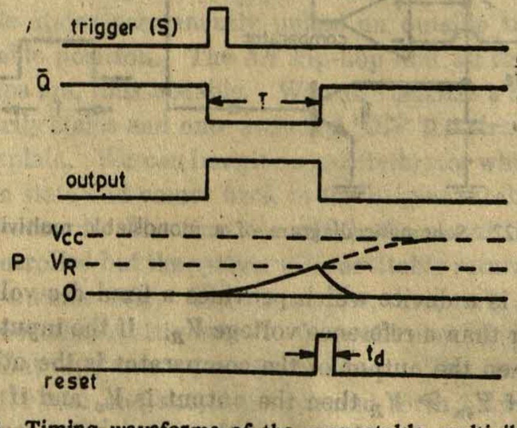


Fig. 10.23 Timing waveforms of the monostable multivibrator

In an actual circuit using NE 555 timer, the reference voltage is also derived from the V_{CC} and is set at $\frac{2}{3}V_{CC}$. There is a comparator in the trigger circuit also and the *d-c* voltage or the reference voltage for that comparator is $V_{CC}/3$ Since the charging circuit voltage and the reference voltages are both derived from V_{CC}, the timing interval generated is independent of the V_{CC} voltage variations. The pulse width T is normally given by $T = 1.1\ RC$. Applying a negative going trigger to the trigger terminals initiates the process.

10.4.2 ASTABLE MULTIVIBRATOR

An astable multivibrator does not have any of its states stable. Both states are quasi-stable and the circuit oscillates between the states without any trigger from outside. A timer circuit which will produce astable operation is shown in Fig. 10.2.4 There are two reference voltages V_R and $V_{Trigger}$ ($= V_T$) and two comparators CP1 and CP2. Three resistances each of value R_1 are connected across V_{CC} and provide the V_R and V_T voltages. Obviously $V_R = 2V_{CC}/3$ and

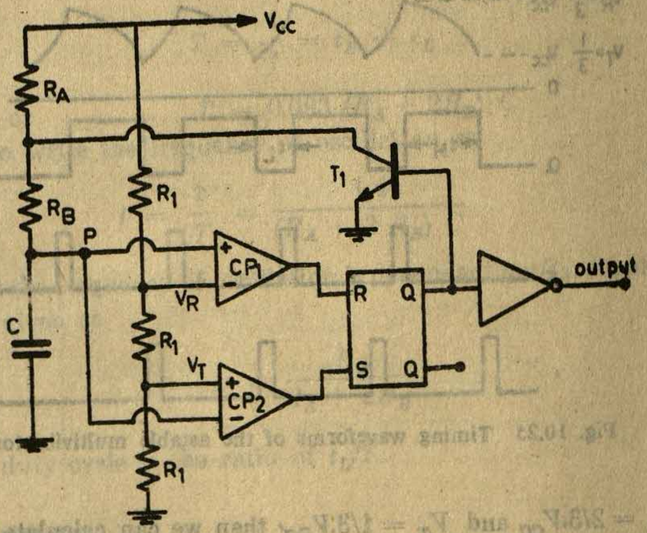


Fig. 10.24 Block diagram of an astable Multivibrator

$V_T = V_{CC}/3$ Two resistances R_A and R_B are used in series to charge the capacitor C from V_{CC}, and R_B is used for discharging C through the transistor switch T_1.

Let us see how the astable multivibrator made from this timer circuit operates. Let us assume, rather randomly, that $Q = 0$ and $\overline{Q} = 1$. The switch T_1 will be a short circuit and the current will only flow through R_A. If the capacitor was uncharged, the voltage at P will be small or zero. $CP2$ will have its positive input higher than the negative input and, therefore, the output will be high making S

high. This in turn will set the FF and $Q = 1$, $\overline{Q} = 0$. Once $\overline{Q} = 0$, T_1 will open and the capacitor C will charge through $R_A + R_B$. When the voltage at P crosses V_T we will have $CP2$ going low and hence $S = 0$. Since R is also 0 the FF will remain in its previous state of $Q = 1$; $\overline{Q} = 0$. C continues charging and as soon as the voltage at P exceeds V_R we will have $CP1$ going high. This will make $R = 1$, $S = 0$ and FF will reset to $Q = 0$, $\overline{Q} = 1$. T_1 again closes and the capacitor starts discharging through R_B and T_1. $CP1$ immediately goes low maintaining $S = 0$, $R = 0$. Once the capacitor has discharged to V_T the comparator $CP2$ will go high making $S = 1$ and setting the FF to $Q = 1$, $\overline{Q} = 0$ The waveform is shown in Fig. 10.25. The output alternately goes high and low. The capacitor charges and discharges between V_R and V_T, the two reference voltages derived from V_{CC}. Steady state conditions only are shown in the figure.

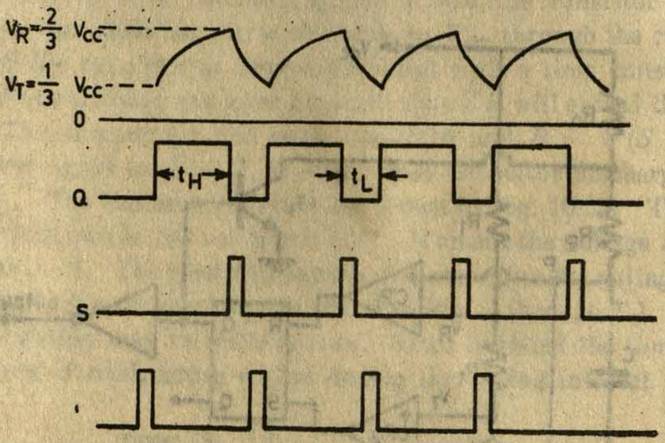


Fig. 10.25 Timing waveforms of the astable multivibrator

If $V_R = 2/3.V_{CC}$ and $V_T = 1/3.V_{CC}$, then we can calculate the time it will take the capacitor to charge from V_T to V_R. The time constant is $(R_A + R_B)\,C$ and the final voltage to which the capacitor is charging is V_{CC}. Thus at t_1 the voltage across the capacitor is $V_T = 1/3.V_{CC}$ and

$$\frac{1}{3} \cdot V_{CC} = V_{CC}\,(1 - \exp[-t_1/(R_A + R_B)\,C]$$

At $t = t_2$ the voltage reaches V_R and hence

$$\frac{2}{3}\,V_{CC} = V_{CC}\,(1 - \exp[-t_2/(R_A + R_B)\,C]$$

Solving $$\exp\left[\frac{-t_1}{(R_A+R_B)\,C}\right]=\frac{2}{3}$$

and $$\exp\left[\frac{-t_2}{(R_A+R_B)\,C}\right]=\frac{1}{3}$$

The time for which the output remains high is called t_H and hence taking natural log of both sides and subtracting we get

$$t_2 - t_1 = t_H = 0.693\,(R_A+R_B)\,C \tag{10.4.1}$$

Similarly the time the output is at the low value is called t_L and can be similarly calculated.

Thus $$t_L = 0.693\,R_B.\,C \tag{10.4.2}$$

The period of oscillation is given as the sum of t_H and t_L. Therefore

$$T = \frac{1}{f} = t_H + t_L$$

or $$T = 0.693\,(R_A + 2R_B)\,C \tag{10.4.3}$$

We can also write the frequency of oscillation as

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \tag{10.4.4}$$

We see that the frequency of oscillation is dependent on R_A, R_B and C. The duty cycle D is given as

$$D = \frac{R_B}{R_A + 2R_B} \tag{10.4.5}$$

where the duty cycle is the ratio of t_L/T.

Review Questions

10.1 What is the essential difference between the SR flip-flop using NAND and NOR gates? How is the truth table made universal? Give the truth table.

10.2 Why do we require a narrow trigger pulse to trigger the SR flip-flop?

10.3 What is a JK FF? What is its truth table?

10.4 What is the necessity for the Master-Slave technique of flip-flops?

10.5 Why is the negative edge triggered system preferred?

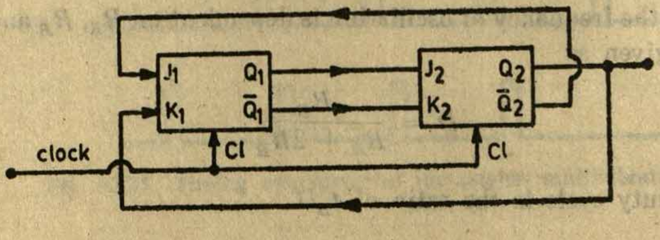
10.6 What is the difference between synchronous and asynchronous operation of a Master-slave JK FF?

10.7 What for is the asynchronous operation used?

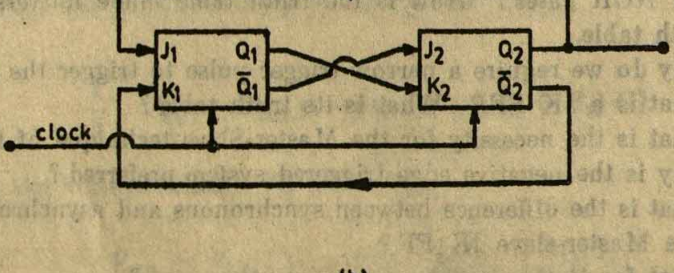
10.8 What is a D FF ?
10.9 How is the serial shift register loaded ?
10.10 How is the parallel shift register loaded ?
10.11 Distinguish between a ripple counter and a synchronous counter.
10.12 How do you divide an input signal frequency by ten ?
10.13 What are astable and monostable multivibrators ?
10.14 Can a timer NE 555 generate square wave of 1 KHz frequency ?
10.15 What is a comparator ?
10.16 Can a pulse be delayed by an arbitrary amount by a one-shot multivibrator ?

Problems

P 10.1 Draw the circuit diagram of a JK FF using NOR gates only.
P 10.2 Draw the circuit diagram of a JK Master-slave FF using (i) NAND gates and (ii) NOR gates only.
P 10.3 If the propagation delay in each gate of the flip-flops is 5 nsecs, calculate the propagation delay of the Master-Slave JK FF of Fig. 10.8.
P 10.4 In a eight bit serial shift register, the sixth bit from the left has been entered wrongly. Can this bit be corrected ? Explain how.
P 10.5 Two JK flip-flops can be connected in various configurations as shown in Fig. P 10. 1. Draw the output waveforms in each case.



(a)



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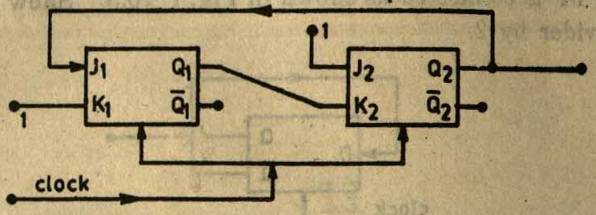
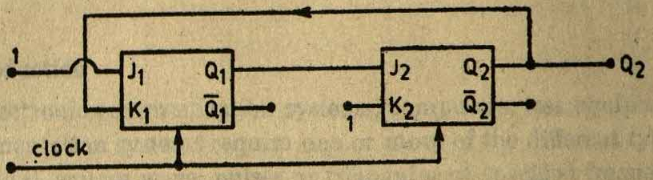


(c)



(d)

Fig. P 10.1

P 10.6 Draw the circuit of a divide by 5 counter using the feedback principle ?

P 10.7 Draw the circuit of a divide by 7 counter using a 4 bit counter and feedback.

P 10.8 What is the waveform at the output in Fig. P 10. 2

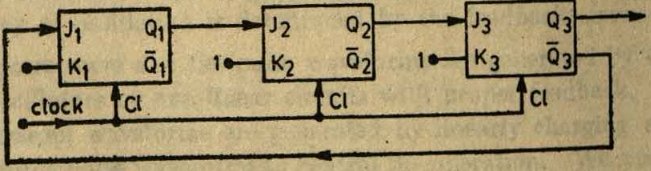


Fig. P 10.2

P 10.9 In the circuit diagram of Fig. 10.22, it is given that $V_{CC} = 12$ V, $R = 10\,\text{K}\Omega$, $C = 0.001\ \mu F$, $V_R = 5$ V. A trigger signal is applied at $t = 0$, find the width T of the gate signal generated.
(hint : $V_R = V_{CC}\ [1 - e^{-T/RC}]$)

P 10.10 An NE 555 timer is connected as shown in Fig. 10.24. The value of C is 0.01 μF, $V_{CC} = 15$ V. Fix suitable values of R_A and R_B to generate a square wave signal of 1 KHz frequency.

P 10.11 A D FF is connected as shown in Fig. P 10.3. Show that it will act as a divider by 2.

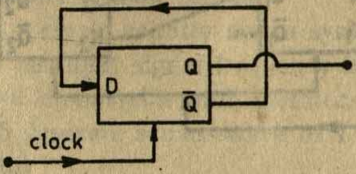


Fig. P 10.3

11

Waveform Generators

11.0 Introduction

All electronic communication systems, computers, test equipments and industrial instrumentation systems require one or more of the different type of waveforms viz. sinoisoidal, square wave, pulses or triangular of specified frequency and amplitude. These signals are generated by electronic circuits known as oscillators and waveform generators. We shall study the generation of such signals in this chapter. The sinusoidal oscillators may be classified into two broad categories of two terminal and four terminal oscillators. The two terminal oscillators, also known as negative resistance oscillators, consist of primarily a two terminal device that has a negative real component of its impedance or admittance in a portion of its operating characteristics and a frequency selective network. Four terminal oscillators also known as feedback oscillators consist of an amplifier and a frequency selective four-terminal passive feedback network through which a portion of the amplifier output is fed back to the input in proper phase and magnitude to ensure oscillation. The frequency of oscillation is determined by the feedback network.

The square wave and the pulse waveforms are generated by what are called relaxation oscillators or non-linear circuits with proper feedback. The triangular and ramp (sweep) waveforms are generated by linearly charging and discharging a capacitor using pulse waveforms to control the operation. We shall describe here some representative circuits of the relaxation oscillators.

11.1 Sinusoidal Oscillators

Other than producing a sinusoidal signal of a given frequency and output voltage or power, the oscillator must generate only a very small amount of harmonic voltages and must have a good frequency and amplitude stability. The frequency of oscillation may vary because the parameters of the resonant as well as the active circuit depends upon the load, mechanical arrangement and temperature etc. Low harmonic content in the output can only be obtained if the amplitude of oscillation is kept as small as possible. Elaborate arrangements have to be made to make amplitude and frequency of an oscillator stable and of low harmonic content. We shall first take up the feedback oscillator circuits and establish a criterion of oscillation.

Let us assume that the output of an amplifier is coupled back to its input through a four-terminal frequency determining network. Various oscillators differ in the type of feedback network that they have and the details of the amplifier. For example, some feedback networks produce a 180° degree phase shift between its input and output voltages at a particular frequency. Such oscillators require an amplifier to produce a phase shift of 180° in order that the feedback signal is in the same phase as the input to the amplifier. Other feedback networks produce a zero phase shift at a particular frequency and therefore, require an amplifier that produces no phase shift between its input and output.

11.1.1 Criterion of Oscillation

We briefly touched upon the subject of the criteria of stability of the feedback amplifiers in Chapter 7. Similar approach can be used to analyse the oscillator circuits where the elements of the circuit are so chosen that the system is unstable. Thus, for a feedback circuit shown in Fig. 7.1, eqn. (7.5)

$$A_f(s) = \frac{A(s)}{1 - A(s).\ f(s)} \tag{11.1}$$

or

$$A_f(s) = \frac{A(s)}{1 + T(s)} = \frac{A(s)}{F(s)} \tag{11.2}$$

where $T(s) = -A(s).f(s)$

and $F(s) = 1 + T(s)$

Putting $s = j\omega$ in eq. (11.1), we see that when

$$(1 - A(j\omega).\ f(j\omega)) > +1$$

the gain with feedback is less than that without feedback and the circuit is a negative feedback amplifier. Whereas, if

$$0 < (1 - A(j\omega).\ f(j\omega)) < +1.$$

the gain with feedback is larger than that without feedback. Such a situation is known as positive feedback. Where $(1 - A(j\omega)\ .\ f(j\omega)) \leqslant 0$, the system becomes unstable. In this system, as soon the d.c. supply is switched on, any noise excitation is amplified and applied back to the input in such a phase that the effective input further increases and the amplitude at the output goes on building up. The amplitude of the output is eventually limited by the nonlinearity of the active device. The feedback network is frequency selective and hence a certain frequency is only fedback in the process. Thus an output is produced without feeding any input signal from the outside. Such a system is called an oscillator.

If we confine our attention to the case where $(1-A(j\omega).\,f(j\omega))=0$,

$$\text{or} \quad A(j\omega).\,f(j\omega)=1 \qquad (11.3)$$

then we get a positive feedback with unity loop transmission. The condition of eq. (11.3) is also called the Berkhausen criterion of oscillation.

Normally in eq. (11.3) the quantity $[A(j\omega).\,f(j\omega)]$ is complex and the criterion of oscillation requires that

$$|\,A\,(j\omega).\,f(j\omega)\,|=1 \qquad 11.4(a)$$

$$\text{and phase of } (A\,(j\omega).\,f(j\omega))=0 \qquad 11.4(b)$$

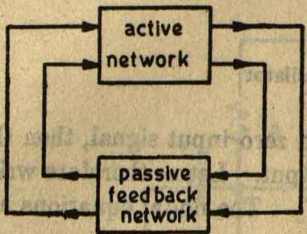
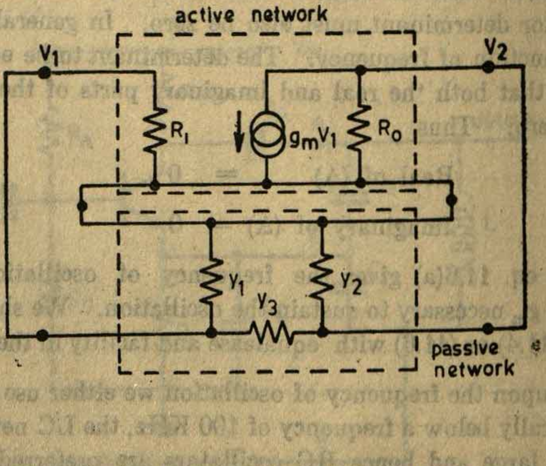
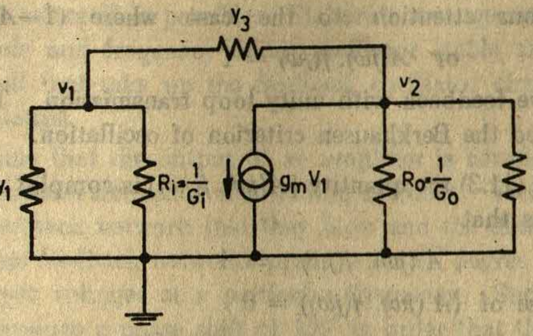


Fig. 11.1 Generalized form of feedback oscillator

A generalised feedback oscillator circuit is shown in Fig. 11.1 where the active network or amplifier may be a transistor or a tube or an operational amplifier. The passive feedback network and the active network are joined in parallel at their input and output terminals. Replacing the active and the passive networks with their equivalent circuits, we have in Fig. 11.2(a), the overall equivalent circuit of the oscillator. The passive network is represented by a π network. The element values are expressed in terms of admittances y_1, y_2 and y_3 to facilitate having any R, L or C components in the network. The active network has been assumed to be unilateral with no internal feedback of its own. The circuit is rearranged and shown in Fig. 11.2(b). We could find the conditions of oscillation using the technique described in eq. 11.4. However an alternative method is sometimes simpler to use and is described next.



(a) Active and passive network



(b) Rearranged circuit

Fig. 11.2 Equivalent circuit of oscillator

If an oscillator is thought of as an amplifier with zero input signal, then the gain of the amplifier must be infinite to produce any output. Let us therefore write the KVL for the circuit of Fig. 11.2(b) and solve for V_2. The nodal equations are

$$0 = (Y_1 + Y_3 + G_i)\, V_1 - Y_3 V_2$$

and

$$0 = (g_m - Y_3)\, V_1 + (Y_2 + Y_3 + G_o)\, V_2$$

Therefore

$$V_2 = \frac{\begin{vmatrix} (Y_1 + Y_3 + G_i) & 0 \\ (g_m - Y_3) & 0 \end{vmatrix}}{\Delta} \qquad (11.5)$$

where

$$\Delta = \begin{vmatrix} (Y_1 + Y_3 + G_i) & -Y_3 \\ (g_m - Y_3) & (Y_2 + Y_3 + G_o) \end{vmatrix}$$

From eq. (11.5) we see that the numerator is zero and, therefore, for any non-zero V_2 the denominator determinant must also be zero. In general the value of Δ is complex and a function of frequency. The determinant to be equal to zero would therefore require that both the real and imaginary parts of the determinant must individually be zero. Thus

$$\text{Real of } (\Delta) = 0 \qquad 11.6(a)$$

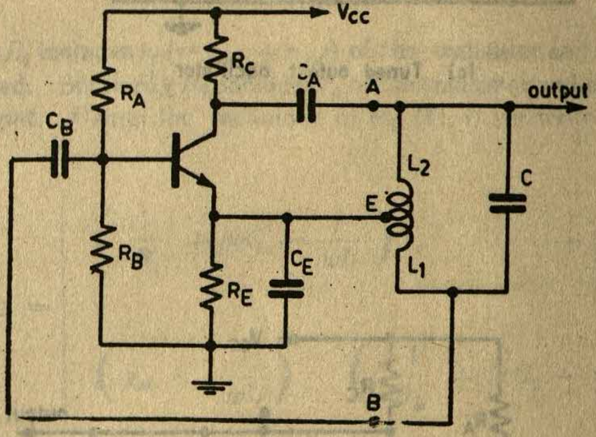
$$\text{Imaginary of } (\Delta) = 0 \qquad 11.6(b)$$

The condition of eq. 11.6(a) gives the frequency of oscillation and eq.11.6(b) gives the value of g_m necessary to sustain the oscillation. We shall apply either the condition of eq. (11.4) or (11.6) with equalease and facility in the analysis to follow.

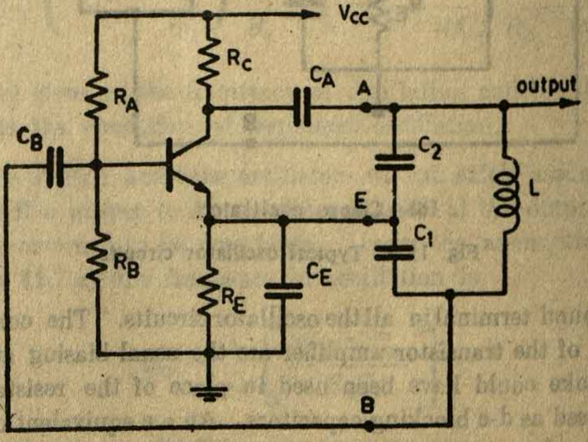
Depending upon the frequency of oscillation we either use LC or RC passive networks. Generally below a frequency of 100 KHz, the LC networks become too cumbersome and large and hence RC oscillators are preferred. Over 100 KHz, on the other hand, LC oscillators are quite convenient and easy to build. There are many types of LC and RC oscillators but we shall describe only one or two typical oscillators in each category.

11.1.2 LC Oscillators

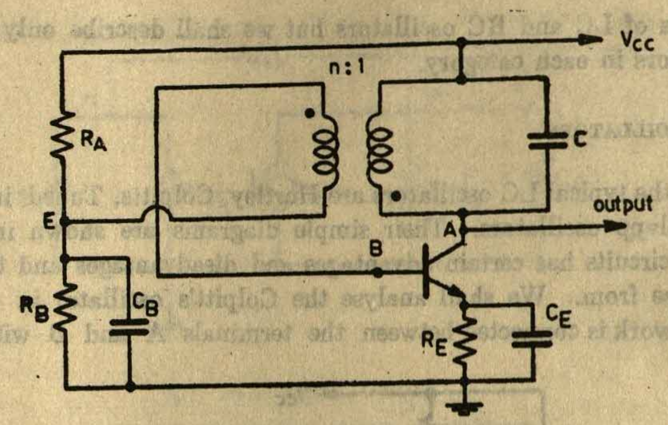
Some of the typical LC oscillators are Hartley, Colpitts, Tuned input, Tuned output, and Clapp oscillators. Their simple diagrams are shown in Fig. 11.3. Each of these circuits has certain advantages and disadvantages and the user has many to choose from. We shall analyse the Colpitt's oscillator in detail. The passive LC network is connected between the terminals A and B with E as the



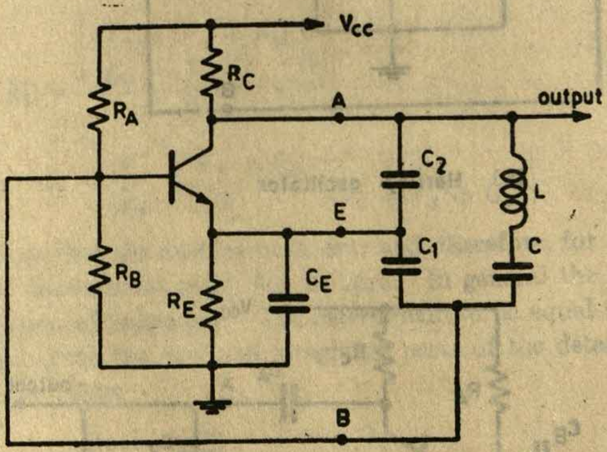
(a) Hartley oscillator



(b) Colpitts oscillator



(c) Tuned output oscillator



(d) Clapp oscillator

Fig. 11.3 Typical oscillator circuits

common or ground terminal in all the oscillator circuits. The components R_C, R_E, C_E, R_A, R_B etc. of the transistor amplifier are the usual biasing and by-pass components. A choke could have been used in place of the resistance R_C. C_A and C_B have been used as d-c blocking capacitors. An a.c equivalent circuit of the Colpitts oscillator is shown in Fig. 11.4.

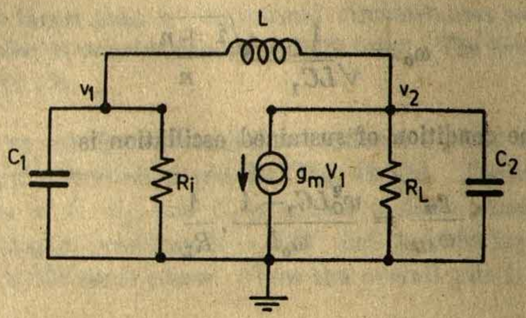


Fig. 11.4 Equivalent circuit of a Colpitts oscillator

The resistance R_i includes r_i ($= r_{bb'} + r_{b'e'}$) of the transistor and any biasing resistances connected. Similarily R_L includes r_o of the transistor and any load resistance across the output. Using the technique of eq. (11.6) we write the circuit determinant as

$$\Delta = \begin{vmatrix} \left(\frac{1}{R_i} + jwC_1 - \frac{j}{wL} \right) & + \frac{j}{wL} \\ \left(g_m + \frac{j}{wL} \right) & \left(\frac{1}{R_L} + jwC_2 - \frac{j}{w_L} \right) \end{vmatrix}$$

$$\text{Real } (\Delta) = \frac{1}{R_i \cdot R_L} - w^2 C_1 C_2 + \frac{C_1}{L} + \frac{C_2}{L} = 0 \qquad 11.7(a)$$

$$\text{and Imag } (\Delta) = \left(wC_2 - \frac{1}{w_L} \right) \frac{1}{R_i} + \left(wC_1 - \frac{1}{wL} \right) \frac{1}{R_L} - \frac{g_m}{wL} = 0 \qquad 11.7(b)$$

Equation 11.7(a) gives w_o the frequency of oscillation and for this frequency the eq. 11.7(b) gives the condition of sustained oscillation.

In the case of FET and tube oscillators we can safely assume that R_i is very large. Further if a proper buffer amplifier is used at the output of the oscillator then R_L can be assumed to be very large. Under the assumption that R_i is very large, from eq. 11.7(a), the frequency of oscillation is

$$w_0^2 = \frac{1}{L} \left[\frac{C_1 + C_2}{C_1 C_2} \right] \qquad (11.8)$$

Letting $C_2 = n\,C_1$, the eq. (11.8) can be rewritten as

$$\omega_o = \frac{1}{\sqrt{LC_1}} \cdot \sqrt{\frac{1+n}{n}} \tag{11.9}$$

From eq. 11.7(b), the condition of sustained oscillation is

$$\frac{g_m}{\omega_{oL}} = \frac{w_0^2 LC_1 - 1}{\omega_o L} \cdot \frac{1}{R_L}$$

solving

$$g_m R_L \geqslant w_0^2 \, LC_1 - 1$$

Substituting for w_o

$$g_m R_L \geqslant 1/n \tag{11.10}$$

$$\text{or} \qquad g_m R_L \geqslant \frac{C_1}{C_2}$$

In most of the transistor circuits R_t is quite small and eq. (11.8) and (11.10) are not valid. From eq. 11.7(a), if it is desired that the frequency of osillation is independent of the active circuit parameters then

$$\frac{C_1}{L}(1+n) \geqslant \frac{1}{R_t R_L} \tag{11.11}$$

giving
$$w_0^2 = \frac{1}{LC_1} \cdot \left(\frac{1+n}{n}\right) \tag{11.12}$$

as before.

Assuming that the condition of eq. (11.11) is satisfied, the condition of sustained oscillation is obtained from eq. 11.7(b) as

$$g_m \geqslant \frac{n}{R_t} + \frac{1}{nR_L} \tag{11.13}$$

In a transistor circuit, for the purpose of simplification, let R_L be very large and $R_t \simeq \beta r_e$. Then eq. (11.13) gives the condition of sustained oscillation as

$$g_m \cdot \beta \, r_e \geqslant \frac{C_2}{C_1}$$

$$\text{or} \quad \beta \geqslant \frac{C_2}{C_1} \tag{11.14}$$

Thus β should be larger than n. In normal circumstances we should include the effect of loading also in considering eq. (11.13),fully. The frequency of oscillation is given by eq. (11.12).

To sum up we see that the amplifier produces a phase shift of 180° between its input and output terminals A and B of Fig. 11.3(b). The frequency determining network consisting of L, C_1, and C_2 produces a sharp phase change around w_0. At w_0 the phase change produced is — 180° and thus the input and the output of the amplifier are in the same phase. Since the overall gain is more than unity the circuit oscillates.

So far we have assumed the coil to be lossless. However, if the coil is assumed to have a small resistance R in series with the inductor to account for the loss, then Q the quality factor of the coil, is defined as $Q = \omega.L/R$. The frequency of oscillation and the condition of oscillation are modified accordingly. For the transistor oscillators we obtain the condition that if

$$(1+n)\frac{C_1}{L} \geqslant \frac{1}{R_tR_L} + \frac{C_1R}{L}\left(\frac{1}{R_L}+\frac{n}{R_t}\right) \tag{11.15}$$

then $$w_0^2 \approx \frac{1}{LC_1}\left(\frac{1+n}{n}\right) \quad \text{as before}$$

and $$g_m \geqslant \left(\frac{1}{nR_L}+\frac{n}{R_t}\right) + \left(\omega_0^2 nC_1 - \frac{1}{R_tR_L}\right)R \tag{11.16}$$

is the requirement of sustained oscillations.

Example 11.1

In a Colpitts oscillator using a transistor (Fig. 11.3(b)) it is given that $I_C = 5mA$, $R_C = 1K\Omega$, $R_A \| R_B = 1.5K\Omega$. If $n = 1$ and $L = 10mH$ calculate the value of C_1 necessary for an oscillator to work at 1 MHz. Check whether the necessary condition of oscillation is satisfied if $Q = 50$.
The transistor parameters are $r_{bb'} = 50\,\Omega$; $\beta = 100$
$f_T = 250\ MHz$, $C_{b'c} = 3pfP$.

Since $n = 1$, from eq. (11.15) and (11.16)

$$w_0^2 = \frac{2}{LC}$$

Hence $$C = .005\ \mu\text{F}.$$

Now
$$g_m \geqslant \frac{1}{R_i} + \frac{1}{R_L} + \omega_0^2\, C^2 R - \frac{R}{R_i R_L} \qquad (11.17)$$

Now
$$R = \frac{\omega_0 L}{Q} = \frac{2}{Q\omega_0 C}$$

Therefore
$$R = \frac{2\pi \times 1 \times 10^6 \times 10 \times 10^{-6}}{50} \simeq 1.256\ \Omega$$

Also
$$R_i = (r_{bb'} + r_{b'e}) \parallel (R_A \parallel R_B)$$

Since
$$r_{b'e} = 100 \times 5\ \Omega$$
$$R_i = (50 + 500) \parallel (1.5\ \text{K}\,\Omega)$$
$$= 402\ \Omega \simeq 400\ \Omega$$

Since $R_L = 1\text{K}\Omega$ we can neglect the term $R/R_i R_L$ as very small, The condition of oscillation is obtained as (substituting for R in the equation 11.17)

$$g_m \geqslant \frac{1}{R_i} + \frac{1}{R_L} + \frac{2w_o C}{Q}$$

or
$$C \leqslant \left[g_m - \frac{1}{R_i} - \frac{1}{R_L} \right] \cdot \frac{Q_o}{2w_o} \qquad (11.18)$$

Putting in the values

$$C \leqslant \left[200 \times 10^{-3} - \frac{1}{402} - \frac{1}{1000} \right] \cdot \frac{50}{2\pi \times 10^{+6} \times 2}$$

or $C \leqslant 0.796 \times 10^{-6}$ Farads

Since C is only 0.005 μF the condition of sustained oscillation is satisfied. Also from eq. (11.15) we see that the assumption is valid since

$$\frac{2 \times 5 \times 10^{-9}}{10 \times 10^{-6}} >> \frac{1}{0.400 \times 10^{+3} \times 10^{+3}} + \frac{5 \times 10^{-9} \times 1.256}{10 \times 10^{-6}} \left(10^{-3} + \frac{10^{-3}}{0.402} \right)$$

$$\text{or} \quad 10^{-3} >> 4.7 \times 10^{-6}$$
$$\text{or} \quad 1 >> .0047.$$

All along in the derivations of eq. (11.15) and (11.16) or even the earlier equations we have assumed that the transistor or the active device is represented by pure resistance R_i and R_o etc. In practice, at the frequencies of interest of the LC oscillators this assumption is not valid. For instance the effect of the input capacitance of the transistor called here as $C_{in} = [C'_{be} + (1 + g_m R_L)\ C'_{be}]$ can be included in the value of C_1. Thus the actual capacitance included in all calculations is

$$\begin{aligned} C_1\,(\text{effective}) &= C_1 + C_{b'e} + (1 + g_m R_L)\, C_{b'c} \\ &= C_1 + C_{in} \end{aligned} \qquad (11.19)$$

We can calculate

$$C_{b'e} = \frac{g_m}{\omega_T} \approx 127 \text{ pF}$$

$$(1 + g_m R_L)\, C_{b'c} = 603 \text{ pF}$$

$$\text{hence} \quad C_{in} = 730 \text{ pF}$$

Since we have calculated C_1 (effective) = 5000 pF the actual value of $C_1 = 5000 - 730 = 4270$ pF. Thus, finally the values of the passive circuit are

$$\begin{aligned} C_2 &= 5000 \text{ pF} \\ C_1 &= 4270 \text{ pF} \\ L &= 10\ \mu H \\ Q &= 50 \\ \text{for} \quad f_{osc} &= 1 \text{ MHz} \end{aligned}$$

The oscillator is shown in Fig. E 11.1

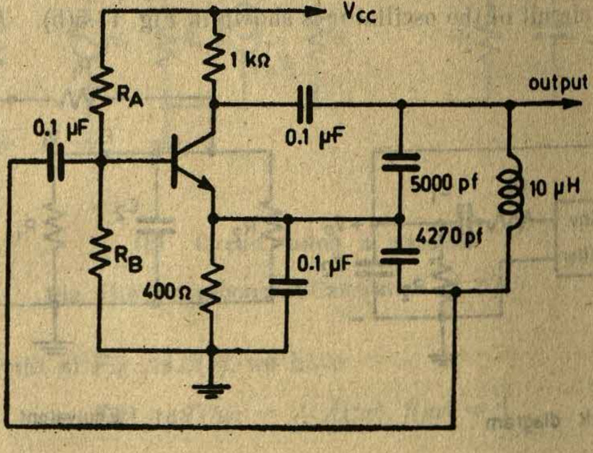


Fig. E11.1 Colpitts oscillator for 1 MHz

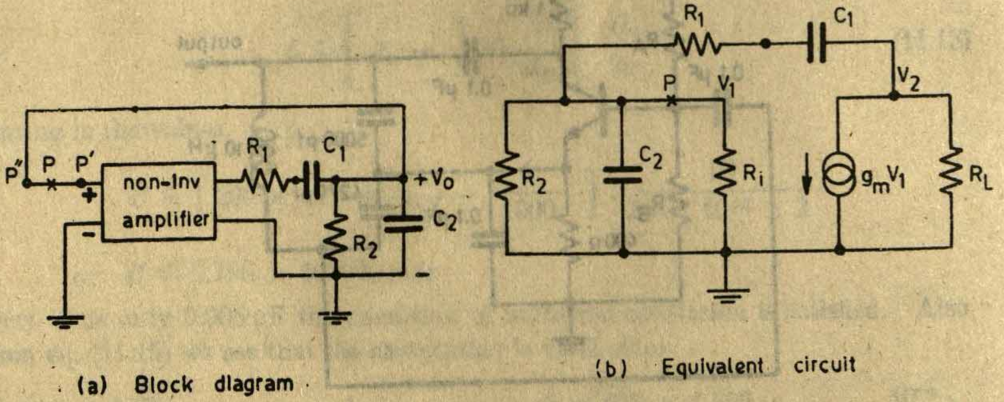
It is sometimes desirable to have n less than one in order to get low distortion in the output waveform. The analysis of Hartley and Tuned output oscillator is rather involved because the expressions are more complex in nature though the technique of analysis is essentially the same. The analysis of Clapp oscillator is very similar to the Colpitts oscillator described above. The choice among the oscillators is governed by many factors. Hartley oscillator is useful at lower frequencies and Colpitts is found to be more suitable at higher frequencies. It is rather difficult to build variable frequency oscillators with a Colpitts circuit because of the requirement of tuning C_2 and C_1 simultaneously. Clapp oscillator gives a good frequency stability against changes in parameters of the active device and the circuit is very convenient to tune

11.1.3 RC OSCILLATORS

In a feedback oscillator, as was mentioned earlier, the overall loop gain $|A(s).f(s)|$ should be unity with zero phase angle. A properly selected RC circuit can produce a zero or 180° phase shift at a given frequency. Provided this phase change with frequency is sharp this RC network can be used in the feedback path of an amplifier to produce an oscillator. The sharpness of the phase-frequency characteristic is being emphasised because then only the frequency of oscillation will be unique and stable. We shall describe here two RC-tuned oscillators called the Wien-bridge oscillator and the RC phase-shift oscillator.

Wien-bridge Oscillator

Wien-bridge oscillator has a number of very desirable features and finds extensive use at frequencies below about 100 KHz. A block diagram of a Wien bridge oscillator is shown in Fig. 11.5(a). It consists of a non-inverting amplifier and a frequency determining network consisting of R_1C_1 in series and R_2C_2 in shunt. An equivalent circuit of the oscillator is shown in Fig. 11.5(b). R_i includes the input resistance and any biasing resistance of the active device used. R_L consists of the output resistance of the device and any load connected to the amplifier.



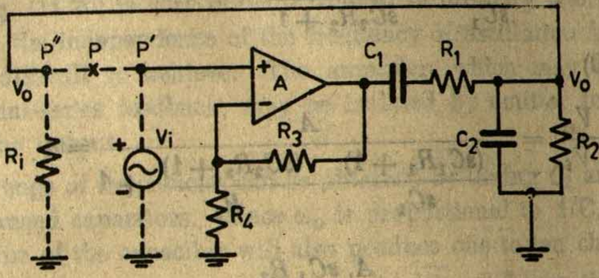
(a) Block diagram

(b) Equivalent circuit

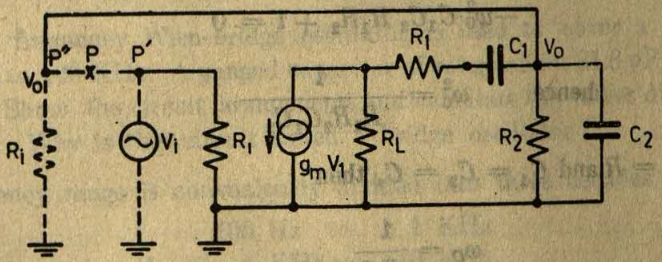
Fig. 11.5 Wien-bridge oscillator

Both the circuits of Fig. 11.5(a) and (b) can be analysed in the same fashion. The circuit of Fig. 11.5(a) represents an oscillator where the amplifier is an op-amp. Here the assumptions that its input impedance is very large and the output impedance is very small are valid. The loop is opened at the point marked P in the diagram. An oscillator or signal generator is connected at P′ and the output is calculated at the point P″. We must connect a proper termination at P″ so that the R_1C_1 R_2C_2 network remains undisturbed. The circuit for the calculation of $T(j\omega)$

is shown in Fig. 11.6(a) for the case of an op-amp and in Fig.11.6(b) for the transistor amplifier. In Fig. 11.6(a) the resistance R_i is infinite.



(a) Circuit using an op-amp



(b) Circuit using a transistor

Fig. 11.6 Measurement/Calculation of T(jw)

Analysing the circuit of Fig. 11.6(a), we have

$$T(s) = T(j\omega) = +A(j\omega).\, f(j\omega) = 1$$

therefore

$$T(j\omega) = \frac{V_o}{V_i} = 1 \tag{11.20}$$

The gain of the amplifier is

$$A = 1 + \frac{R_3}{R_4}$$

Solving the circuit

$$V_o = \frac{AV_i}{R_1 + \frac{1}{sC_1} + \frac{R_2}{sC_2R_2+1}} \times \frac{R_2}{sC_2R_2+1}$$

From eq (11.20)

$$\frac{V_o}{V_i} = \frac{A}{\frac{(sC_1R_1+1)}{sC_1} \cdot \frac{(sC_2R_2+1)}{R_2} + 1} = 1$$

$$\text{or} \qquad \frac{A.\, sC_1R_2}{s^2C_1C_2R_1R_2 + s[C_1(R_1+R_2) + C_2R_2] + 1} = 1$$

$$\text{or} \qquad AsC_1R_2 = s^2C_1C_2R_1R_2 + s(C_1(R_1+R_2) + C_2R_2) + 1$$

Separating the real and imaginary parts, we get

$$-w_0^2\, C_1C_2\, R_1R_2 + 1 = 0$$

$$\text{hence} \qquad \omega_0^2 = \frac{1}{R_1R_2C_1C_2} \tag{11.21}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then

$$\omega_o = \frac{1}{RC} \tag{11.22}$$

Equating the imaginary part

$$AC_1R_2 = C_1(R_1+R_2) + C_2R_2$$

$$\text{or} \qquad ACR = 3\,CR \qquad \text{or} \quad A \geqslant 3 \tag{11.23}$$

Thus the frequency of oscillation is obtained as $1/2\pi\, RC$ and the condition of oscillation is that A should be greater than 3.

The transistor oscillator of Fig. 11.6(b) can be similarly analysed. The frequency of oscillation is obtained as

$$\omega_0^2 = \frac{1}{C^2} \cdot \frac{1}{(R_L+R)} \cdot \left(\frac{1}{R} + \frac{1}{R_i}\right) \tag{11.24}$$

where it is assumed that $R_1 = R_2 = R$ and $C_1 = C_2 = C$

If $R_L \leqslant R$ and $R_i \gg R$: then eq. (11.24) can be simplified to

$$\omega_0^2 = \frac{1}{R^2C^2}$$

which is the same as eq. (11.22). Similarly the condition of oscillation gives that

$$g_m R_L \geqslant 3 \tag{11.25}$$

provided $R_L \leqslant R \leqslant R_i$ (11.26)

The condition of eq. (11.26) is very difficult to meet in ordinary transistor amplifiers and, therefore, the independence of the frequency of oscillation from transistor parameters is difficult to achieve. The amplifier, which may be a CE-CE cascade with a shunt-series feedback, may be isolated by emitter followers both at the input and the output.

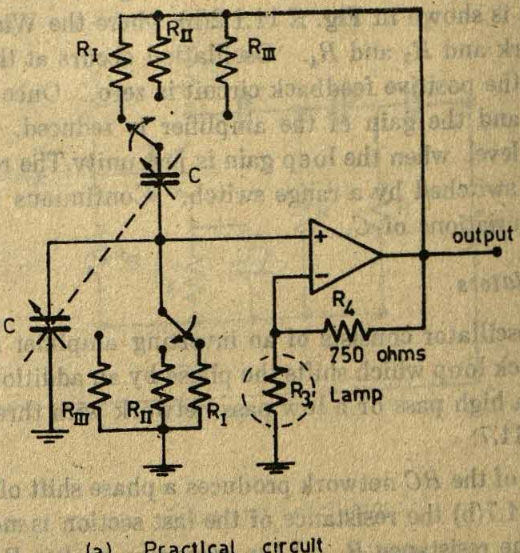
A very wide range of frequencies can be obtained by tuning C_1 and C_2 simultaneously using ganged capacitors. Since ω_0 is proportional to 1/C, a one to ten variation in the value of the capacitor will also produce one to ten change in frequency. In LC oscillators ω_0 is proportional to $1/\sqrt{C}$ and hence the frequency changes by 1 to 3 only for a capacitor change of 1 to 10. A practical Wien-bridge oscillator circuit is shown in Fig. E 11.1.2.

Example 11.1.2

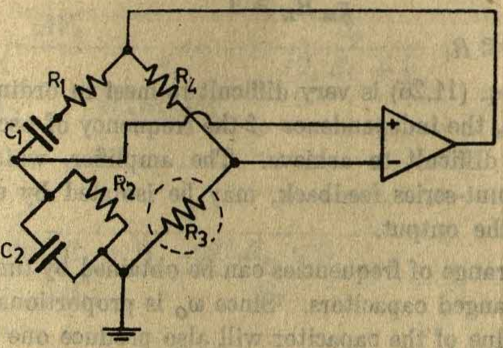
A variable frequency Wien-bridge oscillator is used to cover a frequency range of 100 Hz to 100 KHz. A ganged capacitor of range about 31.8 pF to 318 pF has been used. Show the circuit arangement and calculate the values of the resistances required. Why is this circuit called a bridge oscillator ?

The frequency range is conveniently divided into three decades of

I	100 Hz	to	1 KHz
II	1 KHz	to	10 KHz
III	10 KHz	to	100 KHz



(a) Practical circuit



(b) Bridge configuration

Fig. E11.1.2 Practical Wien-bridge oscillator circuit

The highest frequency of oscillation 100 KHz is obtained with $C = 31.8$ pf. The value of the resistance R in the decade III is

$$R_{III} = \frac{1}{\omega_0 C} = \frac{1}{2\pi \times 100 \times 10^3 \times 31.8 \times 10^{-12}}$$

$$= 50 \text{ Kohms}$$

The values of the resistance in II and I decades are thus 500 Kohm and 5 Mohms. The resistances R_4 and R_3 are used to controlthe gain of the amplifier. Manytimes R_3 is a lamp whose resistance changes as the amplitude of the signal changes across it. To begin with R_3 is small and the gain of the amplifier is large. The bridge circuit idea is shown in Fig. E 11.1.2(b) where the Wien-bridge is formed by R_1C_1, R_2C_2 network and R_3 and R_4. Oscillation occurs at the frequency at which the phase shift of the positive feedback circuit is zero. Once the oscillation builds up, R_3 increases, and the gain of the amplifier is reduced. Oscillation is finally sustained at the level when the loop gain is just unity.The resistance for the three decade ranges are switched by a range switch. Continuous frequency variation is obtained by the variations of C.

Phase Shift Oscillators

Phase shift oscillator consists of an inverting amplifier and an RC ladder network in the feedback loop which shifts the phase by an additional 180°. The ladder network is either a high pass or a low pass network with three or four RC sections as shown in Fig. 11.7.

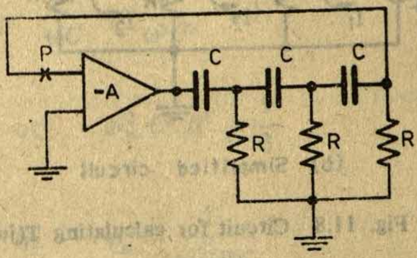
Each section of the RC network produces a phase shift of 60°. In the transistor oscillator of Fig. 11.7(b) the resistance of the last section is modified. A resistance R_1 in series with the resistance R_{in} of the transistor makes $R_1 + R_{in} = R$.

In order to calculate $T(jw)$ in Fig. 11.7(a), we open the loop at the point P and connect a voltage source as shown in Fig. 11.8(a). The circuit is redrawn in Fig. 11.8(b) for convenience. Writing the KVL equations as follows

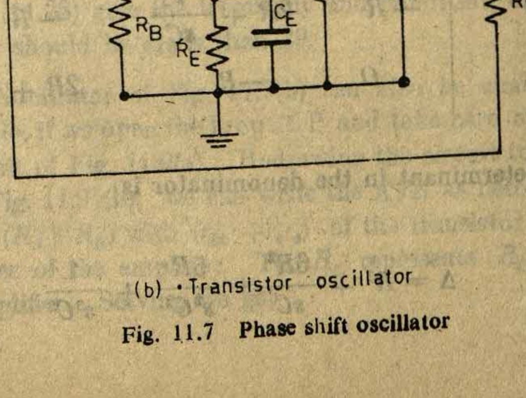
$$-AV_t = \left(R + \frac{1}{sC}\right)(I_1 - I_2)$$

$$O = \left(2R + \frac{1}{sC}\right) I_2 - I_1 R - I_3 R$$

$$O = \left(2R + \frac{1}{sC}\right) I_3 - RI_2$$

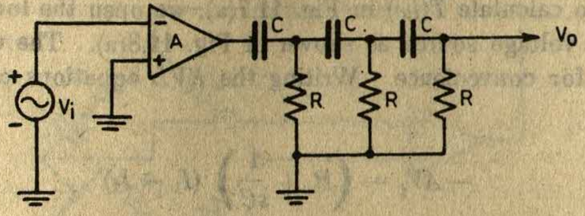


(a) Op - Amp oscillator

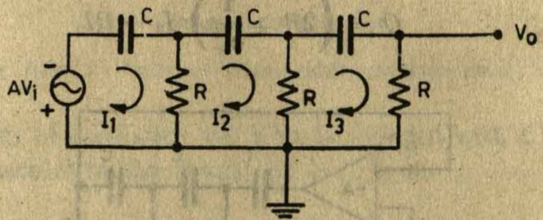


(b) Transistor oscillator

Fig. 11.7 Phase shift oscillator



(a) Complete circuit



(b) Simplified circuit

Fig. 11.8 Circuit for calculating T(jw)

We can obtain I_3 as

$$I_3 = \frac{\begin{vmatrix} R+\dfrac{1}{sC} & -R & -AV_i \\ -R & 2R+\dfrac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} R+\dfrac{1}{sC} & -R & 0 \\ -R & 2R+\dfrac{1}{sC} & -R \\ 0 & -R & 2R+\dfrac{1}{sC} \end{vmatrix}}$$

The value of the determinant in the denominator is

$$\Delta = R^3 + \frac{6R^2}{sC} + \frac{5R}{s^2C^2} + \frac{1}{s^3C^3}$$

and $$I_3 = -\frac{AV_i R^2}{\Delta}$$

Now $$V_0 = R\,I_3\,;\ \text{hence}\ \frac{V_o}{V_i} = \frac{-AR^3}{\Delta}$$

It is required that $V_o/V_i = 1$. Therefore, putting $s = jw$, we get

$$-AR^3 = R^3 - \frac{j6R^2}{\omega C} - \frac{5R}{\omega^2 C^2} + \frac{j}{\omega^3 C^3} \tag{11.26}$$

Separating the real and imaginary parts of eq. (11.26), we get from the imaginary part,

$$-\frac{6R^2}{\omega C} + \frac{1}{\omega^3 C^3} = 0$$

or $$\omega_0^2\, C^2\, R^2 = \frac{1}{6}$$

or $$\omega_o = \frac{1}{\sqrt{6}RC} \tag{11.27}$$

where ω_o is the frequency of oscillation. The real part gives

$$-AR^3 = R^3 - \frac{5R}{\omega^2 C^2}$$

Substituting the value of $\omega^2 C^2 R^2 = 1/6$ we get

$$A \geqslant 29 \tag{11.28}$$

The eq. (11.27) and (11.28) give the frequency and condition of oscillation. The gain of the amplifier should be more than 29.

The transistor oscillator of Fig. 11.7(b) can also be analysed in a similar fashion. For example, if we open the loop at P and take care of the terminaton, we shall get the circuit of Fig. 11.9(a). Redrawing the circuit to suit the convenience of analysis in Fig. 11.9 (b), we can write the *KVL* as before. R_i represents the combination of $(R_A \,||\, R_B)$ with $(r_{bb'} + r_{b'e})$ of the transistor in parallel. This is the input resistance of the amplifier. The R_L represents $R_C \,||\, r_o$ or the load resistance of the amplifier. Solving we get

$$\Delta = \begin{vmatrix} R_L + R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$\text{or,} \quad \Delta = R^3 + 3R^2R_L + \frac{6R^2}{sC} + \frac{4RR_L}{sC} + \frac{5R}{s^2C^2} + \frac{R_L}{s^2C^2} + \frac{1}{s^3C^3}$$

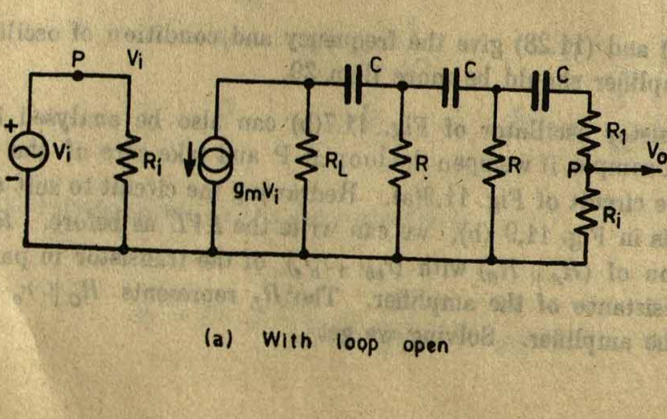
$$V_o = \frac{I_3R_i}{\Delta} = \frac{AR^2R_i}{\Delta} \times V_i$$

Putting $\frac{V_0}{V_i} = 1$ and separating the real and imaginary parts, we get from the imaginary parts

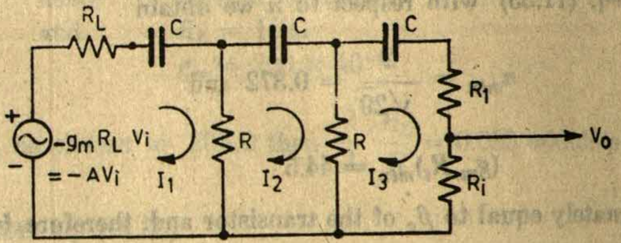
$$-\frac{6R^2}{\omega C} - 4\frac{RR_L}{\omega C} + \frac{1}{\omega^3C^3} = 0$$

or
$$6\omega^2C^2R^2\left(1 + \frac{2}{3} \cdot \frac{R_L}{R}\right) = 1$$

or
$$\omega^2 = \frac{1}{6C^2R^2\left[1 + \frac{2}{3} \times \frac{R_L}{R}\right]} \tag{11.29}$$



(a) With loop open



(b) Circuit redrawn

Fig. 11.9 Equivalent circuit of the transistor Oscillator

To make the frequency of oscillation independent of the transistor parameters it is necessary to have in eq. (11.29)

$$\frac{2}{3} \times \frac{R_L}{R} \leqslant 1$$

Thus, if $R_L \leqslant R$

then $$\omega_0 = \frac{1}{\sqrt{6}\ RC} \quad (11.30$$

From the real part we get

$$- AR^2 R_i = R^3 + 3\, R^2 R_L - \frac{5R}{\omega^2 C^2} - \frac{R_L}{\omega^2 C^2}$$

Simplifying by putting $\omega^2 C^2 R^2 = \dfrac{1}{6\left(1 + \dfrac{2}{3}\dfrac{R_L}{R}\right)}$

$$A = g_m R_L \geqslant 29 \frac{R}{R_t} + 23 \frac{R_L}{R_i} + 4 \frac{R^2{}_L}{RR_i} \quad (11.31)$$

Also $$g_m R_t \geqslant 29 \frac{R}{R_L} + 23 + 4 \frac{R_L}{R} \quad (11.32)$$

Putting $R/R_L = n$, the above equation becomes

$$g_m R_t \geqslant 29n + 23 + \frac{4}{n} \quad (11.33)$$

Minimising the eq. (11.33) with respect to n we obtain

$$n_{min} = \frac{2}{\sqrt{29}} = 0.372 \text{ and}$$

$$(g_m R_t)_{min} = 44.5 \tag{11.34}$$

$g_m R_t$ is approximately equal to β_o of the transistor and, therefore from eq (11.33) and (11.34)

$$\beta_o \geqslant 29n + 23 + \frac{4}{n} \tag{11.35}$$

or
$$\beta_o \geqslant 44.5 \tag{11.36}$$

For good frequency stability $R \gg R_L$ and hence R is also much larger than R_t. Looking into the condition of oscillation of eq. (11.31) and (11.35) we see that this condition will not be met. Both the conditions cannot be satisfied simultaneously in the simple oscillator of Fig. 11.7(b). One method of reducing R_L effectively is to use an emitter follower between the amplifier and the ladder network. The output impedance of the emitter follower will be low and hence the value of R_L and $R \gg R_L$ is satisfied.

Example 11.1.3

A transistor phase shift oscillator is shown in Fig. E. 11.1.3 where $R_A \parallel R_B$ is 2KΩ $I_C = 5\text{mA}$, $\beta = 200$; the frequency of oscillation is 1 KHz. Calculate the values of C, R and R_t such that all the conditions of oscillation are satisfied. Neglect $r_{bb'}$.

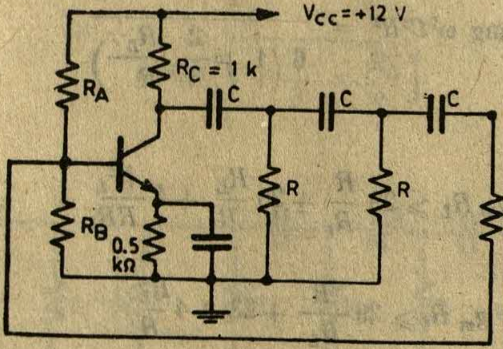


Fig. E 11.1.3 Phase shift oscillator

Now $R_A \parallel R_B = 2K\Omega$

$r_t = 200 \times 5\,\Omega = 1000\Omega$

hence $R_t = 0.667\text{K}\Omega$

and $R_L = 1\text{K}\Omega$

$g_m = 200 \times 10^{-3}$

Let $R \gg R_L$ be chosen as $20\text{K}\Omega$ then $\frac{2}{3}\,\frac{R_L}{R} = 0.033$ which is much smaller than 1. Hence from eq. (11.30)

$$\omega_o = \frac{1}{\sqrt{6}.\,R.C}$$

$$\text{or} \quad C = \frac{1}{\sqrt{6}.\,2\pi \times 10^3 \times 20 \times 10^3}$$

$$\text{or} \quad C = 0.00325\ \mu\text{F}$$

$$R_1 = R - R_t = 20\ \text{K}\Omega - 0.667\ \text{K}\Omega$$

$$= 19.33\ \text{K}\Omega$$

Also $n = R/R_L = 20$

From eq. (11.33)

$$200 \times 10^{-3} \times 0.667 \times 10^{+3} = 29 \times 20 + 23 + \frac{4}{20}$$

We see that this condition is not satisfied.

Let $n = 3.5$ giving $R = 3.5\ \text{K}\Omega$

From eq. (11.31)

$$200 \times 10^{-3} \times 1 \times 10^3 \geqslant 29.\,\frac{3.5}{0.667} + 23\,\frac{1}{0.667} + \frac{4 \times 1}{3.5 \times 667}$$

$$\text{or} \quad 200 \geqslant 188.37$$

which is satisfactory. From eq. (11.30)

$$\omega_o = \frac{1}{\sqrt{6}\,RC\,\sqrt{\left(1 + \frac{2}{3}\,\frac{R_L}{R}\right)}}$$

$$R = 3.5\ \text{K}\Omega$$

$$\text{hence } C = 0.017\ \mu\text{F}$$

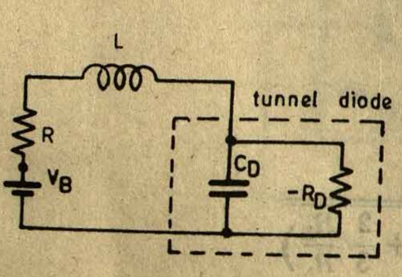
$$\text{and } \quad R_1 = 3.5\,\text{K}\Omega - 0.667\ \text{K}\Omega$$

$$= 2.833\ \text{K}\Omega$$

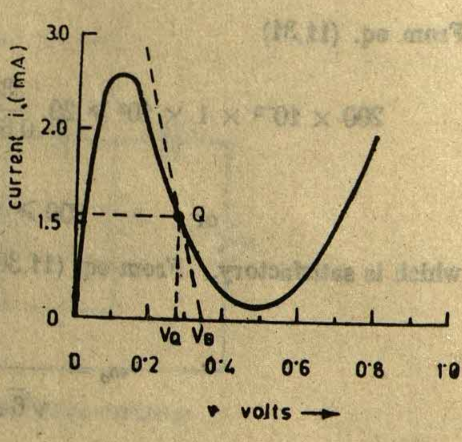
Also from eq. (11.33) $133.4 = g_m R_t \geqslant 125.64$. Of course the condition that $R_L \leqslant R$ is not satisfied and the frequency of oscillation will be somewhat dependent on the transistor parameters.

11.1.4 NEGATIVE RESISTANCE OSCILLATORS

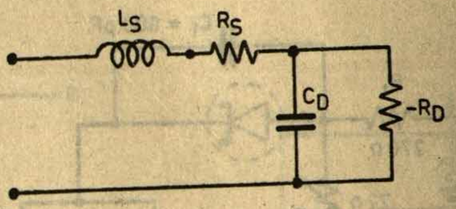
Any one port device that has a negative resistance characteristic over a portion of its operating range may be used as an oscillator. As discussed in chapter 3 the tunnel diode and the UJT exhibit negative resistance over a portion of their V-I characteristics. We have also discussed the characteristics of a tunnel diode in Chapter III. Here the operation of a tunnel diode oscillator will be described briefly. Consider the general circuit of a negative resistance oscillator given in Fig. 11.10(a) along with the V-I characteristic of a tunnel diode in Fig. 11.10(b). As long as the operating point Q is any where between the points X-Y the tunnel diode behaves like a negative resistance. The absolute value of the resistance is given by V_Q/I_Q and is in the range of 100-200Ω. Though actual equivalent circuit is more complex, Fig. 11.10(c), the resistance ($-R_D$) is shunted by a capacitance C_D (depletion region capacitance) which is of the order of few picofarads. V_B is between 100-600 mV. R_S and L_S are the lead resistance and inductance.



(a) General oscillator circuit



(b) v - i characteristic



(c) Equivalent circuit

Fig. 11.10 Tunnel Diode oscillator

The analysis of the oscillator in Fig. 11.10(a) is simple. At the frequency of oscillation the net loop impedance must be zero. Thus

$$R + sL - \frac{R_D}{1 - sC_D R_D} = 0$$

Equating the real and imaginary parts individually to zero, we obtain

$$\omega_0^2 = \frac{1}{LC_D}\left[1 - \frac{R}{R_D}\right] \tag{11.37}$$

and

$$R_D \leqslant \frac{L}{C_D . R} \tag{11.38}$$

It should be remembered that R_D is the magnitude of the negative resistance. As long as R_D is smaller than L/C_DR, any disturbance like noise or closing of a switch will start the oscillation that will grow up in amplitude. The oscillations will be limited by the curvature of the characteristics and at $R_D = L/C_DR$ the amplitude will be constant.

The frequency of oscillation also depends upon R_D as shown in eq. (11.37). The operating point is therefore to be kept in the linear region of the negative resistance to avoid frequency drifts and the amplitude of oscillation limited by some other means. An operating point nearer the point X is preferred. It is only necessary to ensure that $R < |R_D|$. The frequency of oscillation is also affected by the voltage V_B since any change there shifts the operating point and R_D. From all these considerations the circuit of Fig. 11.10(a) is not a very practical circuit.

A typical frequency stable oscillator arrangement is shown in Fig. 11.11 where $f_O = 100$ KHz. L_2C_2 form the tuned circuit. C_1 which includes C_D swamps

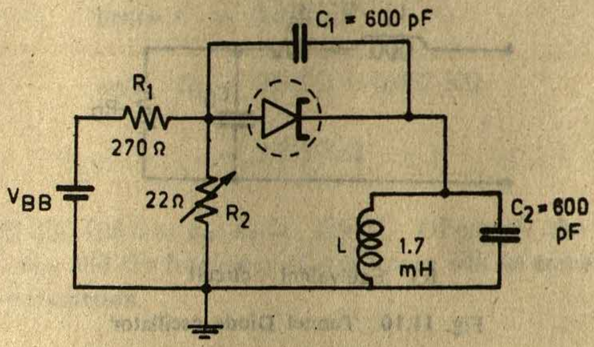


Fig. 11.11 Practical Tunnel Diode Oscillator

any changes of C_D due to bias or temperature changes. The bias is stabilised by using a voltage divider R_1 and R_2. It can be shown that the frequency of oscillation is

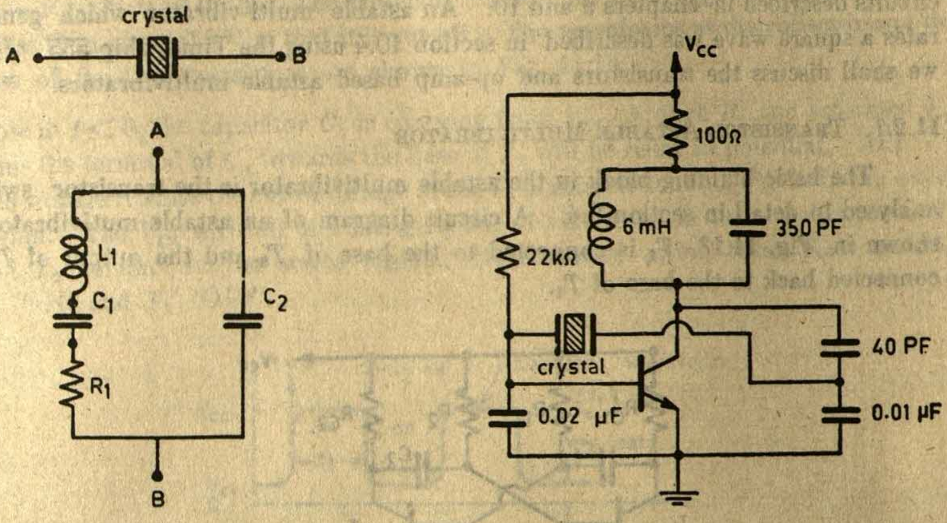
$$\omega_0^2 = \frac{1}{L_2(C_1 + C_2)} - \frac{1}{C_1(C_1 + C_2)\,R_D^2} \tag{11.39}$$

where the lead inductance and resistance have been neglected. One of the main advantages of the tunnel diode oscillator is that it can be used at very high frequencies. For example, if $L_2 = 0.2\ \mu H$ and $C_2 = 3$ pF with $C_1 = 1000$ pF, the frequency of oscillation is 100 MHz.

11.1.5 Crystal Oscillators

Very high frequency stability in oscillators can be obtained by the use of mechanical resonance elements as the frequency determining network. Piezoelectric quartz crystal has been used extensively as one such frequency determining network. The main advantage of the crystal lies in the fact that its effective Q is very high—hundreds of times more than that obtained in ordinary LC circuits. Piezoelectric effect tells us that if the crystal is compressed or stretched in a certain direction, a voltage will appear across the surfaces of the crystal which are perpendicular to the axis of the force applied. Conversely, when a voltage is applied across the surfaces, the crystal expands or contracts. If the applied voltage is alternating, the crystal is set into mechanical vibrations. The amplitude of vibration is maximum if the frequency of the applied voltage corresponds to the mechanical resonance frequency of the crystal. An electrical equivalent circuit of this mechanical resonator, along with its holder, is shown in Fig. 11.12(a). $L_1C_1R_1$ represent the equivalent circuit of the crystal and C_2 is the capacitance of the holder.

The performance of the oscillator will very much depend upon the properties of the crystal, its type, thermal properties and the axis of cut. The frequency of oscillation of some crystals changes with temperature and, therefore, they are kept



(a) Crystal and equivalent circuit (b) Oscillator circuit

Fig. 11.12 Crystal Oscillator

in temperature controlled ovens to improve frequency stability. On the other hand, there are particular cuts of a crystal which have a zero temperature coefficient and are marketed in evacuated glass encolopes. Their stability is adequate for most commercial transmitters and receivers.

A typical oscillator using a crystal is shown in Fig. 11.12(b). The circuit of Fig. 11.12(b) is called a Pierce oscillator. The frequency of oscillation is 100 KHz. The drift is within 10^{-8} Hz per week and the frequency instability is 1.5×10^{-9} per °C.

We have not discussed the amplitude stability and the harmonic content of the various sinusoidal oscillators described. Amplitude of oscillations is normally kept small to ensure low generation of harmonics. The circuit arangements needed to stabilise the amplitude are quite elaborate and beyond the scope of this book. We shall next take up square wave and pulse generators.

11.2 Square Wave Generator

Oscillators discussed so far generate continuous sinusoidal waveform. In all digital systems, and in many analogue systems as well, we require square and pulse waveforms. The main feature of a square wave is that the amplitude level is constant for some period after which it changes abruptly to another level and is constant there. These abrupt changes or switching goes on periodically. Since the square wave signal has two levels only it could be generated using the logic circuits described in chapters 9 and 10. An astable multi-vibrator which generarates a square wave was described in section 10.4 using the Timer chip 555. Here we shall discuss the transistors and op-amp based astable multivibrators.

11.2.1 TRANSISTOR ASTABLE MULTIVIBRATOR

The basic building block in the astable multivibrator is the transistor switch analysed in detail in section 9.4. A circuit diagram of an astable mutivibrator is shown in Fig. 11.13. T_1 is connected to the base of T_2 and the output of T_2 is connected back to the base of T_1.

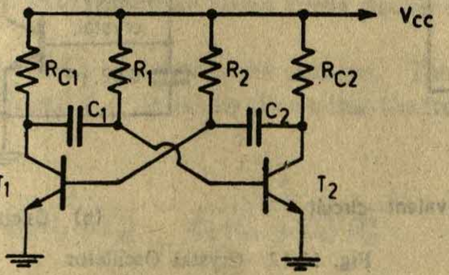


Fig. 11.13 Astable Multivibrator

Assume that the T_1 and T_2 circuits are identical and when the power is switched on both the transistors conduct equally. We shall show that such a situation cannot persist for long. Even if the currents I_{C1} and I_{C2} are identical it will happen that the random noise voltages in both the transistors will be different Thus, it may happen that I_{C1} momentarily increases and the collector voltage V_{C1} reduces momentarily. Since the collector of T_1 is coupled to the base of T_2, this reduction of collector voltage will be transferred to the base of T_2. If the base voltage V_{B2} of T_2 reduces momentarily the current through T_2 will reduce. As the transistors are in the active region they will also amplify any disturbance at the base. Therefore, the reduction of V_{B2} will be amplified by T_2 and the voltage at V_{B1} will rise by a larger amount. Again T_2 is coupled to the base of T_1 and hence V_{B1} will rise resulting in a further increase of the collector current of T_1. The voltage V_{C1} will thus drop by a larger amount because of the regenerative action of T_1 and T_2. We see that a small change is regeneratively coupled back and the voltage V_{C1} falls further. The cycle repeats till T_1 stops conducting and T_2 goes 'ON' or is in saturation. The point to note is that both T_1 and T_2 conducting is not allowed and one of the transistors switches 'off' and the other 'ON' very quickly because of the inevitable minute difference in the circuit voltages or currents.

Having established the fact that both the transistors cannot be conducting simultaneously for long, let us see how the multivibrator operates. Let us assume that immediately before $t = 0$, T_1 is conducting and is 'ON' and T_2 is OFF'. The collector voltage of T_1 will be equal to V_{CE} (Sat) $\approx 0.3\,V$ and the base voltage of

$T_1 = V_{BE}$ (Sat) ≈ 0.7 V. The collector voltage of $T_2 = V_{CC}$ and the base of T_2 is less than about 0.6 V so that it is cut-off. The waveforms at the collector and the base of the two transistors are shown in Fig. 11.14.

Now at $t < 0$, the capacitor C_1 is charging from V_{CC} through R_1 and saturated T_1. Thus the terminal of C_1 towards the base of T_2 will be rising in potential. At $t = 0$ this voltage reaches the cut-in voltage of the T_2 making it conduct and be in the active region. The V_{C2} will fall and bring T_1 out of saturation in turn, making both T_1 and T_2 conduct in the active region. Regenerative action takes place making T_2 'ON' and T_1' 'OFF'.

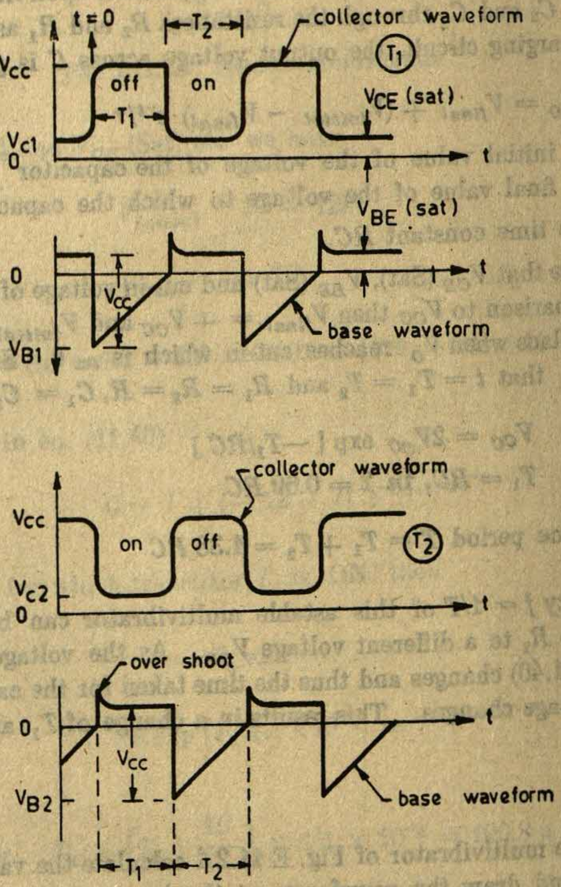


Fig. 11.14 Astable Multivibrator waveform

The collector of T_2 drops suddenly from V_{CC} (the cut-off voltage) to V_{CE} (Sat). This change is coupled to the base of T_1 through the capacitor C_2. The voltage V_{B1} will thus drop by an amount equal to V_{CC}, as shown in Fig. 11.14. At time $t = 0+$ we have $V_{B1} = -(V_{CC} - V_{BE}$ (Sat). C_2 will now start charging to V_{CC}

through R_2 and T_2 in saturation. This charging will be exponential. The initial value of the voltage is $\approx -V_{CC}$ and the final value is $+V_{CC}$. However, as the voltage rises to the cut-in voltage of T_1 it conducts and regenerative cycle repeats. As T_1 goes into saturation, the voltage V_{B2} shows a jump to $-[V_{CC}-V_{BE}$ (sat). The waveform is as shown in Fig. 11.14. C_1 now charges from V_{CC} through R_1 and T_1. If the resistance $R_1 = R_2$ and $C_1 = C_2$ then $T_1 = T_2$.

At the time $t=0+$ when V_{C1} jumps from V_{CE} (Sat) to V_{CC}, the sudden transition is transmitted to the base of T_2 resulting in the overshoot (though small) shown in Fig. 11.14. Similar overshoot is also shown in V_{B1} when T_2 switches from 'ON' to 'OFF'. The time period T_1 and T_2 are dependent upon the rates of charging of the capacitors C_2 and C_1 through the resistances R_2 and R_1 as explained earlier. Now in a RC charging circuit, the output voltage across C is given by

$$V_O = V_{final} + (V_{initial} - V_{final})\, e^{-t/\tau} \tag{11.40}$$

where $V_{initial}$ = initial value of the voltage of the capacitor

V_{final} = final value of the voltage to which the capacitor is charging

and τ is the time constant RC.

If we assume that V_{CE} (Sat), V_{BE} (Sat) and cut-in voltage of the transistor are negligible in comparison to V_{CC} then $V_{final} = +V_{CC}$ and $V_{initial} = -V_{CC}$ and the switching takes place when V_O reaches cut-in which is ≈ 0. Solving eq. (11.40) for the condition that $t = T_1 = T_2$ and $R_1 = R_2 = R$, $C_1 = C_2 = C$ we obtain

$$V_{CC} = 2V_{CC} \exp[-T_1/RC]$$

or

$$T_1 = RC.\ln 2 = 0.69\,RC \tag{11.41}$$

Thus the time period $T = T_1 + T_2 = 1.38\,RC$ (11.42)

The frequency $f = 1/T$ of this astable multivibrator can be changed easily by returning $R_1 = R_2$ to a different voltage V_{BB}. As the voltage V_{BB} is changed, the V_{final} in eq. (11.40) changes and thus the time taken for the capacitor to charge to the cut—in voltage changes. This results in a change of T_1 and T_2 and hence the frequency.

Example 11.2.1

In the astable multivibrator of Fig. E 11.2.1 calculate the values of T_1 and T_2 given $V_{BB} = 7$V and draw the waveforms at the base of the transistors. Let $h_{FE} = 30$;

The collector current of the 'ON' transistor is given as

$$\frac{V_{CC} - V_{CE}\,(\text{Sat})}{R_C} = \frac{(12 - 0.3)\,V}{2.2K} = 5.32\,\text{mA}$$

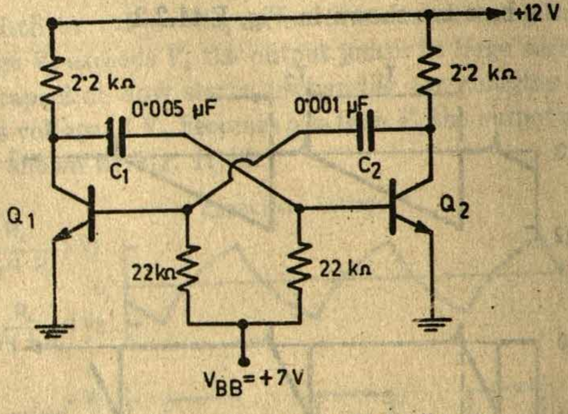


Fig. E11.2.1 Astable Multivibrator

Neglecting V_{BE} (Sat) and V_{CE} (Sat) etc. we have

$$V_{initial} = -12V$$

$$V_{final} = 7V$$

$$\tau_1 = RC = 22 \times 10^3 \times 0.005 \times 10^{-6} = 1.1 \times 10^{-4}$$

Putting the values in eq. (11.40)

$$0 = 7 + (-12 - 7)\ e^{-t/1.1\times10^{-4}}$$

If T_1 is the period for which transistor T_1 is 'ON' then

$$t \to T_1 \text{ and}$$

$$19 \exp [T_1/1.1\times10^{-4}] = 7$$

$$\text{or}\quad T_1 = \left[l_n\ \frac{19}{7}\right] \times 1.1 \times 10^{-4} = 109.8\ \mu \text{ sec}$$

Similarly $\tau_2 = RC = 22 \times 10^3 \times 0.001 \times 10^{-6} = 2.2 \times 10^{-5}$

$$\text{and}\quad T_2 = 2.2 \times 10^{-5}\ l_n \left[\frac{19}{7}\right] = 21.968\ \mu \text{ sec.}$$

The waveforms at the base are shown in Fig. E 11.2.2

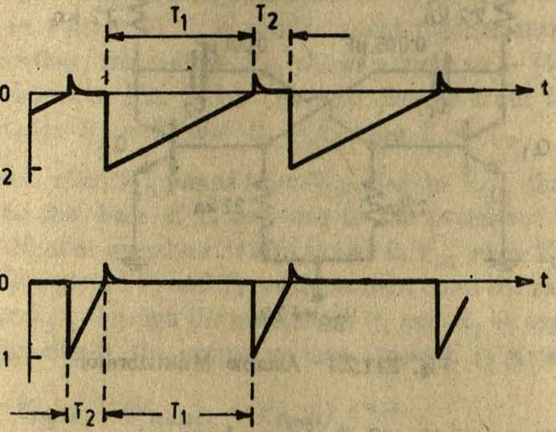


Fig. E11.2.2 Base Waveforms

11.2.2 OP-AMP SQUARE WAVE GENERATOR

So far we have discussed, in this section, square wave generator built around a discrete device like the transistor. Op-Amps can be used to generate square waves by using the positive feedback along with the negative feedback. A square wave generator is shown in Fig. 11.15. In an op-amp if the voltage V_1 is slightly larger (say 1 mV) than V_2, then the output is large negative ($-V_{CC}$). On the otherhand,

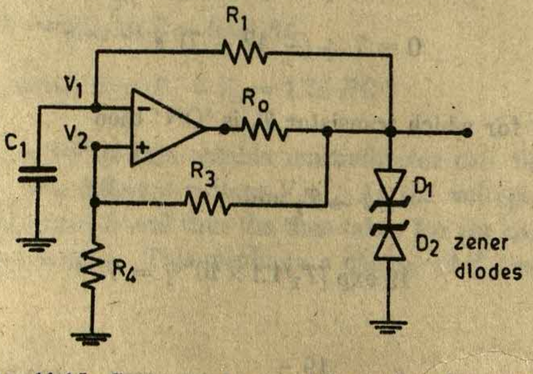


Fig. 11.15 Square wave generation using Op-Amp.

if V_2 is larger than V_1 than the V_{OUT} is large positive ($+V_{CC}$). The Zener diodes D_1 and D_2 in conjunction with R_0 restrict the excursion of the V_{OUT} to $\pm V_Z$, the voltage of the Zener diodes.

Positive feedback is provided through R_3 and R_4. Assuming, to begin with, that the voltage across the capacitor is zero, any noise or disturbance will be amplified. Because of the positive feedback the circuit will amplify regeneratively and the output will switch to $+V_Z$. Capacitor C starts charging to $+V_Z$ through R_1. Once the voltage V_1 exceeds V_2 the output jumps to large negative but is restricted to $-V_Z$. The capacitor now starts discharging (or charging to $-V_Z$) through R_1. Again when the voltage of V_1 becomes less than V_2 the output swings to $+V_Z$. The waveforms are shown in Fig. 11.16.

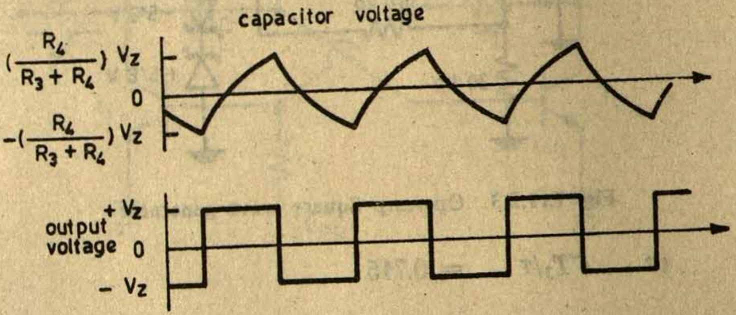


Fig. 11.16 Waveforms at the capacitor and the output

The two threshold voltages at which the op-amp switches are $\pm V_Z \cdot \dfrac{R_4}{R_3+R_4}$.

In other words, when the output is $+V_Z$, the voltage at V_2 is $\dfrac{+V_Z R_4}{R_3+R_4}$.

Similarly when the output is $-V_Z$, the voltage at the positive terminal is $-V_Z \cdot \dfrac{R_4}{R_3+R_4}$. The voltage across the capacitor has to exceed these threshold values for the change of state to occur.

The circuit shown in Fig. 11.15 is fairly convenient to use and works well at frequencies below about 10 KHz. At higher frequencies the delay of the op-amp and its 'slew rate' limit the speed of switching. The Zener diodes of unequal voltages will generate a non-symmetrical wave where T_1 and T_2 will not be equal.

Example 11.2.2

A square wave generator circuit is shown in Fig. E 11.2.3. Calculate its threshold voltages and the times T_1 and T_2.

The threshold voltages at which the op-amp will switch to the other state are

$$\pm \frac{5.6 \times 20}{120} = \pm 0.93\,V$$

Using eq. (11.40), if the initial value is -0.93 and the final value is $+5.6\,V$ and the time constant is τ then the capacitor charges till the voltage reaches $+0.93$. Thus

$$+0.93 = 5.6 + (-0.93-5.6)\, e^{-T_1/\tau}$$

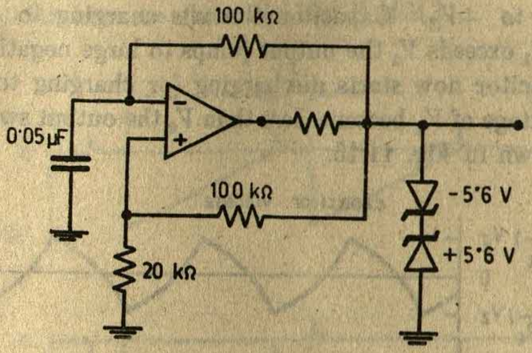


Fig. E11.2.3 Op-Amp Square wave generator

or $e^{-T_1/\tau} = 0.715$

or $T_1 = 100 \times 10^{+3} \times .05 \times 10^{-6}\, 1_n \left(\frac{1}{.715}\right)$

or $T_1 = T_2 = 1.677$ m sec

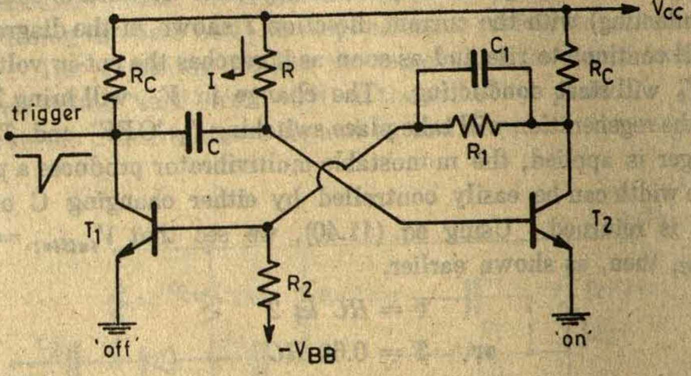
Hence the time period of oscillation is 3.354 msec or the frequency is 298 Hz.

11.3 Pulse Generators

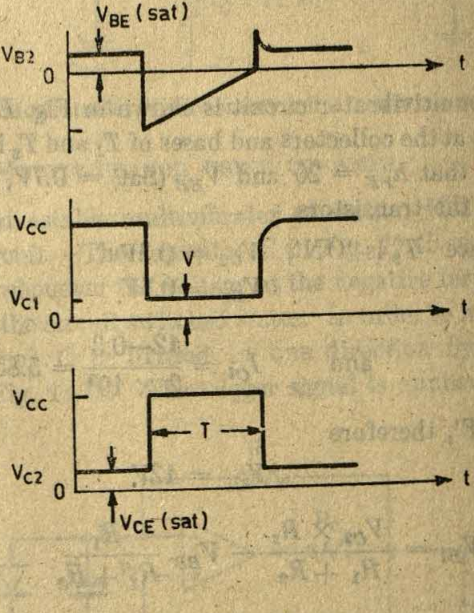
Basically the square wave generator, as the name suggests, generates a waveform which is symmetrical in the sense that the periods T_1 and T_2 are equal. In the circuits for the generation of these waveform it will be quite easy to produce a signal where $T_1 \neq T_2$. Pulse generators consist of circuits which generate narrow pulses whose width can be controlled and whose frequency can be varied. A technique which is quite popular is to generate square waves and then trigger a monostable multivibrator with it to generate variable width narrow pulses. A monostable multivibrator using the timer chip 555 was described in the previous chapter. It this section we shall describe a transistor and an op-amp based monostable multivibrator.

11.3.1 Collector Coupled Transistor Monostable Multivibrator

A monostable multivibrator, as discussed earlier, is a circuit which has only one stable state. If it is triggered to the second state externally then it comes back to the first state after a certain time which can be controlled. A circuit diagram of a monostable multivibrator along with the waveforms at some important places is shown in Fig. 11.17. The collector of T_1 is a.c. coupled to the base of T_2 but the collector of T_2 is d.c. coupled to T_1. This fact makes a great difference between this circuit and previous astable circuit of Fig. 11.13. It can be shown that T_2, 'ON' and T_1 'OFF' is a stable state of operation. Once T_1 is 'OFF' the capacitor C cannot charge through T_1 and base of T_2 is permanently at V_{BE} (Sat). Since T_2 collector is at V_{CE} (Sat), the base of T_1 is negative and thus T_1 is 'OFF' permanantly.



(a) Circuit diagram



(b) Waveforms

Fig. 11.17 Collector coupled Monostable Multivibrator

Now when a negative trigger signal is applied at the collector of T_1 and is of sufficient magnitude it brings T_2 out of saturation and into the active region. V_{C1} rises and T_1 starts conducting. Once both the transistors are in the active region, regenerative action takes place and T_1 is switched 'ON' and T_2 'OFF'. The V_{C1} will drop by an amount almost equal to V_{CC}—actually $I_{C1}.R_C$. Since the voltage across the capacitor cannot change instantaneously, the change of V_{CC} at the collector of T_1 will be transformed to the base of T_2. The base voltage V_{B2} will be $\simeq -V_{CC}$ at $t = 0+$ as shown in Fig. 11.17(b). The capacitor now starts charging through T_1 (now conducting) with the current direction I shown in the diagram. The voltage V_{B2} will continue to rise and as soon as it reaches the cut-in voltage of T_2, the transistor T_2 will start conducting. The change in V_{C2} will bring T_1 out of saturation and the regeneration will take place switching T_1 'OFF' and T_2 'ON'. Thus when a trigger is applied, the monostable multivibrator produces a pulse of width T. The pulse width can be easily controlled by either changing C or the voltage to which R is returned. Using eq. (11.40), we see that $V_{initial} = -V_{CC}$ and $V_{final} = V_{CC}$, then, as shown earlier,

$$T = RC \ln 2 \tag{11.43}$$

$$\text{or} \quad T = 0.69\, RC$$

We see that T_1 'ON' lasted only for the duration of T and the circuit returned to its permanent state. This state is, therefore, called a quasi-stable state. The monstable multivibrator can be used to establish a fixed time interval of T seconds.

Example 11.3.1

A monostable multivibrator circuit is shown in Fig. E 11.3.1. Calculate the values of the voltages at the collectors and bases of T_1 and T_2 in the stable state. Also find T. It is given that $h_{FE} = 20$ and V_{BE} (Sat) $= 0.7V$, V_{CE} (Sat) $= 0.3V$ and $V_{cut-in} = 0.6$ V for the transistors.

$$\text{Since } T_2 \text{ is 'ON'}, \quad V_{C2} = 0.3V$$

$$V_{B2} = 0.7V$$

$$\text{and} \quad I_{C2} = \frac{12-0.3}{2 \times 10^3} = 5.85 \text{ mA}$$

Also T_1 is 'OFF', therefore

$$V_{C1} = 12V$$

$$\text{and} \quad V_{B1} = \frac{V_{C2} \times R_2}{R_1 + R_2} - V_{BB}.\frac{R_1}{R_1 + R_2}$$

$$= \frac{0.3 \times 10}{35.0} - \frac{12 \times 22}{35.0} = -6.68V$$

$$T \text{ is given as } 0.69\, RC = 0.69 \times 22 \times 10^{+3} \times .001 \times 10^{-6}$$

$$= 0.015 \text{ m sec} = 15\ \mu \text{ sec.}$$

The C_2 and R_3 form the triggering circuit. The diode allows a negative signal only to pass through to the collector circuit.

C_1 in Fig. 11.17 and Fig. E. 11.3.1 is called a commutating capacitor. It assists the monostable multivibrator in making fast changeover from one stable state to the quasi-stable state. It is also known as 'speed up' capacitor. It aids the switching by causing the base of T_1 to respond more rapidly to a change at the collector of T_2. The capacitor hastens the removal of the stored base charge of T_1 so that it can switch 'OFF' from 'ON' at the end of the period T. The value of C_1 depends upon the transistors and R_1 and R_2 and may be in the range of tens of picofarads.

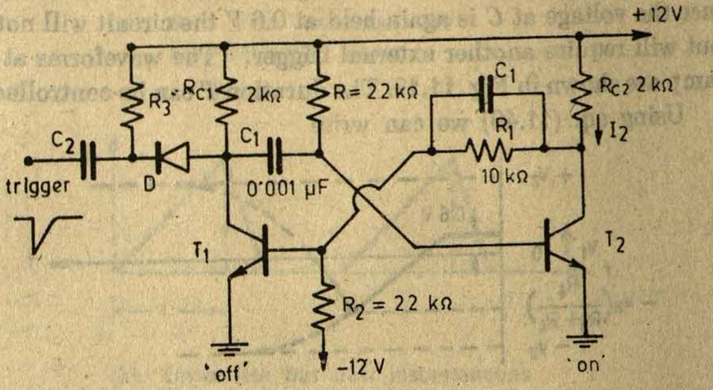


Fig. E 11.3.1 Monostable Multivibrator with triggering arrangement

11.3.2 Monostable Multivibrator using Op-Amps

The op-amp based astable multivibrator of section 11.2 can be modified to act as a monostable circuit. The capacitor C in Fig. 11.15 was allowed to charge to $+V_Z$ and $-V_Z$ and whenever the voltage at the negative terminal of the op-amp exceeded the $V_{threshold}$, the circuit switched states. In order to make one of the states 'stable' the excursion of C is limited in one direction by putting a diode D_1 across it as shown in Fig. 11.18. The trigger signal is applied at the positive ter-

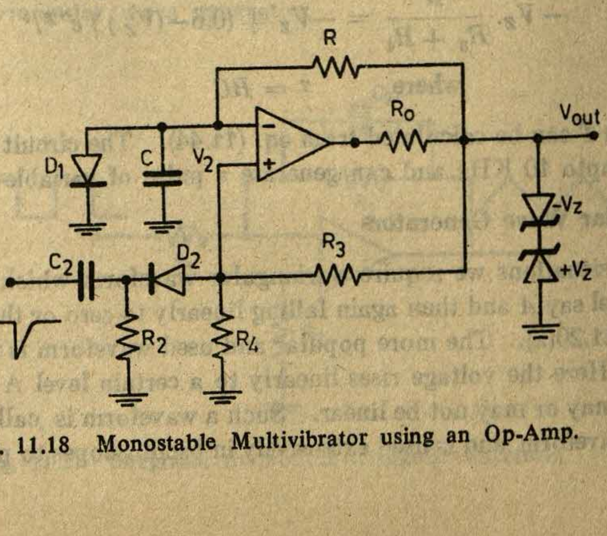


Fig. 11.18 Monostable Multivibrator using an Op-Amp.

minal through a diode D_2 and C_2R_2 circuit. In the steady state the positive voltage feedback at the plus terminal makes the V_{OUT} as $+V_Z$ as long as the voltage at the negative terminal is fixed at about 0.6V (the voltage of the diode D_1). The voltage at the positive terminal is greater than 0.6V i.e.,

$$(V_Z.R_4)/(R_4+R_3) > 0.6V.$$

The negative trigger signal reduces the voltage V_2 below V_1 and the output swings to—V_Z. The capacitor C now starts charging to $-V_Z$ through R. As soon as the voltage V_1 becomes less than V_2 the circuit switches back to its initial state. Since the voltage at C is again held at 0.6 V the circuit will not trigger again by itself but will require another external trigger. The waveforms at the terminals of the op-amp are shown in Fig. 11.19. The duration T can be controlled by adjusting R_3 or R_4. Using eq. (11.40) we can write

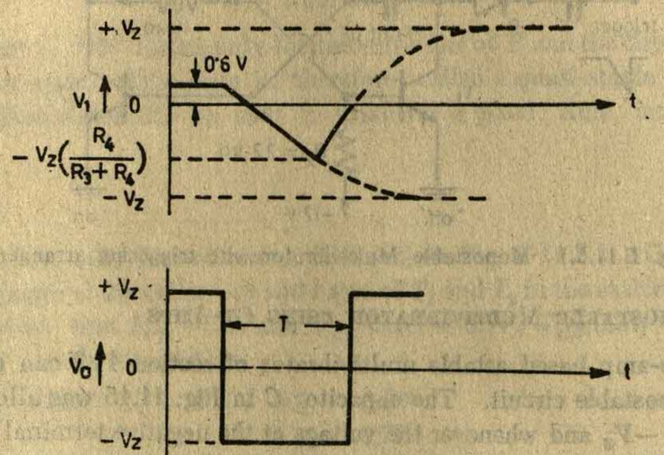


Fig 11.19 Waveforms at the Op-Amp input and output terminals

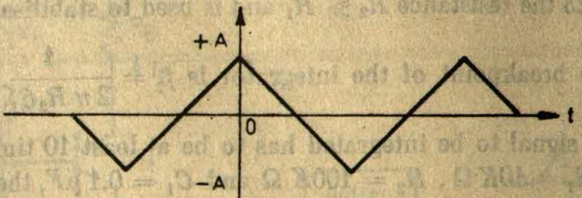
$$-V_Z.\frac{R}{R_3+R_4} = -V_Z + (0.6-(V_Z))\,e^{-T/\tau} \qquad (11.44)$$

$$\text{where} \qquad \tau = RC$$

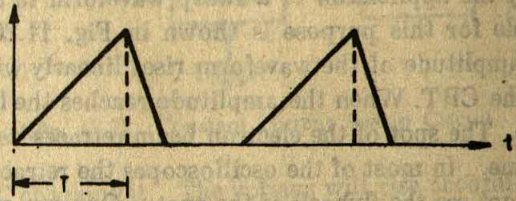
Thus the width T can be calculated from eq. (11.44). The circuit is useful for triggering speeds upto 10 KHz and can generate a pulse of variable width.

11.4 Triangular Wave Generators

In many situations we require a triangular waveform which is rising linearly to a certain level say A and then again falling linearly to zero or the previous level as shown in Fig. 11.20(a). The more popular and used waveform is the one shown in Fig. 11.20(b) Here the voltage rises linearly to a certain level A but its fall back is quicker and may or may not be linear. Such a waveform is called sweep, ramp or sawtooth waveform and is used extensively in oscilloscopes to produce the linear



(a) Both rise and fall are symmetrically linear



(b) Linear rise but near instantaneous fall (sweep)

Fig. 11.20 Triangular Waveforms

movement of the electron beam on the screen of the Cathode Ray Tube (Section 3.5). Variety of circuits have been used to generate the sweep waveforms but we shall describe only one or two representative circuits.

The triangular waveform of Fig. 11.20(a) is easily generated by integrating a square wave. The integrator was described in Chapter 8. The circuit of Fig. 11.21 shows a trinagular wave generator.

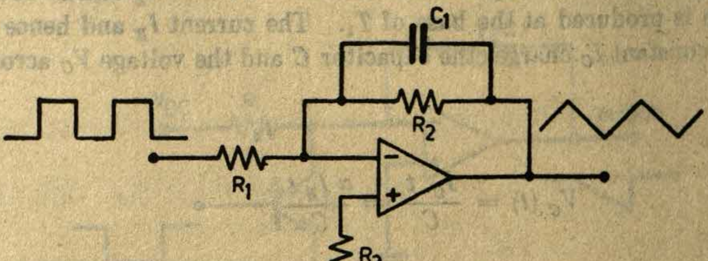


Fig. 11.21 Integrator to produce triangular waveform

In Fig. 11.23 the resistance $R_2 \gg R_1$ and is used to stabilise the operation of thé circuit. The breakpoint of the integrator is $f_2 = \frac{1}{2\pi R_2 C_1}$. The minimum frequency of the signal to be integrated has to be at least 10 times larger than f_2. For example if $R_1 = 10K\,\Omega$, $R_2 = 100K\,\Omega$ and $C_1 = 0.1\,\mu F$, then the frequencies above which the circuit will act as an triangular generator are 160 Hz and above.

Sweep waveform

In all Oscilloscopes and Television receiver etc. the election beam is shifted from left to right, say, by the application of a sweep waveform to the horizontal plates. A waveform suitable for this purpose is shown in Fig. 11.20(b). Over the time $O-T$ seconds the amplitude of the waveform rises linearly with time and the spot moves linearly on the CRT. When the amplitude reaches the level A the waveform falls quickly to zero. The spot of the electron beam retraces its path to the original position in quick time. In most of the oscilloscopes the retrace of the spot is blanked out and we do not see the flyback of the spot. One can see that there are two or three important conditions that are required for a sweep waveform. The most important requirement is that the waveform be absoletely linear over the period $O-T$. Secondly its flyback period be small and thirdly the start of the sweep be controllable from outside. In other words the sweep should start whenever a trigger signal is applied and also it should stop when it reaches a predetermined level, say A. A detailed discussion of sweep circuits is beyond the scope of this book and we shall attempt a brief description only.

Among the many categories of the sweep circuits possibly the three most important ones are the (i) constant-current sweep (ii) Miller sweep and (iii) Bootstrap sweep generators. We had described a constant current source in connection with the input circuit of an op-amp in Chapter 8. A block diagram of a constant current sweep is shown in Fig. 11.22. The Zener diode V_Z and D conduct and a fixed voltage is produced at the base of T_1. The current I_E and hence I_C are constant. The constant I_C charges the capacitor C and the voltage V_C across the capacitor is

$$V_C(t) = \frac{I_C \cdot t}{C} = \frac{\alpha I_E t}{C} \quad (11.45)$$

Normally, if the base of T_2 is kept 'High' then T_2 will be in saturation and all the I_C will be diverted into it. The voltage across C will practically be zero ($\approx$0.3V). If a negative going pulse is applied at the base of T_2, then T_2 will cut-off and the cur-

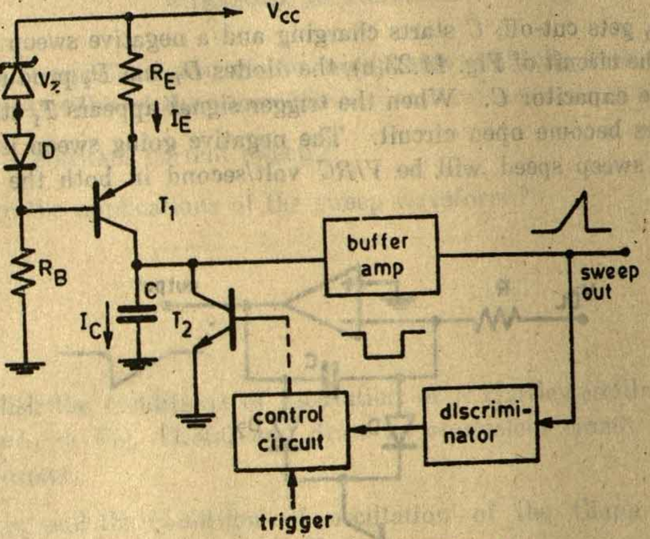
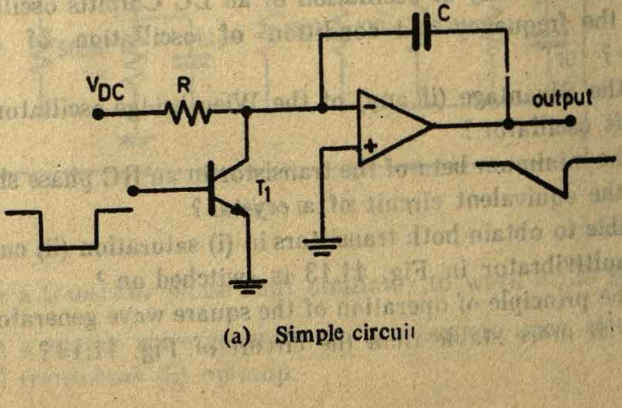


Fig. 11.22 Constant current Sweep Circuit

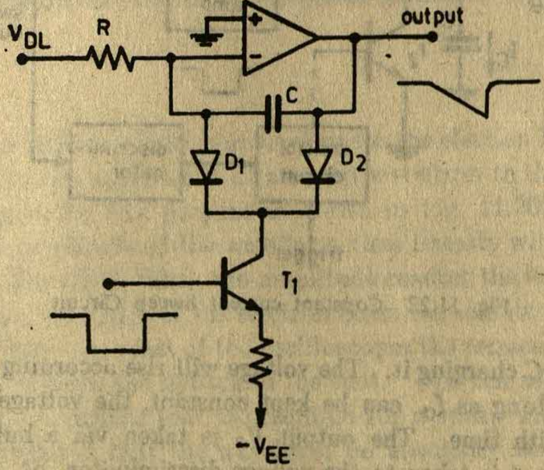
rent I_C will flow in C charging it. The voltage will rise according to the eq. (11.45). It is seen that, as long as I_C can be kept constant, the voltage across C will be varying linearly with time. The output V_C is taken via a buffer amplifier. A portion of the output is taken to the voltage discriminator or threshold circuit. When the output reaches 'A' volts (Fig. 11.20) the discriminator produces an output which in turn triggers the control circuit. The output of the control circuit goes 'High' again and the sweep stops. The 'control' circuit has an additional provision of a trigger input to initiate the sweep cycle. The control circuit will just be a flip-flop in this situation.

The integrator of Fig. 11.21 can also be modified to produce a sweep circuit. This type of sweep is called a Miller Sweep circuit. Two arrangements for reducing the retrace or flyback period are shown in Fig. 11.23. The linearity of the sweep will depend on the gain of the amplifier. In both circuits, as long as the base of T_1 is high the output is at zero volts. In Fig. 11.23(a) as soon as the base of T_1



(a) Simple circuit

goes 'Low' T_1 gets cut-off, C starts charging and a negative sweep appears at the output. In the circuit of Fig. 11.23(b), the diodes D_1 and D_2 produce a short circuit across the capacitor C. When the trigger signal appears T_1 stops conducting and the diodes become open circuit. The negative going sweep is formed at the output. The sweep speed will be V/RC volt/second in both the cases.



(b) another arrangement ($V_{DL}=V_{DC}$).

Fig. 11.23 Miller Sweep Circuits

Review Questions

11.1 What is the Berkhausen criterion of oscillation ?

11.2 What is the difference between feedback oscillators and negative resistance oscillators ?

11.3 What is the difference between the Colpitts and Clapp oscillators ?

11.4 What is the condition of balance of the Wien-bridge ?

11.5 What is the frequency of oscillation of an LC Colpitts oscillator.

11.6 What is the frequency and condition of oscillation of a Wien-bridge oscillator ?

11.7 What is the advantage (if any) of the Wien-bridge oscillator over the RC phase-shift oscillator ?

11.8 What is the minimum beta of the transistor in an RC phase shift oscillator ?

11.9 What is the equivalent circuit of a crystal ?

11.10 Is it possible to obtain both transistors in (i) saturation (ii) cut off, when the astable multivibrator in Fig. 11.13 is switched on ?

11.11 What is the principle of operation of the square wave generator using an op-amp ? Is it more stable than the circuit of Fig. 11.13 ?

11.12 Compare the performance of the monostable multivibrators using transistors (Fig. 11.17) and the timer 555 ?

11.13 What is a constant current sweep ?

11.14 What are the applications of the sweep waveform ?

Problems

P 11.1 Establish the conditions of oscillation of a Hartley oscillator. Assume $L_2 = nL_1$ in Fig. 11.3(a) and draw an equivalent circuit for the autotransformer.

P 11.2 Find ω_0 and the condition of oscillation of the Clapp oscillator in Fig. 11.3(d).

P 11.3 Design a Clapp oscillator to oscillate at 2 MHz.

P 11.4 Design a Wien-bridge oscillator at 1 KHz frequency.

P 11.5 Find the frequency of oscillation of the RC phase-shift oscillator shown in Fig. P 11.1. Given that $I_D = 2mA$ and $g_m = 2\ mA/V$. What is the gain ?

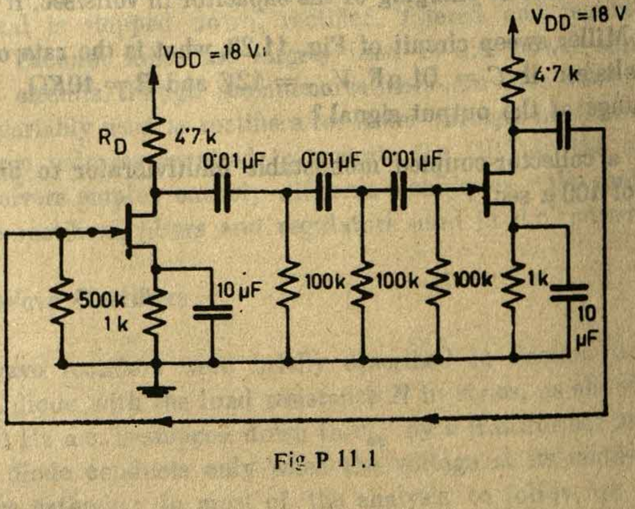


Fig P 11.1

P 11.6 Design a transistor phase shift oscillator to work at 20 KHz.

P 11.7 Design a square wave generator to give square wave signal at 10 KHz. Use (i) transistors (ii) op-amp.

P 11.8 An astable multivibrator using FET is shown in Fig. P 11.2. Find the waveforms at the drain, gate and the source and calculate the frequency.

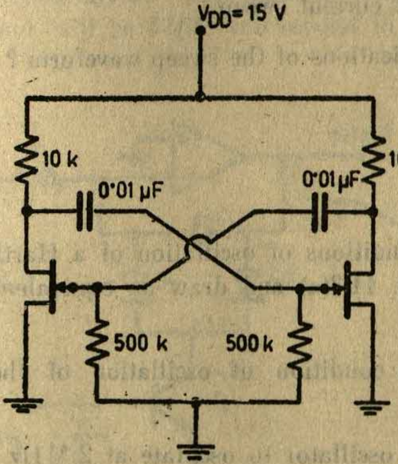


Fig P 11.2

P 11.9 Design a monostable circuit of Fig. 11.18 to give a gate signal of 10 μ-sec. with a peak-to-peak signal of ± $3V$.

P 11.10 In the circuit of Fig. 11.22, find the constant current I_C if $V_{CC} = 12V$, $V_Z = 8V$ and $R_E = 2K\Omega$. Assume a drop of 0.7 across the diodes. What is the rate of charging of the capacitor in volts/sec. if $C = .01$ μF ?

P 11.11 In the Miller sweep circuit of Fig. 11.23, what is the rate of charging of C in volts/sec if $C = .01$ μF, $V_{DC} = 12V$ and $R = 10K\Omega$, What is the total range of the output signal ?

P 11.12 Design a collector-coupled monostable multivibrator to produce a gate signal of 100 μ sec.

12

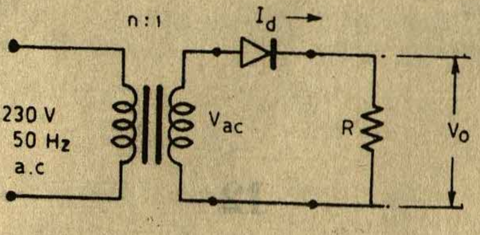
Power Supplies

12.0 Introduction

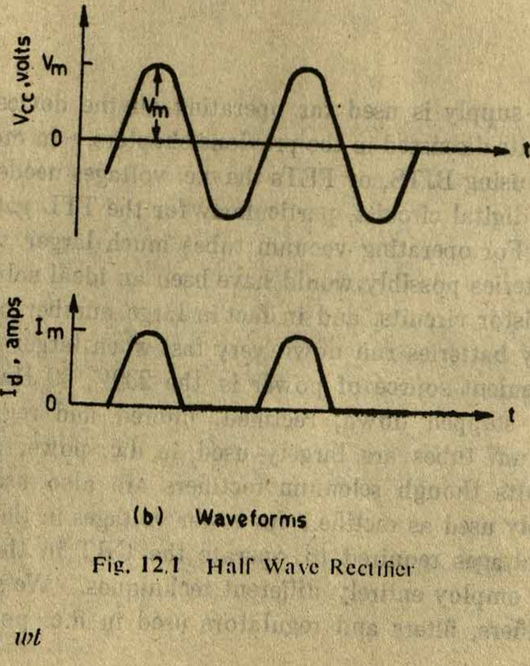
A d.c. power supply is used for operating all the devices in the analogue and the digital circuits discussed in the previous chapters. In most of the analogue circuit applications using BJTS, or FETs the d.c. voltages needed are in the range of $\pm 18V$. In the digital circuits, particularly for the TTL gates the d.c. voltage required is $+5V$. For operating vacuum tubes much larger voltages, like $250V$. etc, are used. Batteries possibly would have been an ideal solution for supplying power to the transistor circuits, and in fact in large number of applications they are. Unfortunately batteries run down very fast when larger currents are drawn and the only convenient source of power is the $230V$, 50 Hz a.c. supply mains. The a.c. signal is stepped down, rectified, filtered and regulated to give the required d.c. Vacuum tubes are largely used in d.c. power supplies meant for vacuum tube circuits though selenium rectifiers are also used. Semiconductor diodes are invariably used as rectifiers for lower voltages in the transistor circuits. Extremely large voltages required to operate the CRT in the oscilloscopes and television receivers employ entirely different techniques. We shall in this chapter discuss diode rectifiers, filters and regulators used in d.c. power supplies.

12.1 Half Wave Rectifiers

Half wave rectifiers were briefly described in Section 3.1.1. The circuit consists of a diode with the load resistance R in series, as shown in Fig. 12.1(a). The $230V$, 50 Hz a.c. is stepped down to v_{ac} by a transformer and applied to the diode. The diode conducts only when the voltage at its anode is positive with respect to the cathode. In most of the analysis to follow we shall neglect the small cut-in voltage of the diode in comparison to the v_{ac} The diode current i_a is therefore, as shown in Fig. 12.1(b). It is positive and unidirectional. The output voltage V_o across the load resistance will be i_aR. Now



(a) Circuit diagram



(b) Waveforms

Fig. 12.1 Half Wave Rectifier

$$v_{ac} = V_m \sin \omega t$$

hence

$$i_d = \frac{V_m \sin \omega t}{R} = I_m \cdot \sin \omega t \qquad 0 \leqslant \sin \omega t \leqslant 1$$

$$\text{and} \qquad = 0 \qquad -1 \leqslant \sin \omega t \leqslant 0 \tag{12.1}$$

where $I_m = V_m/R$, the max. value of the current.

The output voltage will have the same waveshape as the input signal for the positive half cycle and zero otherwise. The average value or d.c. value of the current will be

$$I_{dc} = [\, i_d \,]_{average} = \frac{1}{2\pi} \int_0^{2\pi} \frac{V_m \sin \omega t}{R} \, d\omega t$$

average

$$= \frac{1}{2\pi} \int_0^{\pi} \frac{V_m \sin \omega t.\ d\omega t}{R} + 0$$

$$\text{or} \quad I_{dc} = \frac{V_m}{\pi R} = \frac{I_m}{\pi} \tag{12.2}$$

Thus the average value of the current is $1/\pi$ times the peak value I_m. The average or d.c. value of the voltage

$$V_{dc} = I_{dc} \cdot R = \frac{V_m}{\pi} \tag{12.3}$$

The r.m.s. value of the current can also be found as

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} i_d^2 \ d\omega t}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t \ d\omega t}$$

$$\text{or } I_{rms} = \frac{I_m}{2} \tag{12.4}$$

$$\text{Similarly} \quad V_{rms} = \frac{V_m}{2} \tag{12.5}$$

It is very instructive to examine the various frequency components present in the current waveform i_d of Fig. 12.1(b). A Fourier-Series analysis of the half sinusoidal signal, refer eq. (3.1.2) shows that

$$i_d = \frac{I_m}{\pi} + \frac{I_m}{2} \sin wt - \frac{2I_m}{3\pi} \cos 2\omega t \quad \frac{2I_m}{15\pi} \cos 4\omega t + \tag{12.6}$$

It means that the output consists of a zero frequency or d.c. signal, component at w and various high frequency terms like 2ω, 4ω, etc. The voltage $V_o = i_d R$ will also have the same frequency terms. We are only interested in the dc term in a power supply. All other harmonics are undesirable and have to be removed by a filter as shown later. In fact the ratio of the effective value of the a.c.

components to the d.c. or average value is used as a measure of performance of a power supply and is called the Ripple Factor. The ripple factor is defined as

$$\gamma = \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I^2}}$$

or

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \qquad (12.7)$$

For the half rectifier, from eq. (12.4) and (12.2)

$$I_{rms} = \frac{I_m}{2}, \text{ and } I_{dc} = \frac{I_m}{\pi}$$

hence

$$\gamma = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21 \qquad (12.8)$$

Thus the ripple factor is quite high for the half wave circuit. As was mentioned in Section 3.1.1, the Peak Inverse Voltage (PIV) for a half-wave rectifier is V_m Volts.

Example 12.1.1

In the half wave rectifier of Fig. 12.1, the input voltage v_{ac} to the rectifier is 20 sin 314t and the load resistance is 500 Ohms. Calculate (i) the peak, average and the rms values of the current (ii) the d.c. voltage and power output (iii) the a.c. power input and (iv) the ripple factor. Assume the diode to be ideal.

Now $V_m = 20$ volts
hence $I_m = V_m/R = (20/0.5)$ mA $= 40$ mA
From eqn. (12.2)

$$I_{dc} = \text{average value of the current} = I_m/\pi$$
$$= 40/\pi = 12.73 \text{ mA}$$

From Eqn. (12.7)

$$I_{rms} = I_m/2 = 20 \text{ mA}$$

$$V_{dc} = \frac{V_m}{\pi} = \frac{20}{\pi} = 6.37 \text{ volts.}$$

$$V_{rms} = \frac{20}{2} = 10 \text{ volts.}$$

The d.c. power output $= I_{dc}^2 . R$

$$= (12.73)^2 \times 10^{-6} \times 0.5 \times 10^3$$
$$= 81.03 \text{ mW}$$

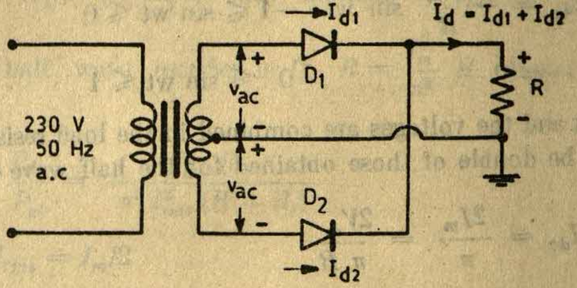
The a.c. power input $= I^2_{rms} \cdot R$ (since the diode is ideal)

$= 200$ m.W.

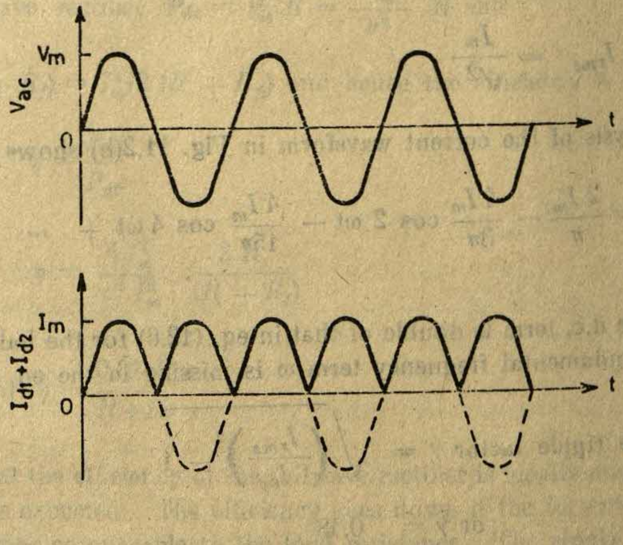
The ripple factor from eqn. (12.8) is 1.21

12.1.2 Full Wave Rectifier

The circuit arrangement in the half-wave rectifier is such that the current is driven into the load only during half the cycle. By the full wave rectifier arrangement of Fig. 12.2(a) it will be possible to get over this difficulty and drive the load during the positive and the negative half cycles of the input. The circuit consists of a centre tapped transformer with the windings as indicated. During



(a) Circuit diagram



(b) Waveforms

Fig. 12.2 Full wave Rectifier

the positive half cycle, the diode D_1 conducts and the current i_{d1}, flows into the load R. The voltage at the anode of diode D_2 is negative throughout this positive cycle and hence it is cut-off. During the negative half cycle the voltage at the anode of D_2 is positive and it conducts with current i_{d2}. Thus, the load current and hence the voltage across R is unidirectional as showa in Fig. 12.2(b). The currents i_{d1} and i_{d2} are

$$i_{d1} = \frac{V_m}{R} \sin wt \qquad 0 \leqslant \sin wt \leqslant 1$$

$$= 0 \qquad -1 \leqslant \sin wt \leqslant 0$$

and

$$i_{d2} = -\frac{V_m}{R} \sin wt \qquad -1 \leqslant \sin wt \leqslant 0$$

$$= 0 \qquad 0 \leqslant \sin wt \leqslant 1$$

The two currents and the voltages are combined in the load resistance R. Hence their values will be double of those obtained for the half wave circuit. Thus

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R} \tag{12.9}$$

$$V_{dc} = \frac{2V_m}{\pi} \tag{12.10}$$

Calculating the rms value

$$I_{rms} = \frac{I_m}{\sqrt{2}} \tag{12.11}$$

A Fourier analysis of the current waveform in Fig. 11.2(b) shows that

$$I_d = I_{d1} + I_{d2} = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t - \frac{4I_m}{15\pi} \cos 4\omega t + \ldots \tag{12.12}$$

As expected, the d.c. term is double of that in eq. (12.6) for the half wave circuit, but then the fundamental frequency term ω is missing in the eq. (12.12).

$$\text{The ripple factor } \gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\text{or } \gamma = 0.48 \tag{12.13}$$

Eq. (12.13) shows that the ripple factor in full wave rectifier is much less than that of the half-wave rectifier.

Between the two rectifier circuits, the half wave and the full wave — the voltage output, ripple factor and the efficiency of the full wave rectifier is superior. An additional factor in favour of the full wave rectifier circuit is that equal current flows through the two halves of the centre tapped secondary of the transformer and consequently d.c. saturation of the core is avoided. Half wave rectifier has the advantage of a simpler circuitry and lower cost.

The efficiency of the rectifier circuit is defined in terms of the d.c. power output to the load and the total power input from the a.c. supply. Thus, in the half wave rectifier circuit the total input power is $I_{rms}^2 . R$. We have assumed that the diode is lossless but in actual circuits there is an equivalent forward resistance R_f of the diode. This resistance is the average slope of the *v-i* characteristic of the diode. The total input power is thus modified to $I_{rms}^2 (R + R_f)$. The d.c. output power in half wave rectifier is $I_{dc}^2 \ R = \frac{I_m^2}{\pi^2} R$. Hence the efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_m^2 \ R}{\pi^2 \ I_{rms}^2 \ (R + R_f)} \tag{12.14}$$

Substituting for $I_{rms} = I_m/2$

$$\eta = 0.405 \frac{R}{R + R_f} \tag{12.15}$$

For the full wave rectifier $P_{dc} = I_{dc}^2 \ R = \frac{4I_m^2}{\pi^2} \ R$ and

$P_{ac} = I_{rms}^2 \ (R + R_f) = I_m^2/2 \ (R + R_f)$ and hence the efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$\eta = \frac{4 \, I_m^2}{\pi^2 \, I_m^2} . \frac{2 \, R}{(R + R_f)}$$

$$\text{or } \eta = \frac{0.81 \, R}{R + R_f} \tag{12.16}$$

We see that the efficiency of the fullwave rectifier is ideally double of the half wave rectifier as expected. The efficiency goes down if the forward resistance of the diode becomes comparable to the load resistance. The ripple factor in both the half wave and the full wave rectifiers is still considerably higher than desirable.

The frequency components other than the zero frequency must be reduced by some method in order to provide a useful d.c. voltage at the output. The simplest technique will be to filter out the unwanted frequencies by a low pass filter.

Example 12.1.2

The load resistance in the full wave rectifier circuit of Fig. 12.2(a) is 0.5 K Ohms and the transformer rating is 230V, 50 Hz primary with 30-0-30 volts secondary. The diode resistance is $R_f = 50$ Ohms. Calculate (i) the peak, average and rms values of the current (ii) average value of the d.c. (iii) the d.c. power output, (iv) the efficiency and (v) the ripple factor.

$$\text{Now } I_m = \frac{V_m}{R} = \frac{30}{0.5} = 60 \text{ mA}$$

$$\text{From } I_{dc} = \frac{2I_m}{\pi} = 38.2 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = 42.43 \text{ mA}$$

$$V_{dc} = \frac{2V_m}{\pi} = 19.1 \text{ volts}$$

D.C. power output = $I_{dc}^2 \times R$ = 729.62 mW

Total power input = $I_{rms}^2 (R + R_f)$ = 990.17 mW

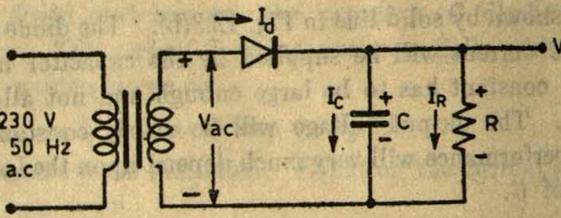
$$\text{Hence the rectifier efficiency} = \frac{729.62}{990.17} = 73.69\ \%$$

The ripple factor = 0.48

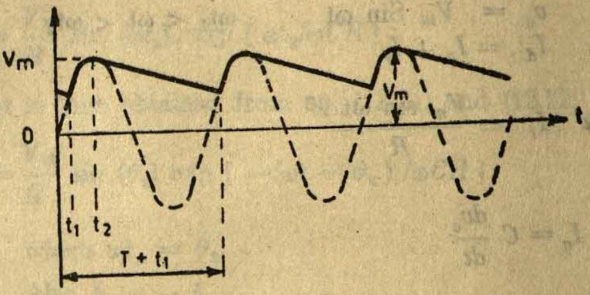
12.2 Capacitor Input Filter

One of the commonly used filters is a large capacitor across the load. This is done with a view to bypass or provide another low resistance path to the harmonics of the rectifier signal. If the reactance of the capacitor $X_C \leqslant R$, then the 50 Hz, 100 Hz and 200 Hz signal components, etc are shunted by the capacitor and hence very small amounts of these a.c. currents flow into the load R. In fact the situation changes dramatically in the case of half wave rectifier with capacitor input filter as shown in Fig. 12.3.

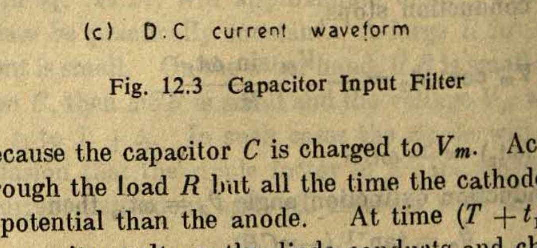
During the positive half cycle the diode conducts and the capacitor C charges to the peak value of v_{ac}. After that the voltage v_{ac} starts falling but the diode



(a) Capacitor filter



(b) Voltage waveform



(c) D.C current waveform

Fig. 12.3 Capacitor Input Filter

cannot conduct because the capacitor C is charged to V_m. Actually the capacitor does discharge through the load R but all the time the cathode of the diode is at a higher positive potential than the anode. At time $(T + t_1)$ the input voltage again exceeds the capacitor voltage, the diode conducts and charges the capacitor again. The capacitor voltage follows the input during the interval t_1 to t_2 and the diode current flows as shown in Fig. 12.3(c) The capacitor provides the load current during the period t_2 to $T + t_1$ by discharging through the load. The discharge time constant is RC. If this time constant is low then the capacitor will discharge more during the interval. The voltage waveform across the load will therefore be as shown by solid line in Fig. 12.3(b). The diode current will be in pulses and the load current will be supplied by the capacitor most of the time. Of course the time constant has to be large enough and not allow the capacitor to discharge much. The output voltage will be nearly constant and the ripple will be low. The performance will very much depend upon the load current drawn for a given value of C.

The i_d and V_{dc} can be calculated as follows. The current i_d flows in pulses when the diode conducts and charges the capacitor. During this interval the voltage across the capacitor follows the input supply signal and is equal to it. Thus, during t_1 to t_2

$$v_c = V_m \text{ Sin } \omega t \qquad \omega t_1 < \omega t < \omega t_2$$

and $I_d = I_c + I_r$

Now $I_r = \dfrac{V_m \sin \omega t}{R}$

and $I_c = C \dfrac{dv_c}{dt}$

or $I_c = wC\, V_m \cos \omega t$

Hence, during t_1 to t_2

$$I_d = \frac{V_m \sin wt}{R} + \omega C V_m \cos \omega t$$

$$= \frac{V_m}{R}\sqrt{1 + \omega^2 c^2 R^2} \sin\left[\omega t + \tan^{-1}(\omega CR)\right] \qquad (12.17)$$

During the rest of the cycle $I_d = 0$ and $I_c = -I_r$. Thus at the time t_2, immediately as the conduction stops,

$$\omega C\, V_m \cos \omega t_2 = -\frac{V_m \sin \omega t_2}{R}$$

$$\text{or } \tan(\omega t_2) = -\omega CR \qquad (12.18)$$

If we define the conduction extinction angle $\theta_2 = \omega t_2$, then

$$\theta_2 = \tan^{-1}(-wCR)$$

We can write $\tan^{-1}(\omega CR) = \pi - \tan^{-1}(-\omega CR)$ (12.19)

Hence the diode current of eq. (12.17) can be rewritten as

$$i_d = \frac{V_m}{R}\sqrt{1 + \omega^2 C^2 R^2} \sin(\omega t_2 - \omega t) \qquad \dots \omega t_1 < \omega t < \omega t_2 \qquad (12.20)$$

Once the diode switches off, the capacitor C discharges through R as mentioned earlier. The current I_r reduces exponentially with a time constant of CR and can be written down as

$$-I_c = I_r = A \exp\,(-t_2/CR) \tag{12.21}$$

where A is a constant to be evaluated. Equating the current just before and after the time I_2 we can write

$$\frac{V_m}{R} \sin \omega t_2 = A \exp\,[-t_2/CR]$$

$$= A \exp\,[-\omega t_2/wCR]$$

$$\text{hence } A = \frac{V_m}{R} \sin\,(\omega t_2).\ \exp\,[\omega t_2/\omega CR] \tag{12.22}$$

The load current is thus obtained from eq. (12.21) and (12.22) as

$$I_r = \frac{V_m}{R} \sin\,(\theta_2) \exp\,[-(\omega t - \theta_2)/\omega CR] \tag{12.23}$$

where $wt_2 = \theta_2$

Also $I_c = -I_r$

and $V_c = V_R = I_R.R$

The voltage of the capacitor during the interval when it is supplying current is, thus

$$V_c = V_m.\sin\,(\theta_2) \exp\,[-\omega t - \theta_2)/wCR) \tag{12.24}$$

The extinction angle θ_2 lies in the second quadrant and will be between 90° to 180° depending upon the value of wRC. Similarly the voltage at the output, eq. (12.24), depends upon wCR. Since CR has the dimension of time, wCR is a dimension-less number. If C or R is large the term wCR will be large and the exponential term in eq. (12.24) will approximate unity. The voltage across the load will in this case be practically constant. A large R for a given C will mean that the load current is small. On the other hand, if R is small and the load current is heavy for a given C, then wCR is small and the voltage V_R will drop appreciably during the period t_2 to $T + t_1$. In such cases the ripple will be quite high. We come to the conclusion that the ripple factor in a capacitor-input filter circuit is very much load-current dependent and will increase with the load current.

Once the input signal exceeds the voltage across the capacitor at $T + t_1$ the diode switches on and charges the capacitor. The input voltage at $T + t_1$ is

$$V_R = V_c = V_m \sin\,(2\pi + \omega t_1)$$

$$= V_m \sin \omega t$$

$$\text{or } V_c = V_m \sin \theta_1 \tag{12.25}$$

where $\omega t_1 = \theta_1$ is the ignition or firing angle. Equating the voltage just before and after the time t_1, we obtain from eq. (12.24) and (12.25)

$$V_m \sin \theta_1 = V_m \sin \theta_2 \exp [-(\omega t_1 - \theta_2 + 2\pi)/wCR] \tag{12.26}$$

Hence $\sin \theta_1 = \sin \theta_2 . \exp [-(\theta_1 - \theta_2 + 2\pi)/wCR)$ (12.27)

We see that θ_1, θ_2 and wCR are interconnected in a very complex manner, Once we select wCR, the value of θ_2 is fixed from eqn. (12.18) and θ_1 can be calculated from eq. (12.27). Since eq. (12.27) is a transcendental equation it is difficult to calculate θ_1. Graphical methods are often employed to determine θ_1. Taking a value of wCR for example, we find θ_2 from eq. (12.18) and plot the left-hand and right-hand sides of eq. (12.27) separately for various values of θ_1.

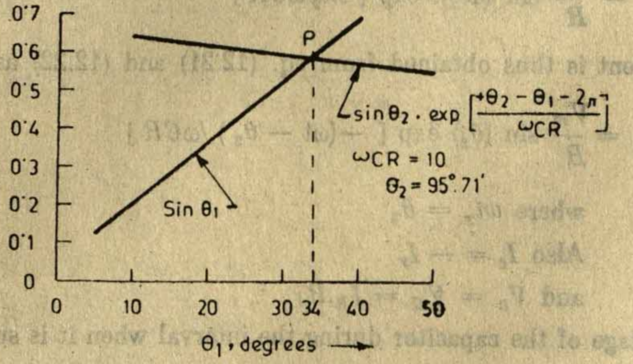


Fig. 12.4 Plot of Sin θ_1 and sin θ_2. exp [$(\theta_2 - \theta_1 - 2\pi)$/wcR] for different values of θ_1.

Assuming a value of $wCR = 10$, $\theta_2 = 95.71°$ we have plotted the curves for $\sin \theta_1$ and $\sin \theta_2 \exp \dfrac{\theta_2 - \theta_1 - 2\pi}{10}$ in Fig. 12.4. We see that two curves intersect at P. Hence $\theta_2 = 95.71°$ and $\theta_1 = 34°$. In a similar manner we can obtain graphically the values of θ_2 and θ_1 for different wCR. We have given a set of values of wCR, θ_2 and θ_1 in Table 12.1.

Table 12 1 : Conduction angles in rectifier

wCR	θ_2 in degree	θ_1 halfwave in degree	θ_1 fullwave in degrees
1	135.0	1	20
5	101.3	25	46
10	95.71	34	58
40	91.4	60	74
100	90.57	72	80

The voltage at the output follows the input signal for the period t_1 to t_2 and then follows the curve of eq. (12.24). This waveform has been shown dotted in the Fig. 12.3(b). The d.c value of the output can be found by averaging this curve over the two periods. Thus

$$V_{dc} = \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2} V_m \sin \omega t \, d\omega t + \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} V_c \, d\omega t \qquad (12.28)$$

where V_c is given in eq. (12.24)

$$V_c = V_m \sin \theta_2 . \exp \left[\frac{\theta_2 - wt}{wCR}\right]$$

Solving eq. (12.28)

$$V_{dc} = \frac{V_m}{2\pi} \sqrt{1 + w^2C^2R^2} \, . \, [1 - \cos(\theta_2 - \theta_1)] \qquad (12.29)$$

We see from eqn. (12.29) that V_{dc} is strongly dependent on wRC and the conduction angle $(\theta_1 - \theta_2)$. But the conduction angle itself depends on wRC, hence V_{dc} will be a function of wCR only. For a fixed load, wCR will be small when C is small, and it will be large for a large C. Thus, for a small capacitor the V_{dc} approaches V_m/π. As C is increased, the d.c. output voltage increases and approaches V_m. Fig. 12.5 shows a plot of wCR versus V_{dc}/V_m.

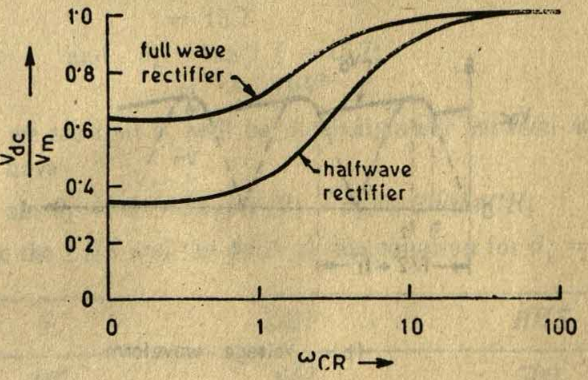


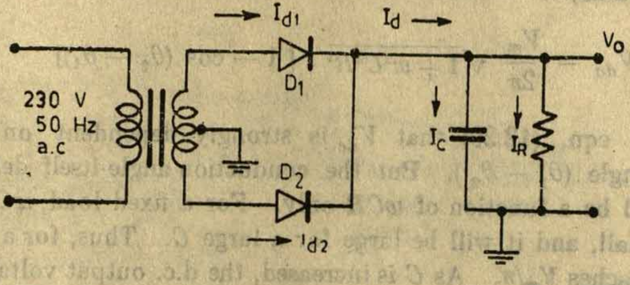
Fig. 12.5 ωCR vs. output voltage

Since the capacitor is charged upto $+V_m$, the diode has to face a maximum voltage of $V_m - (-V_m) = 2V_m$ on the negative half cycle. The *PIV* of the diode is therefore $2V_m$. The diode current has a maximum and as wCR is higher, the peak is more pronounced. The actual current in the diode can be calculated from eq. (12.20).

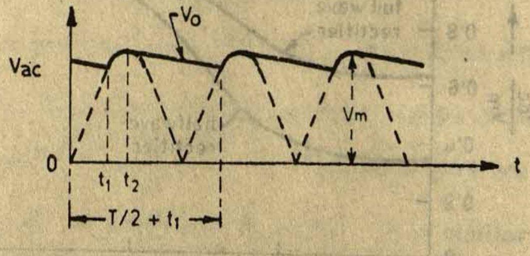
In a half wave rectifier with capacitor input filter when the load current is increased with C remaining fixed, the ripple increases, the d.c. voltage reduces and the performance of the circuit is adversely affected. Such circuits are useful for low current applications only.

12.2.1 FULL WAVE RECTIFIER WITH CAPACITOR INPUT FILTER

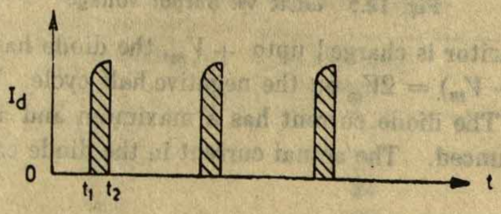
The capacitor input simple filter described can also be used in full wave rectifier circuits. Figs. 12.6 (a), (b) and (c) show the circuit diagram, the voltage waveform V_c and the current pulses I_d. Once the diode D_1 (say) conducts, the capacitor is charged but as the input voltage starts falling, the diode is switched off and the load current is supplied by the charged capacitor. During the negative half cycle, the diode D_2 conducts and charges C. The waveform across the capacitor is shown in Fig. 12.6 (b) and the diode currents in Fig. 12.6 (c).



(a) Circuit diagram



(b) Voltage waveform



(c) Current waveform

Fig. 12.6 Fullwave rectifier with the capacitor input filter

The analysis of this circuit is very similar to the one described above for the half wave rectifier circuit. The ignition angle θ_1 (= ωt_1) and extinction angle θ_2 (= ωt_2) are determined similarly and eq. (12.27) is modified to

$$\sin\theta_1 = \sin\theta_2 \exp\left[-(\theta_1 + \pi - \theta_2)/wCR\right] \qquad (12.30)$$

The eq. (12.30) can be solved graphically. Some selected values of wCR, θ_1 and θ_2 are shown in Table 12.1.

The variation in the V_{dc} due to the variation in wCR, either due to changes in the load or due to a change of C for a fixed load, is calculated and plotted in Fig. 12.5. The changes in V_{dc} due to change in the load is much less in the full-wave circuit in comparison to the half wave rectifier. In ordinary transistor power supplies using semiconductor diodes a large value of ωCR is used. This results in large peak currents through the diodes when they conduct. Semiconductor diodes are capable of withstanding large peak currents. Ripple factor for such power supplies will also be quite low.

Example 12.2.1

In a half wave rectifier with capacitor input filter as shown in Fig. 12.3, the load resistance is 100 Ohms, C is 500 μF and V_{ac} = 30 sin 314t. Find (i) the ignition angle, (ii) the conduction angle and (iii) the d.c. output voltage.

$$\begin{aligned} \text{Now} \quad wCR &= 314 \times 500 \times 10^{-6} \times 100 \\ &= 15.7 \\ \text{and} \quad \theta_2 &= \tan^{-1}(-15.7) \\ &= +93.64^\circ \end{aligned}$$

From table 12.1 we see that θ_1 will be approximately between 40° to 50°. From eqn. (12.27) we have

$$\sin\theta_1 = \sin\theta_2 \exp\left[(\theta_1 - \theta_2 + 2\pi)/wCR\right]$$

We will calculate the *LHS* and the *RHS* of this equation for θ_1 = 40°, 45° and 50°.

θ_1	*LHF*	*RHS*
40°	.642	.709
45°	.707	.7056
50°	.766	.7017

We see that the two values are practically same at 45°. Hence $\theta_1 = 45^\circ$
The conduction angle is $\theta_2 - \theta_1 = 48.6$.
From eq. (12.29), we have

$$V_{dc} = \frac{30}{2\pi}\sqrt{1 + (15.7)^2}\left[1 - \cos(48.6)\right]$$

$$= 25.5 \text{ volts.}$$

Example 12.2.2

A fullwave rectifier has $R = 500$ Ohms and $C = 250\ \mu f$. The ratings of the transformer are 230V/30-0-30 volts. Calculate the conduction angles and the value of d.c. voltage.

We calculate the value of wCR as

$$wCR = 39.25 = 40^\circ$$

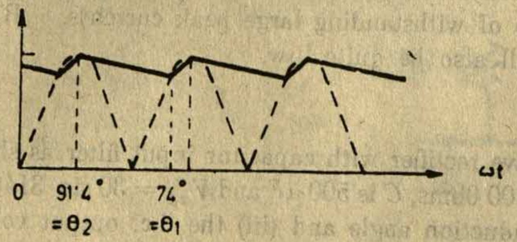
From Table 12.1, for a full wave rectifier with wCR of 40

$$\theta_2 = 91.4$$

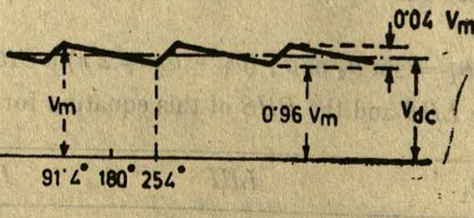
$$\theta_1 = 74^\circ$$

hence $\theta_2 - \theta_1 = 17.4^\circ$

Figure E 12.1 shows the approximate waveform



(a) Waveform



(b) Blownup view

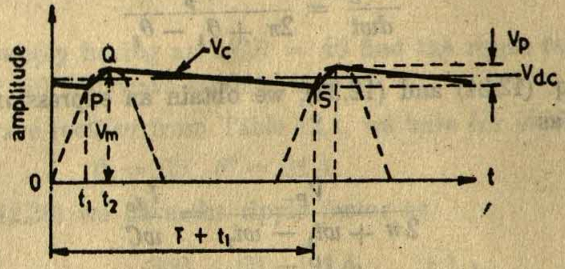
Fig. E 12.1

From Fig. E 12.1 (b) we see that

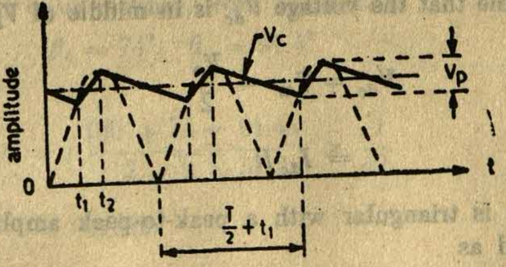
When $\theta_2 = 91.4^\circ$, the voltage V_0 is V_m sin 91.4 = 29.99 volts. At the ignition angle θ_1 the value of V_0 is V_m sin 74° = 28.84 volts. We can assume that V_{dc} is the average value between the two limits. Hence $V_{dc} = 29.42$ volts.

12.2.2 RIPPLE FACTOR CALCULATION

The ripple factor calculation is quite tedious and complex in the case of the capacitor input filters. However, with certain approximations, it can be calculated rather easily. For example, we can assume that the charging and the discharging of the capacitor is linear as shown in Fig. 12.7.



(a) Half wave rectifier



(b) Full wave rectifier

Fig. 12.7 Approximations of the capacitor Voltage

In the half wave rectifier shown in Fig. 12.7 (a), it will mean that *PQ* and *QS* are linear. The waveform is triangular. During the interval t_1 to t_2, the capacitor charges and during the interval t_2 to $T + t_1$ it discharges at a constant rate. While loosing charge the voltage v_c is

$$V_c = q/C$$

where q is the charge.

The rate of loss of charge can be calculated as

$$\frac{dV_c}{d\omega t} = \frac{1}{\omega C}\,(dq/dt)$$

$$\text{Now} \quad dq/dt = I_{dc}$$

$$\text{Hence} \qquad \frac{dV_c}{dwt} = \frac{I_{dc}}{wC} \tag{12.31}$$

As the voltage falls from Q to S in a time $(T + t_1 - t_2)$, the total change is V_P. Thus

$$\frac{dV_c}{dwt} = \frac{V_p}{2\pi + \theta_1 - \theta_2} \tag{12.32}$$

Equating eq. (12.31) and (12.32), we obtain an expression for the peak to-peak voltage V_P as

$$\frac{V_P}{2\pi + wt_1 - wt_2} = \frac{I_{dc}}{wC}$$

$$\text{or} \qquad V_P = \left(2\pi + wt_1 - wt_2\right) \cdot \frac{I_{dc}}{wC} \tag{12.33}$$

We can assume that the voltage V_{dc} is in middle of V_P. That is

$$V_{dc} = V_m - \frac{V_P}{2} \tag{12.34}$$

$$= I_{dc} R$$

The ripple voltage is triangular with a peak-to-peak amplitude V_P. Its r.m.s. value can be found as

$$V_{ac} = \frac{V_P}{2\sqrt{3}}$$

$$\text{or} \quad V_{ac} = \frac{(2\pi + wt_1 - wt_2)}{2\sqrt{3}} \quad \frac{I_{dc}}{wC} \tag{12.35}$$

The ripple factor can, therefore, be written down from eq. (12.34) and (12.35) as

$$\gamma = \frac{V_{ac}}{V_{dc}} = \frac{(2\pi + wt_1 - wt_2)}{2\sqrt{3}} \left(\frac{1}{wCR}\right) \tag{12.36}$$

The ripple factor in the case of the full wave rectifier shown in Fig. 12.7 (b), can be similarly written down as

$$\gamma = \frac{\pi + wt_1 - wt_2}{2\sqrt{3}} \left(\frac{1}{wCR}\right)$$

$$\text{or } \gamma = \frac{(\pi + \theta_1 - \theta_2)}{2\sqrt{3}\,.\,wCR} \tag{12.37}$$

For large wCR values the conduction angle $(\theta_1 - \theta_2)$ can be neglected in comparison to 2π or π in eq. (12.36) and (12.37) and further approximation to the ripple factor may be made.

Example 12.2.3

In a power supply having an $wCR = 40$ find the ripple factor if a (i) half wave rectifier, and (ii) full wave rectifier is used.

For a half wave rectifier from Table 12.1, we have for $wCR = 40$

$$\theta_1 = 60^\circ,\ \theta^o = 91.4$$

Hence from eq. (12.36) we have the ripple factor as

$$\gamma = \left(\frac{360 + 60 - 91.4}{2\sqrt{3} \times 57.2}\right) \cdot \left(\frac{1}{40}\right)$$

$$\gamma = .041$$

In the case of the full wave rectifier, from Table 12.1

$$\theta_1 = 74^\circ,\quad \theta_2 = 91.4^\circ$$

Hence from eq. (12.37)

$$\gamma = \left(\frac{180 + 74 - 91.4}{2\sqrt{3} \times 57.2}\right) \times \frac{1}{40}$$

$$= 0.0205$$

12.3 Inductor Input Filters

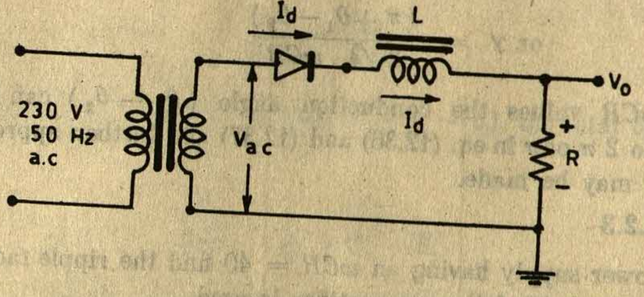
A series inductor may be used to filter out the unwanted frequency components at the output. The inductor does not offer any impedance practically to the zero frequency or d.c. component but offers a high impedance to the harmonic frequencies.

As long as the impedance of the inductor in the Fig. 12.8 (a) is higher than the load resistance R, the unwanted frequency components are reduced in amplitude. The circuit diagram and the waveforms in an inductor input filter in a half wave rectifier are shown in Fig. 12.8. The current I_d can be calculated as follows.

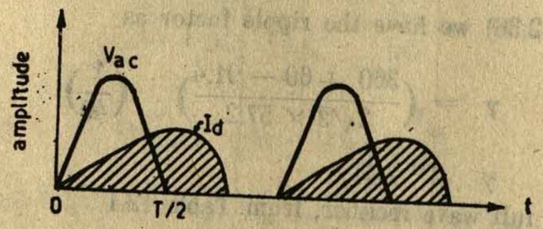
Analysing the circuit of the Fig. 12.8 (a) we can write

$$V_m \sin wt = L\frac{dI_d}{dt} + R\,.\,I_d \tag{12.38}$$

We assume that $I_d = 0$ at $t = 0$, and obtain, by solving the eq. (12.38), the current through the diode as



(a) Circuit diagram



(b) Current waveform

Fig. 12.8 Inductor Input Filter in Half-wave rectifier

$$I_d = \frac{V_m}{\sqrt{R^2 + w^2 L^2}} \sin(wt - \theta) + \sin\theta . \exp\left[- wt . \frac{R}{wL}\right] \qquad (12.39)$$

Where I_m = max value of the current I_d

$$= \frac{V_m}{\sqrt{R^2 + w^2 L^2}}$$

$$\text{and } \theta = \tan^{-1} \frac{wL}{R}$$

We know that the voltage across a capacitor cannot change instantaneously. Similarly a current through an inductor cannot change instantaneously. The inductor stores energy in its magnetic field when the current is rising and going above the average value. Once the current falls below the average value, the inductor releases its stored energy and supplies current to the load. The current in eq. (12.39) consists of two parts. The first part

$$I'_d = \frac{V_m}{\sqrt{R^2+w^2L^2}} \sin(\text{wt} - \theta) \tag{12.40}$$

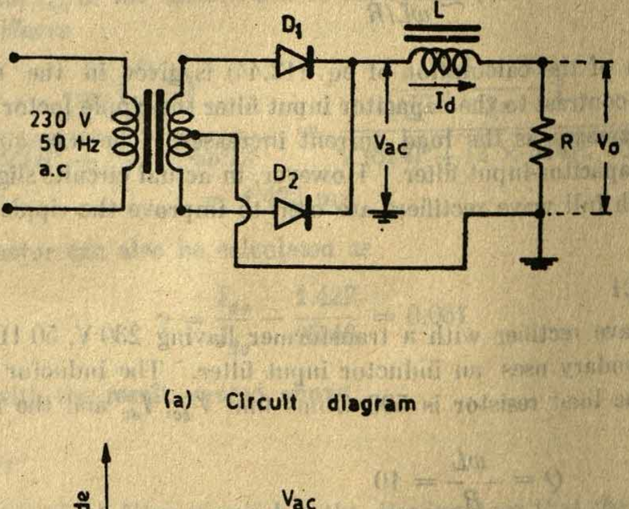
is the usual steady state current produced by the voltage V_m sin wt. The second part

$$I''_d = \frac{V_m \sin\theta}{\sqrt{R^2+w^2L^2}} \,.\, \exp\left[-(wt).\,\frac{R}{wL}\right] \tag{12.41}$$

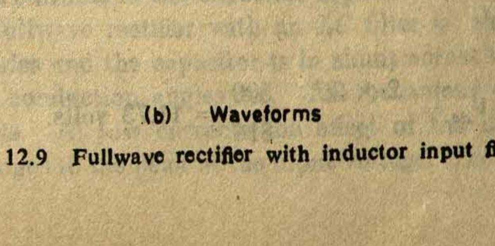
depends upon the inductance and decays slowly as the inductance is increased. At time $t = 0$, the current $I_d = 0$ since both I'_d and I''_d are of opposite sign. The current increases slowly, peaks after a time $t = T/2$ and exists for a considerable period after that, as shown in the figure. The average value of V_{dc} is small and hence the half wave rectifier with inductor filter is not used.

12.3.1 FULLWAVE RECTIFIERS

The full wave rectifier with the inductor input filter is shown in Fig. 12.9(a). The current and voltage waveforms are shown in Fig. 12.9(b). The current in



(a) Circuit diagram



(b) Waveforms

Fig. 12.9 Fullwave rectifier with inductor input filter

individual diodes is shown dotted and hence the total current I_d through the load resistance R is as shown. The individual currents overlap and thus I_d flows throughout the cycle. The d.c. voltage in fullwave rectifier was shown to be, (eq. (12.12)), $\frac{2V_m}{\pi}$. However, in practical inductors there is a loss associated with it and the equivalent circuit is a pure inductance in series with a resistance R_l which accounts for the losses. Thus the d.c. voltage at the output in Fig. 12.9(a) is

$$V_{dc} = \frac{2V_m}{\pi} \cdot \frac{R}{R + R_l} \tag{12.42}$$

and

$$I_{dc} = \frac{2V_m}{\pi} \cdot \frac{1}{R + R_l} \tag{12.43}$$

It can be shown that the ripple factor is approximated as

$$\gamma \approx \frac{0.236}{\omega L/R} \tag{12.44}$$

An illustration of the calculation of eq. (12.44) is given in the example 12.3.1

In direct contrast to the capacitor input filter the ripple factor in the inductor input filter decreases as the load current increases. The d.c. output voltage is higher in the capacitor-input filter. However, in actual circuits slightly more complex filters with full wave rectifiers are used to improve the ripple factor and the regulation.

Example 12.3.1

A full wave rectifier with a transformer having 230 V, 50 Hz. primary and 30-0-30 V. secondary uses an inductor input filter. The inductor has $L = 10\ H$, $Q = 10$. If the load resistor is 500 Ohms find V_{dc}, I_{dc} and the ripple factor.

Since $$Q = \frac{\omega L}{R_l} = 10$$

hence the equivalent loss resistance R_l of the coil $= \frac{314 \times 10}{10}$

$= 314$ Ohms.

From eq. (12.42)

$$V_{dc} = \frac{2 \times 30}{\pi} \cdot \frac{500}{814} = 11.73 \text{ volts.}$$

From eq. (12.43)

$$I_{dc} = \frac{V_{dc}}{R} = 23.46 \text{ mA.}$$

From eq. (12.44)

$$= \frac{0.236}{wL/R} = 0.061$$

If we assume that the output has only the d.c. and second harmonic present at the output of the fullwave rectifier then from eq. (12.12)

$$\text{d.c. voltage component} \rightarrow \frac{2V_m}{\pi}$$

$$\text{second harmonic} \rightarrow \frac{4V_m}{3\pi}$$

We can calculate I_{ac} as the current due to the second harmonic component of the input signal. Hence

$$I_{ac} = \frac{\frac{1}{\sqrt{2}}\left(\frac{4V_m}{3\pi}\right)}{\sqrt{(R^2 + R_i^2) + 4\omega^2 L^2}} = \frac{\frac{1}{\sqrt{2}}\left(\frac{4 \times 30}{3\pi}\right)}{\sqrt{(814)^2 + (2 \times 314)^2 . 100}}$$

$$= 1.422 \text{ mA}$$

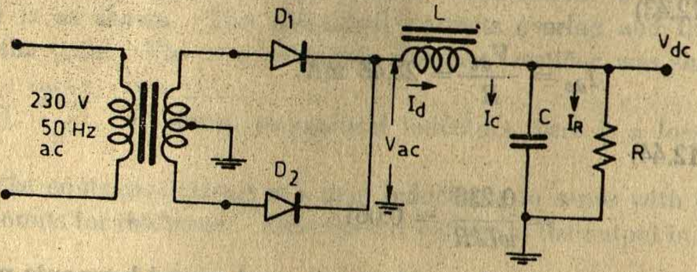
Hence ripple factor can also be calculated as

$$\gamma = \frac{I_{ac}}{I_{dc}} - \frac{1.422}{23.46} = 0.061$$

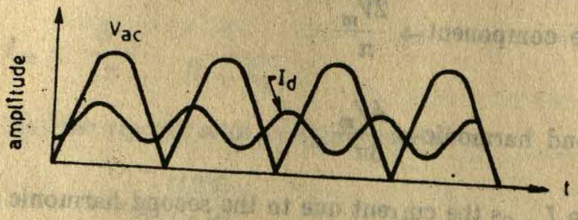
which agrees with the result quoted above.

12.4 LC Filters

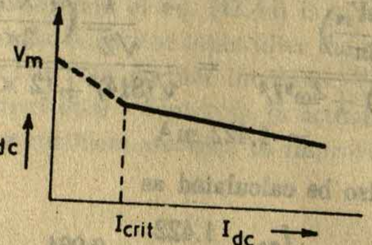
A capacitor input filter circuit has the disadvantage that the diode peaking current increases as the value of C is increased in order to reduce the ripple at a given load. The inductor input filter gives a lower output voltage but it reduces the peak currents through the diode rectifier. A combination of L and C eliminates the undersirable peak currents of the capacitor input filter and gives a very smooth output voltage. A fullwave rectifier with an LC filter is shown in Fig. 12.10. The inductor is in series and the capacitor is in shunt across the load. It is difficult to calculate the conduction angles etc. The behaviour of the circuit can be analysed in two parts. At low currents the effect of the inductor is negligible and the capacitor charges to the peak of the input voltage. The capacitor discharges



(a) Circuit diagram



(b) Waveform



(c) Voltage – current output

Fig. 12.10 Full wave rectifier with LC filter

to supply the load current. As the load current increases the voltage across the capacitor is reduced because of the larger discharge. For such low value of currents, the energy stored in the inductor is too small to matter. The conduction time may be slightly lengthened as the current increases.

As the current increases still further, the capacitor discharges still further but the inductor effect starts becoming noticeable. As explained in connection with inductor input filter, the current is maintained once the conduction angles of D_1 and D_2 overlap. The energy is stored in the magnetic field of the inductor and it supplies the current thoughout the cycle. The current flow under such conditions is shown in Fig. 12.10(b). The $I_{dc}-V_{dc}$ is shown in Fig. 12.10(c). The dotted curve indicates the fall in the output when the inductance effect is not predominant. Beyond a certain current I (critical), the inductor stores the energy and the current is continuous giving a voltage that is fairly constant with the load current.

As in the example of E12.3.1 the effect of various frequency components present at the input can be calculated individually and the total effect summed up. In the full wave rectifier, the eq. (12.12) shows that various frequency components are

$$d.c. \quad \frac{2V_m}{\pi}$$

$$2w \quad \frac{4V_m}{3\pi}$$

$$4w \quad \frac{4V_m}{15\pi}$$

If we neglected $4w$ and other higher frequency terms as negligible in comparison to *dc* and the second harmonic, then the ripple factor in the *LC* filter can be calculated easily. In the region where $I_{dc} < I_{critical}$ and the current is continuous in the inductor, we can further assume that $wL = X_L$ is much larger than X_c, and $X_c << R$. Also X_L is much larger than R and hence the only impedance in the circuit is X_L. It means that with all these assumptions we can write

$$v_{ac} = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2wt$$

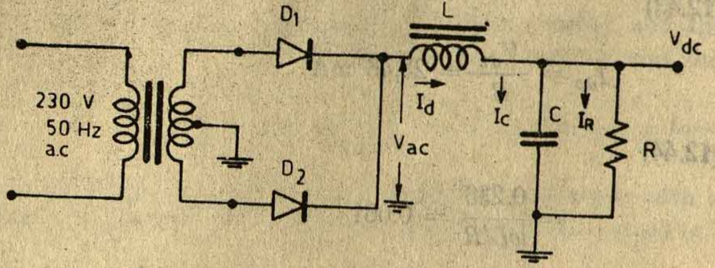
$$\text{and} \quad I_{ac} \approx \left(\frac{4V_m}{3\pi}\right) \frac{1}{\sqrt{2}} \frac{1}{X_L} \tag{12.45}$$

where I_{ac} is the r.m.s. current. Since $\frac{2V_m}{\pi}$ is the d.c. component V_{dc}, eq. (12.45) can be written as

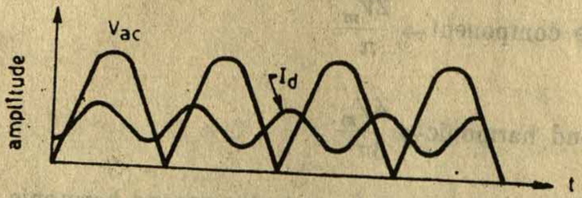
$$I_{ac} = \frac{\sqrt{2}.V_{dc}}{3} \frac{1}{X_L}$$

The d.c. term does not produce any drop across the inductor since it is assumed to be lossless. We have $X_c << R$, hence an approximation.

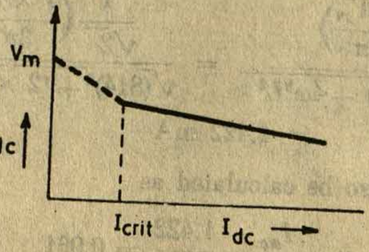
$$V_{ac} \approx I_{ac} \cdot X_c$$



(a) Circuit diagram



(b) Waveform



(c) Voltage – current output

Fig. 12.10 Full wave rectifier with LC filter

to supply the load current. As the load current increases the voltage across the capacitor is reduced because of the larger discharge. For such low value of currents, the energy stored in the inductor is too small to matter. The conduction time may be slightly lengthened as the current increases.

As the current increases still further, the capacitor discharges still further but the inductor effect starts becoming noticeable. As explained in connection with inductor input filter, the current is maintained once the conduction angles of D_1 and D_2 overlap. The energy is stored in the magnetic field of the inductor and it supplies the current thoughout the cycle. The current flow under such conditions is shown in Fig. 12.10(b). The $I_{dc}-V_{dc}$ is shown in Fig. 12.10(c). The dotted curve indicates the fall in the output when the inductance effect is not predominant. Beyond a certain current I (critical), the inductor stores the energy and the current is continuous giving a voltage that is fairly constant with the load current.

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$$2w \quad \frac{4V_m}{3\pi}$$

$$4w \quad \frac{4V_m}{15\pi}$$

If we neglected $4w$ and other higher frequency terms as negligible in comparison to dc and the second harmonic, then the ripple factor in the LC filter can be calculated easily. In the region where $I_{dc} < I_{critical}$ and the current is continuous in the inductor, we can further assume that $wL = X_L$ is much larger than X_c, and $X_c << R$. Also X_L is much larger than R and hence the only impedance in the circuit is X_L. It means that with all these assumptions we can write

$$v_{ac} = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2wt$$

$$\text{and} \qquad I_{ac} \approx \left(\frac{4V_m}{3\pi}\right) \quad \frac{1}{\sqrt{2}} \quad \frac{1}{X_L} \tag{12.45}$$

where I_{ac} is the r.m.s. current. Since $\frac{2V_m}{\pi}$ is the d.c. component V_{dc}, eq. (12.45) can be written as

$$I_{ac} = \frac{\sqrt{2}.V_{dc}}{3} \quad \frac{1}{X_L}$$

The d.c. term does not produce any drop across the inductor since it is assumed to be lossless. We have $X_c << R$, hence an approximation.

$$V_{ac} \approx I_{ac} . X_c$$

Therefore,
$$V_{ac} = \frac{\sqrt{2}.V_{dc}}{3} \quad \frac{X_c}{X_L} \tag{12.46}$$

From eq. (12.46), the ripple factor is calculated as

$$\gamma = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{2}}{3} \cdot \frac{1}{4w^2 LC} = \frac{0.471}{4\ w^2\ LC} \tag{12.47}$$

For a 50 Hz. supply,
$$\gamma = \frac{1.19 \times 10^{-6}}{LC} \tag{12.48}$$

This shows that the ripple factor is quite small for moderate values of L and C in an actual circuit. We have assumed that there are two components in v_{ac} — the d.c. and the second harmonic component. The critical current, $I_{critical}$, beyond which the current in the inductor becomes continuous, occurs when the peak a.c. current is equal to I_{dc}. The I_{dc} is contributed by the d.c. component and the peak a.c. current by the second harmonic component of the input v_{ac}. Therefore

$$\frac{2\ V_m}{R.\ \pi} = \frac{4\ V_m}{3\ \pi\ (X_L)\ 2w} = \frac{4\ V_m}{3\ \pi\ (2wL)} \tag{12.49}$$

where the impedance of the filter circuit has been assumed to be dominated by the X_L. As mentioned earlier it is assumed that $X_L \gg X_C$, $X_C \ll R$ and $X_L \gg R$. From eq. (12.49) we obtain

$$R = 3\ wL \tag{12.50}$$

or
$$L = \frac{R}{3w} \approx R \times 10^{-3} \tag{12.51}$$

This is the critical value of the inductor. For a given load R, the inductor must be larger than the value given in eq. (12.51). Now

$$I_{dc} = \frac{2\ V_m}{\pi R}$$

From eq. (12.50) at the critical point, $I_{critical}$ is obtained by substituting for R

$$I_{critical} = \frac{2\ V_m}{(3\ wL)}$$

$$I_{critical} = \frac{0.212\ V_m}{wL} \tag{12.52}$$

We must ensure that at least this current flows in the circuit all the time. A standard method is to connect a resistance across the capacitor as a bleeder resistance. Even with no load, a fixed current ($I_{critical}$) is drawn from the circuit, to stabilise the operation. As and when the load current is drawn, the circuit supplies the current.

Example 12.4

In a full wave rectifier circuit using an LC filter, it is given that $L = 10\ H$, $C = 100\ \mu F$ and $R = 500$ Ohms. Calculate the I_{dc}, $I_{critical}$, I_{ac}, V_{ac}, V_{dc} and ripple factor if $V_m = 30\ V$.

$$X_L = 2wL = 2 \times 314 \times 10 = 6.28\,K \text{ Ohms.}$$

$$X_C = \frac{1}{2wC} = \frac{1}{314 \times 100 \times 10^{-6}} = 15.9 \text{ Ohms.}$$

Hence $X_L \gg X_c$

and $X_c \ll R$

as the required assumption for the simple analysis.

$$V_{dc} = \frac{2V_m}{\pi} = \frac{60}{\pi} = -\ 19.09 \text{ volts.}$$

$$I_{dc} = \frac{V_{dc}}{R} = 38.2 \text{ mA}$$

From eq. (12.45) $$I_{ac} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L} = \frac{\sqrt{2}}{3} \cdot \frac{19.09}{2 \times 3.14 \times 10^{-3}}$$

$$= 1.43 \times 10^{-3}$$

$$V_{ac} = I_{ac} \cdot X_c = 1.43 \times 10^{-3} \times 15.9$$

$$= 22.7 \text{ mV.}$$

hence $$\gamma = \frac{V_{ac}}{V_{dc}} = \frac{22.7 \times 10^{-3}}{19.09} = 1.19 \times 10^{-3} = .00119$$

D.C. power output $= V_{dc} \cdot I_{dc} = 19.09 \times 38.2 = 729.24$ mW.

From eq. (12.52).

$$I_{critical} = \frac{0.212 \times 30}{314 \times 10} = 2.025 \text{ mA.}$$

It will be necessary to connect a bleeder resistance of value less than $\frac{19.09}{2.025} =$ 9.43 K Ohm across the output.

12.4.1 CLC FILTER

A capacitor input LC filter has the configuration shown in Fig. 12.11. Since the capacitor C_1 is at the input of this filter, the output voltage V_o is higher than that of the LC filter of the previous section. The output voltage may approach V_m for low currents. The ripple factor is also small. However, for large load currents, i.e. small R, the capacitor C_1 discharges and the output voltage falls. A large value of C_1 is desirable if this is to be avoided. Now the peak surge current through the diodes of the rectifier will be very large for a large C_1. Hence this type of filter is suitable for low load current applications like home rectifiers etc. and for rectifiers using semiconductor diodes where the peak currents are not a problem. The ripple increases with the load current unlike the LC filter where the ripple is independent of the load.

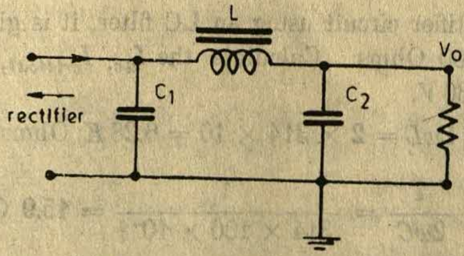


Fig. 12.11 CLC Filter

12.5 Bridge Rectifier

A bridge rectifier circuit is shown in Fig. 12.12. As the name suggests the four diodes are connected in a bridge and circuit is a full wave rectifier. One of the main features of the bridge rectifier is that it does not require a centre tap transformer. On the positive half of the cycle, the current flows from A through D_1, R, D_2 and back to B. During the negative half cycle the current flows from B through D_3, R, D_4 and back to A. The current through the load R is in the same direction during the two half cycles. The CLC filter has been shown as an illustration only. When D_1 and D_2 conduct the diodes D_3 and D_4 are reverse biased and vice-versa. The peak inverse voltage across the diode is V_m only whereas it was $2V_m$ in the full wave rectifier circuit. The current flows all the time in the secondary of the transformer of the bridge rectifier, as against the full wave rectifier where the current flows half the time in each winding of the centre-tapped transformer. The current rating of the transformer in the bridge rectifier is thus about

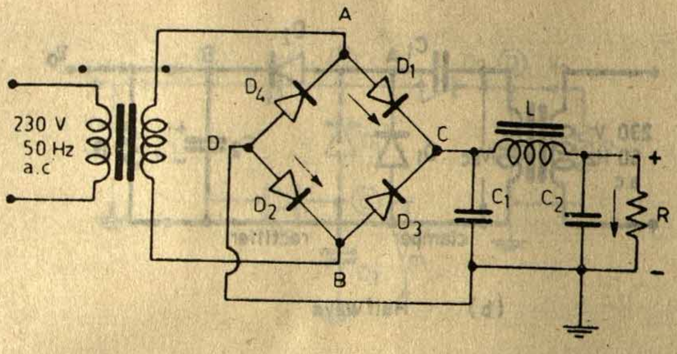
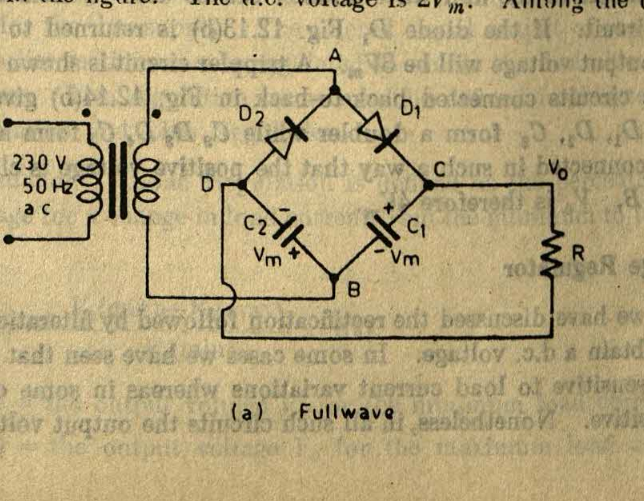


Fig. 12.12 Bridge Rectifier

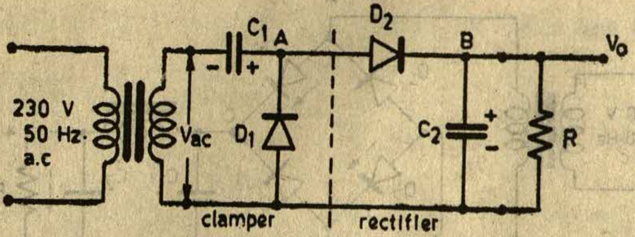
2/3 of the rating of the same transformer in the full wave circuit. It other words, a larger transformer of larger ratings will be used in the bridge circuit for the same rectifier load current specifications.

12.5.1 VOLTAGE DOUBLERS

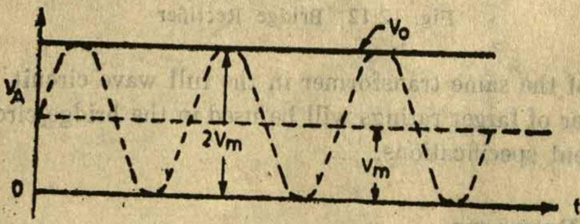
For the same transformer ratings the d.c. output may be doubled by using a voltage doubler shown in Fig. 12.13. Such circuits are useful only when the load current is very small. Consider the circuit of Fig. 12.13(a) called the full wave voltage doubler. During the positive half cycle the capacitor C_1 gets charged to V_m as shown. Similarly during the negative half cycle the capacitor C_2 is charged to V_m. The voltage across the points CD where the load R is connected is thus $2V_m$. The doubler in Fig. 12.13(b) can be analysed as a clamper followed by a half wave rectifier. Thus, C_1 and D_2 behave like a clamper wherein the voltage at the point A is clamped to zero and cannot become negative. The voltage V_{ac} is $V_m \sin \omega t$ as shown in Fig. 12.12(c). After the clamper, the voltage V_A is a sine wave with V_m as the average value. The rectifier D_2 and the capacitor C_2 produce V_0 shown dotted in the figure. The d.c. voltage is $2V_m$. Among the two doubler



(a) Fullwave



(b) Half wave



(c) Waveforms for (b)

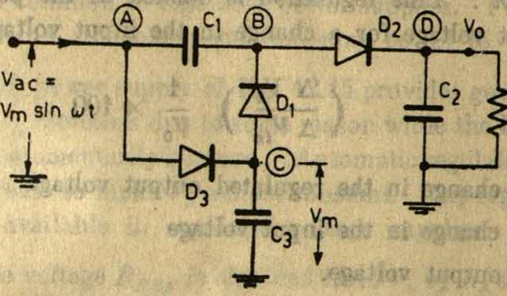
Fig. 12.13 Voltage Doublers

circuits shown, the full wave circuit has the advantage that the ripple frequency is twice the supply frequency, and the maximum voltage across each capacitor is only V_m. Filtering is therefore easier. In the half wave circuit, the ripple frequency is same as the supply frequency and the voltage across C_2 is $2V_m$. Regulation of the full wave doubler is much better than that of the half wave one. One disadvantage of the full wave circuit is that there is no common ground point between the transformer and load.

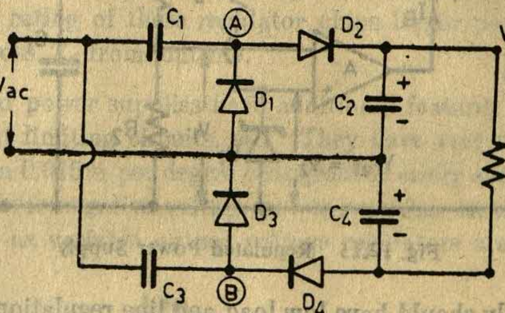
The principle of the half wave doubler can be used to make a trippler and a quadrupler circuit. If the diode D_1 Fig. 12.13(b) is returned to V_m instead of ground, the output voltage will be $3V_m$. A trippler circuit is shown in Fig. 12.14(a) Two doubler circuits connected back-to-back in Fig. 12.14(b) give a quadrupler circuit. C_1, D_1, D_2, C_2 form a doubler while C_3 D_3 D_4 C_4 form another doubler but with D_3 connected in such a way that the positive voltage is clampled to zero at the point B. V_0 is therefore $4V_m$.

12.6 Voltage Regulator

So far we have discussed the rectification followed by filteration of a.c. signal in order to obtain a d.c. voltage. In some cases we have seen that the output voltage is very sensitive to load current variations whereas in some other circuits it is not so sensitive. Nonetheless, in all such circuits the output voltage is not cons-



(a) Trippler



(b) Quadrupler

Fig. 12.14 Voltage Multiplying Circuits

tant for load current or input voltage variations. In almost all applications of electronic circuits using transistors or IC circuits it is important to have a constant voltage source for the d.c. supply. The filtered signal output of the rectifiers discussed in the earlier sections can be regulated to obtain the desirable characteristic of the d.c. source. Two regulation terms need be defined in this context. They are Load Regulation and Line Regulation.

Load Regulation : Load Regulation is defined as the percentage change in the output voltage for a change in load current from the minimum to the maximum. Thus

$$\text{Load regulation (percentage)} = \frac{V_0(\text{min}) - V_0(\text{max})}{V_0(\text{min})} \times 100 \tag{12.53}$$

where V_0 (min) = the output voltage V_0 for the minimum load current

V_0 (max) = the output voltage V_0 for the maximum load current.

Line Regulation : Line regulation is defined as the percentage change in the regulated output voltage for a change in the input voltage.

$$\text{line regulation} = \left(\frac{\Delta V_0}{\Delta V_{in}}\right) \frac{1}{V_0} \times 100 \qquad (12.54)$$

where ΔV_0 = change in the regulated output voltage

ΔV_{in} = change in the input voltage

V_0 = output voltage.

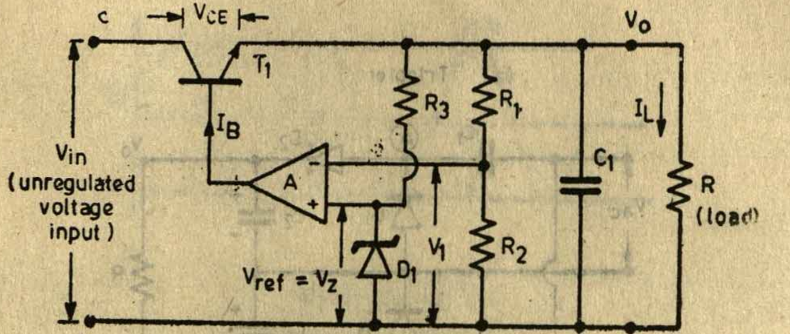


Fig. 12.15 Regulated Power Supply

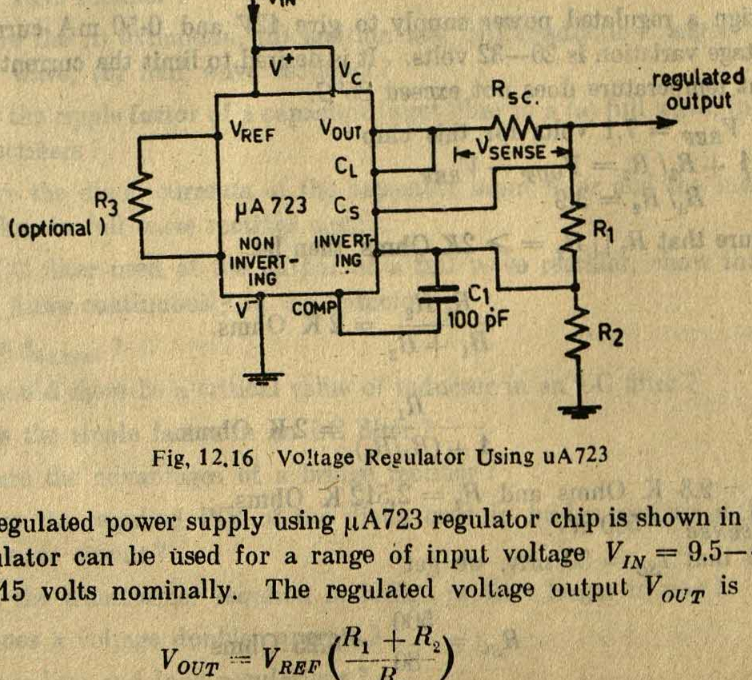
A good power supply should have low load and line regulations. The basic circuit diagram of an automatic voltage regulator is shown in Fig. 12.15. The series transistor T_1 controls the output voltage V_0 which is the difference of V_{in} and the drop V_{CE} across the transistor. The drop V_{CE} is controlled by the base current I_B. Thus T_1 behaves like a variable resistor and any change of voltage is absorbed by it as a change of its resistor value. The output voltage V_0 is sensed by a voltage divider consisting of R_1 and R_2. The voltage V_1 is compared with a voltage reference source V_{REF} and the error is amplified by an error amplifier A. The output of the amplifier drives the base current I_B.

Let us assume that the load current I_L increases due to some reason. A large load current will mean that the voltage V_0 drops from its normal value. The voltage V_1 will thus momentarily reduce. Since $V_{ref} = V_z$ remains constant, the output of the error amplifier A goes positive or higher because of the polarity of the connection. The sense signal V_1 is connected to the Inverting input of the error amplifier. The curent I_B will therefore increase, resulting in a smaller V_{CE} drop across T_1. The smaller V_{CE} will compensate for the fall in V_o and hence the voltage is restored to its original value. Similarly if V_o increases, V_1 increases and the output of the error amplifier reduces, reducing I_B and hence increasing V_{CE}. This will mean that the change in V_o will be restored. Thus we see that V_o is regulated against load current variations. Load regulation of 0.05% for small current variations is quite common in regulated power supplies. For larger current variations like 1 to 50 mA, the load regulation may be 0.1 to 0.2%.

The regulated power supply of Fig. 12.15 provides good line regulation also. For example, if V_{in} increases due to some reason while the load current I_L is constant then V_o will momentarily increase. Automatic regulation will occur and the drop V_{CB} will increase to make V_o almost constant. Line regulation of 0.1 to 0.5% of V_o is easily available in regulated voltage supplies.

The reference voltage R_{REF} is obtained from V_o by R_3 and zener diode combination. For larger current I_L, number of series transistors may be connected in parallel to handle the total current. The error amplifier, the series transistor and V_{REF} source are available in a chip form for moderate currents of 50—100 mA. Many regulator chips with different ratings are available in the market. To increase the current rating of these regulator chips larger power series transistors are connected across T_1 from outside.

The regulated power supplies have additional features like short circuit protection and current limiting circuits, etc. They have very low temperature drifts and a drift less than 0.015% per degree centigrade is easily available. The regulator works equally well for negative voltage power supplies. In the IC chip regulators, both fixed as well as variable output voltage regulators are available.



Fig, 12.16 Voltage Regulator Using uA723

A regulated power supply using μA723 regulator chip is shown in Fig. 12.16. This regulator can be used for a range of input voltage $V_{IN} = 9.5—40$V. The $V_{REF}=7.15$ volts nominally. The regulated voltage output V_{OUT} is

$$V_{OUT} = V_{REF}\left(\frac{R_1 + R_2}{R_2}\right) \tag{12.55}$$

The current limit resistor R_{SC} is calculated from

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}$$

where I_{SC} is the short circuit current
and V_{SENSE} = sense voltage across the R_{SC}
specified by the manufacturer.

The voltage V_{SENSE} is temperature dependent. If the maximum ambient temperature is say $+85°C$, then V_{SENSE} is $= 500$ mV. Chart is available for V_{SENSE} vs. Temperature for the μA723 chip. The higher limit of $85°C$ is adequate for most applications.

The resistance R_3 is optional but its value, if used, can be fixed as the parallel combination of R_1 and R_2 i.e.

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

While making a power supply with this chip care should be taken to see that the impedance at the INVERTING or other terminals is greater than 2K Ohms. This chip can be used for a maximum load current of 150 mA without any external series transistor.

Example 12.6.1

Design a regulated power supply to give $12V$ and 0-50 mA current. The input voltage variation is 20—32 volts. It is desired to limit the current to 80 mA if ambient temperature does not exceed $85°C$.

Let $V_{REF} = 7.1$ volts for this chip
Now $1 + R_1/R_2 = V_{OUT} - V_{REF}$
therefore $R_1/R_2 = 3.9$
If we ensure that $R_1 \,||\, R_2 = \geqslant 2K$ Ohms, then let

$$\frac{R_1 R_2}{R_1 + R_2} = 2\text{ K Ohms.}$$

or

$$\frac{R_1}{1 + (R_1/R_2)} = 2\text{ K Ohms.}$$

hence $R_1 = 9.8$ K Ohms and $R_2 = 2.512$ K Ohms.
Taking $V_{SENSE} = 500$ mV.
and given that $I_{SC} = 80$ mA, we get

$$R_{SC} = \frac{500}{80} = 6.25\text{ Ohms}$$

and $R_3 = 2$ K Ohms for minimum temperature drift.
The values of R_1, R_2, R_3 and R_{SC} can be connected as in Fig. 12.16 to obtain the desired regulated power supply. The load regulation (max) specified by the manufacturer is 0.2% of V_{OUT} from 1 to 50 mA. Similarly the line regulation is 0.5% of V_{OUT} (12-40V.). The temperature coefficient is 0.015% per degree centigrade.

A good rule of thumb for the design of the regulators is to keep the current coming out of the V_{REF} terminal equal to 1 mA. This will mean that $R_1 \| R_2 = 7.1$ K Ohms.

Review Questions

12.1 Why is the ripple factor of the half wave rectifier higher than that of the full-wave rectifier ?

12.2 What are the frequency terms present at the output of the half wave rectifier ?

12.3 What is the required PIV of the diode in the half wave rectifier ?

12.4 What are the frequency terms present at the output of the full wave rectifier ?

12.5 What is the ripple factor of the fullwave rectifier ?

12.6 What is the effect of putting a large capacitor at the output of (i) half wave, (ii) full wave rectifier ?

12.7 What are the (i) extinction, (ii) ignition and (iii) conduction angles in a (a) full wave, (b) half wave rectifiers ?

12.8 What is the ripple factor of a capacitor input filter in a (a) full wave, (b) half wave rectifiers ?

12.9 Compare the diode currents of the capacitor input filter and the inductor input filter in full wave rectifier circuit.

12.10 In an LC filter used at the output of a full wave rectifier, show that the current flows continuously in the inductor.

12.11 What is $I_{critical}$?

12.12 Why should there be a critical value of inductor in an LC filter ?

12.13 What is the ripple factor in an LC filter ?

12.14 What are the advantages of a bridge rectifier ?

12.15 Compare the required PIV of the diode used in bridge rectifier with that in full wave circuit ?

12.16 Why is the transformer required in bridge rectifier larger in size ?

12.17 How does a voltage doubler operate ?

12.18 What are line and load regulations ?

12.19 What is the function of the error amplifier in the automatic voltage regulator ?

12.20 What is the function of the current limit in the voltage regulator ?

Problems

P.12.1 In a half wave rectifier with 30 V, 50 Hz. signal input find V_{dc}, I_{dc}, I_{rms}, ripple factor and efficiency if the load R is 100 Ohms. What is the PIV of the diode required ?

P.12.2 Repeat Problem 12.1 for a full wave rectifier. Compare the performance of the two circuits.

P.12.3 In a capacitor input full wave rectifier circuit, the transformer secondary has 15-0-15V rating and the load resistance is 6.4 Ohms. The capacitor used is 5000 μf. Find V_{dc}, I_{dc}, ripple factor and the power input and output of this supply (hint : You have to find I_{rms} for calculating the power input which is $I_{rms}^2 \times R$).

P.12.4 Repeat the problem 12.3 for a half wave rectifier. What are the peak currents in the diodes in the two cases ?

P.12.5 In Problem 12.3, if the load is changed to 12.8 Ohms with everything else remaining the same then what will be the load regulation ?

P.12.6 A full wave rectifier uses an LC filter with the following specifications. The transformer secondary has 15-0-15V. rating, the load $R = 6.4$ Ohms, $C = 500\ \mu F$. Find the minimum value of the inductor required and select a suitable value to obtain a ripple less than 0.01 volt. Find V_{dc}, I_{dc}, I_{ac} and $I_{critical}$. What is the bleeder resistor required ?

P.12.7 An inductor input filter is used in a fullwave rectifier circuit. The $V_{ac} = 30\ V.$, 50 Hz. and $R = 50$ Ohms. Find the value of L to have a ripple of less than 0.02 volts. What is the V_{dc}, I_{dc} and power output of this supply.

P.12.8 In the voltage doubler of Fig. 12.13(b), estimate the values of C_1 and C_2 if $V_{ac} = 10{,}000 \sin 2\pi \times 40 \times 10^3 \times t$. What is the PIV of the diodes used ? Assume $R = 1$ Mohm.

P.12.9 Sketch the waveform in the voltage tripler circuit of Fig. 12.14(a) at the points A, B, C and D.

P.12.10 In the voltage regulator using $\mu A723$ chip, the output voltage required is + 15 volts with $V_{IN} = 22\text{-}30$ volts. The maximum current desired is 30 mA with a current limit of 50 mA. The ambient temperature is 85° C. Select values of R_1, R_2, R_3 and R_{SC} in Fig. 12.16.

APPENDIX 'A'

Laboratory Experiments

Eight experiments have been suggested here as a supplement to the theory course on Basic Electronics. Depending upon the time available and the level of the students concerned they may complete the whole experiment or may do a part only.

The first two experiments are meant to familiarise the student with the electronic devices, components and general laboratory instruments. For example, in experiment 1, it is expected that the Laboratory Instructor will arrange a display of all the components and devices mentioned and explain the details of the various items. Only the topics are mentioned here and the details are left for the Instructors to fill in. Similarly, in experiment 2, the instruments mentioned are to be demonstrated and the details given to the students. Towards the end, the students should be allowed to use the oscilloscope and measure various waveforms etc.

From experience it has been found that though the transistor amplifier is the basic amplifier circuit, the students find it extremely difficult to start with. With the modern trend of using OP-AMPS as the basic amplifier in a black box it is also convenient to start the amplification idea with OP-AMPS and take up transistor amplifier at the end.

The students find the logic circuits and the digital experiments very interesting and stimulating. Since they do not have any earlier exposure to these ideas we have found it expedient to give a one-hour lecture/demonstration before the experiment is started.

EXPERIMENT NO. 1

Components and Devices

Aim : Familiarization with components and devices used in Electronic circuits and systems.

1. Resistances :
   - (i) Range or values
   - (ii) Types like wirewound, carbon film, metal film, etc.
   - (iii) Stability
   - (iv) Accuracy
   - (v) Percentage tolerance
   - (vi) Wattage — power dissipation
   - (vii) Colour code.
2. Variable Resistances—Potentiometers :
   - (i) Range of values
   - (ii) Types like wirewound, carbon film, etc.
   - (iii) Tubular preset, rotary, helical, etc.
   - (iv) Linear and logarithmic
   - (v) Wattage
   - (vi) Accuracy.
3. Capacitances :
   - (i) Range of values
   - (ii) Types like air, paper, ceramic, mica, polysterene, foil, electrolytic, etc.
   - (iii) Accuracy
   - (iv) Percentage tolerance
   - (v) Voltage rating
   - (vi) Shape — disc, tubular, ganged
   - (vii) Padders and trimmers.
4. Inductances :
   - (i) Range of values
   - (ii) Core — air core, ferrite core, etc.
   - (iii) Chokes
   - (iv) Q values
   - (v) Variable inductance—variable core.
5. Transformers :
   - (i) Power transformer—ratings
   - (ii) Audio transformer
   - (iii) r. f. transformer, core materials
   - (iv) Pulse transformer

6. Diodes :
   - (i) Vacuum diodes—ratings
   - (ii) Semiconductor diodes—germanium, silicon ; ratings.
   - (iii) Selenium rectifiers
   - (iv) Power diodes—ratings
   - (v) R. F. diodes
   - (vi) LED
   - (vii) Photodiode, tunnel diode, etc.

7. Transistors :
   - (i) BJT — germanium, silicon ; ratings.
   - (ii) Frequency of operation
   - (iii) FET — ratings

8. Tubes :
   - (i) Triodes—ratings
   - (ii) Pentodes—ratings
   - (iii) Power tubes.

9. I. C. Circuits :
   - (i) NAND GATE 7400
   - (ii) Op-Amp. 741
   - (iii) Regulator Chip 723
   - (iv) Flip-Flop
   - (v) Timers NE 555, etc.

10. CRT :
    - (i) Size—ratings
    - (ii) Persistence
    - (iii) Colour of the screen
    - (iv) Sensitivity, etc.

EXPERIMENT NO. 2

Laboratory Instruments

Aim : Familiarization with Laboratory Instruments.

1. Multimeter :
   - (i) Range of measurements, frequency, etc.

- (ii) No. of functions
- (iii) Input impedance and sensitivity
- (iv) Analogue and digital display.

2. **Audio Oscillator :**
   - (i) Range of frequency
   - (ii) Output voltage and impedance level
   - (iii) Accuracy and stability.

3. **Waveform Generators :**
   - (i) Type of waveforms generated
   - (ii) Range of operation
   - (iii) Output voltage and impedance level
   - (iv) Linearity and stability.

4. **Pulse Generators :**
   - (i) Range of operation, frequency
   - (ii) Minimum pulse width generated
   - (iii) Output voltage and impedance levels
   - (iv) Stability and accuracy.

5. **Voltmeters :**
   - (i) Digital voltmeters and vacuum tube voltmeters.
   - (ii) Range of measurements
   - (iii) Frequency of operation
   - (iv) Input impedance
   - (v) Stability and accuracy
   - (vi) R. M. S. and average value reading instruments
   - (vii) D.C. voltage measurement.

6. **Oscilloscopes :**
   - (i) Single beam and double beam/trace oscilloscopes
   - (ii) Sensitivity and bandwidth of the vertical amplifier
   - (iii) Trigger and synchronization
   - (iv) Calibration of time and amplitude
   - (v) Various measurement functions.

EXPERIMENT NO. 3

Operational Amplifier

Aim :

(1) To measure the voltage gain, the frequency response, the input impedance and the output impedance of (a) Inverting amplifier (b) Non-inverting amplifier, using an Op-Amp.

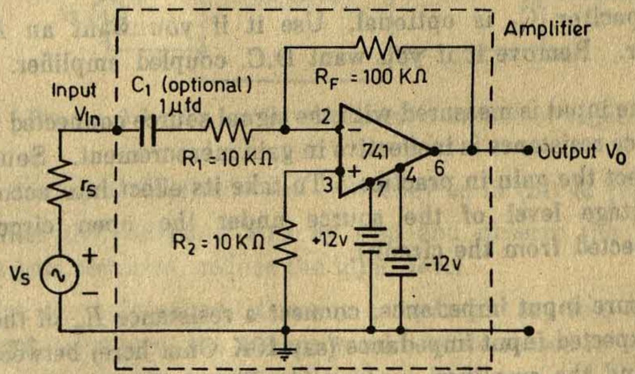
(2) To use the Op-Amp. as a summer.

(3) To measure the input impedance and the voltage gain of a voltage follower.

(4) To use the Op-Amp. as (a) a differentiator and (b) an integrator.

Procedure .

(1) (a) *Inverting amplifier :*



Pin nos. 1 and 5 → off-set null
8 → no connection

Fig. A 3.1 : Inverting Amplifier.

(i) Connect the amplifier as shown in Fig. A 3.1.

(ii) Measure d.c. voltages at all the pins of the op-amp by preferably a digital voltmeter (high input impedance).

(iii) Connect a signal source at the input terminals setting the frequency at say 1 KHz and output to zero.

(iv) Connect an oscilloscope at the output terminal and observe the output by increasing the signal input slowly. The output signal will start increasing in amplitude and would finally be distorted beyond a certain input level. Don't increase the input any more and measure the input signal by an electronic millivoltmeter.

(v) Set the input level to a value much smaller than the one measured in (iii). Observe the output and input waveforms. Ensure no distortion at the output.

(vi) Measure the output and input voltage levels using CRO as well as electronic voltmeter. Calculate the gain and compare with the theoretical value. Measure the phase difference between output and input signals.

(vii) Change the signal frequency from say 10 Hz to 1 MHz in steps keeping the input level fixed as above. Suggested steps are 10, 20, 50, 100, 200, 500, 1000, 2000, 5000, 10K, 20K, 50K, 100K, 200K, 500K and 1 M Hz. Measure and tabulate gain at each of these frequencies observing the output in scope every time. Note any distortion. Plot gain in dB versus the frequency on a semilog (5 cycles) graph paper. Mark and note down the 3 dB frequencies and obtain the bandwidth of the amplifier. Compare the experimental results with the theoretical ones.

(viii) The capacitor C_1 is optional. Use it if you want an A.C. coupled amplifier. Remove it if you want D.C. coupled amplifier.

(ix) When the input is measured with the signal source connected in the circuit, the source resistance is ineffective in gain measurement. Source resistance does affect the gain in practice. To take its effect into account, measure the voltage level of the source under the open circuit condition (disconnected from the circuit).

(x) To measure input impedance, connect a resistance R_x of the same order as the expected input impedance (say 10K Ohm here) between the signal source and the amplifier as shown in Fig. A 3.2.

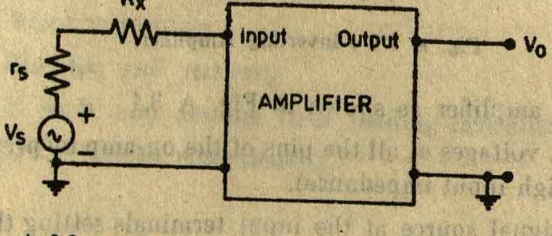


Fig. A 3.2 : Set up for measurement of Input Impedance.

(xi) Set the amplitude of the signal source at twice the value and the frequency at the same value as in (v) and (iii) respectively.

(xii) Observe the output with and without R_x in circuit and ensure no distortion by reducing the input level if necessary.

(xiii) Measure the output without R_x in the circuit. Call it V_{01}. Measure the output with R_x in the circuit. Call it V_{02}. Calculate the R_{in} by

$$R_{in} = \frac{R_X}{\frac{V_{01}}{V_{02}} - 1}$$

(xiv) Prove the formula in (xiii). Remember that R_1 is part of the amplifier.

(xv) To measure the output impedance connect a variable resistance (decade resistance) box across the output terminals through a large capacitor (say 100 Mfd) as shown in Fig. A 3.3. Keep high resistance initially.

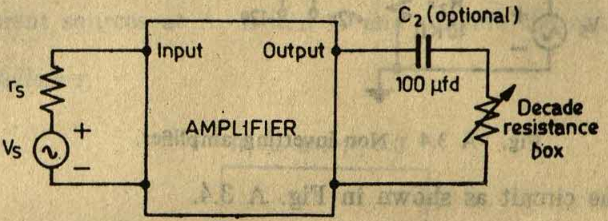


Fig. A 3.3 : Set up for measurement of Output Impedance.

(xvi) Set the input amplitude and frequency as in (iii) & (v).

(xvii) Reduce the resistance step by step and observe the output waveform. If it gets distorted, reduce the input level.

(xviii) When the external resistance is comparable say less than ten times the output resistance, the output would be decreased in amplitude. Avoid any distortion by reducing the input level.

(xix) At this point measure the output V_{01} without the external resistance.

(xx) Then connect the external resistance as arrived at (xviii) and measure the output V_{02}. The output resistance R_0 is given by

$$R_o = \left(\frac{V_{01}}{V_{02}} - 1\right) R_x$$

R_x is the value of the external resistance. Derive the formula.

(xxi) The capacitor should be large so that there is practically no signal voltage drop across it at the test frequency. Since the resistances are small, the capacitor has to be very large. Test frequency may also be increased within the bandwidth.

(xxii) If the output signal level does not reduce with the smallest resistance connected, the output impedance is much smaller than the external resistance.

(xxiii) You can change the gain of the amplifier by either changing, R_F or R_1 or both. Try.

1. (b) *Non-inverting Amplifier.*

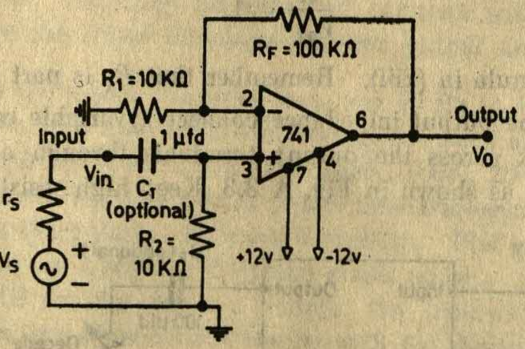


Fig. A 3.4 : Non-inverting amplifier.

(i) Connect the circuit as shown in Fig. A 3.4.

(ii) Repeat steps (ii) to (ix) of 1 (a).

(iii) To measure input impedance repeat steps (x) to (xiii).
The input impedance of an operational amplifier in the non-inverting mode is quite large. When a resistance R_2 is connected from non-inverting terminal to ground for the purpose of providing a dc. bias path, the input impedance would be approximately R_2. To obtain large input impedance, a large R_2 is connected.

(iv) To measure output impedance, repeat steps (xv) to (xxii) in 1 (a).

2. *Summing Amplifier*

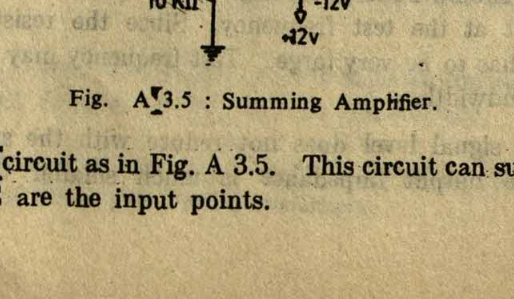


Fig. A 3.5 : Summing Amplifier.

(i) Connect the circuit as in Fig. A 3.5. This circuit can sum up three signals. A, B and C are the input points.

(ii) Connect a signal source at A setting it at a convenient frequency say I KHz and small output. Observe and measure the signal level at the output of the amplifier. There should be no distortion.

(iii) Repeat step (ii) above by connecting signal generators at inputs B and C.

(iv) Connect the same signal at A and B simultaneously. Observe the output. It should not be distorted. Measure the output and compare with that in (ii) and (iii) above. Observe the phase of the output signal with respect to the input signal.

(v) Repeat step (iv) above by connecting the same signal at inputs A, B and C simultaneously.

(vi) Try different sources at A, B and C and observe the output.

3. *Voltage follower.*

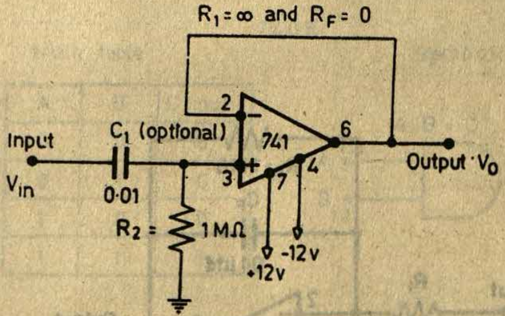


Fig. A 3.6 : Voltage follower.

(i) Connect the circuit as shown in Fig. A 3.6.

(ii) Repeat steps (ii) through (vi) of 1 (a).

(iii) Increase the input signal level and find the limit when the output is distorted.

(iv) To measure input impedance, repeat steps (x) to (xiv) of 1 (a).

(v) To measure output impedance, repeat steps (xv) to (xvii) of 1(a).

4. (a) *Differentiator and* (b) *Integrator*

(i) Connect the circuits as shown in Fig. A 3.7 (a) and (b).

(ii) Measure the d.c. voltages at every point.

(iii) Connect small level sinusoidal signal say at a frequency of 1 KHz at the input terminal. Observe the output waveform on CRO and measure the output amplitude and phase.

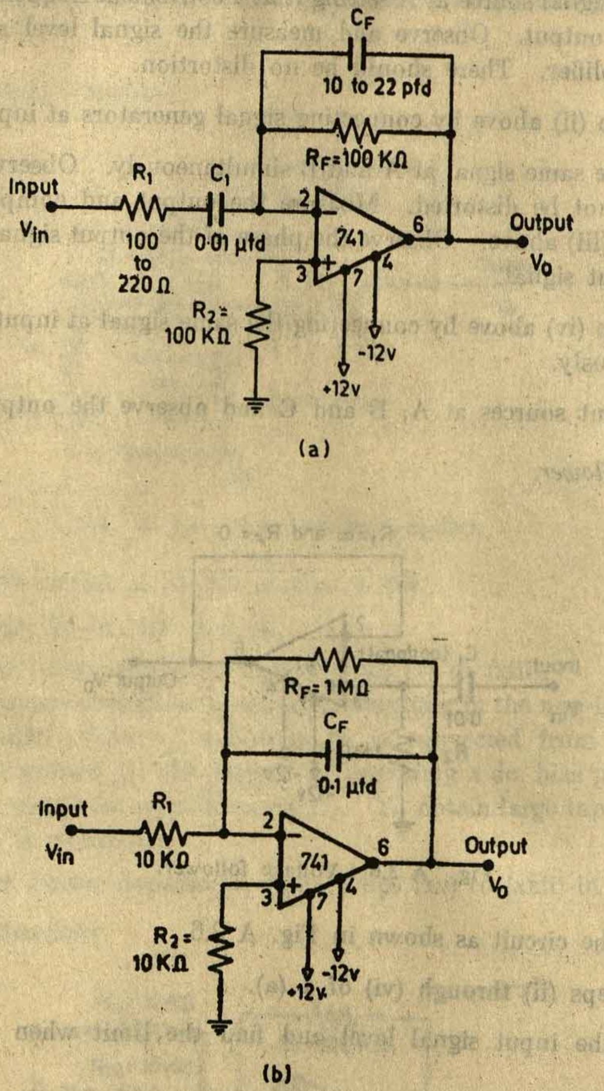


Fig. A 3.7 (a) : Differentiater and (b) integrater.

(iv) Mathematically differentiate and integrate a sinusoidal function say, A sin ωt. and compare the results with the experimental observation as made in (iii) above.

(v) Apply a 1 KHz square wave or pulse train of small amplitude to the input. Observe the output waveform and measure its amplitude. Compare your results with what you would obtain by mathematical differentiation and integration of a square or pulse train,

EXPERIMENT NO. 4

Logic Gates

Aim : Verify the truth table of LOGIC GATES like AND, OR, NOT, NAND, NOR, EX-OR.

(1) AND : The truth table and symbol of a logic AND gate are shown in Fig. A4.1.

Note : The truth table can be verified by connecting either zero volts (logic 0) or five volts (logic 1) to the inputs A (pin 1) and B (pin 2) and observing the output C at pin 3. Thus if 5 volts (1) is connected to A input and zero volts (0) to the B input, the output will be Low (0) and so on. When 5 volts input is given to both A AND B, the output is 5 volts (1).

7408

truth table

A	B	C = out
0	0	0
0	1	0
1	0	0
1	1	1

symbol

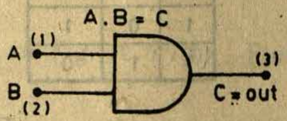


Fig. A 4.1

(2) OR : The truth table and symbol of a logic OR Gate are shown in Fig. A4.2.

7432

truth table

A	B	C = out
0	0	0
0	1	1
1	0	1
1	1	1

symbol

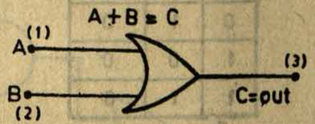


Fig. A 4.2

(3) NOT ; The truth table and symbol of a NOT circuit are shown in Fig. A 4.3. NOT can be easily realised by a NAND or NOR Gate.

7404

truth table

A	C=out
0	1
1	0

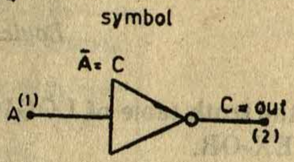


Fig. A 4.3

(4) NAND : The truth table and symbol of a NAND Gate are shown in Fig. A 4.4.

Note : Any input being 0 the output is 1.

7400

truth table

A	B	C=out
0	0	1
0	1	1
1	0	1
1	1	0

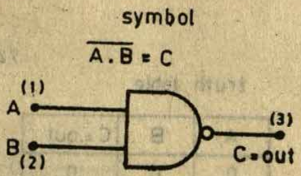


Fig. A 4.4

(5) NOR : The truth table and symbol of a NOR Gate are shown in Fig. A 4.5.

Note : Any input being 1 the output is 0.

7402

truth table

A	B	C=out
0	0	1
0	1	0
1	0	0
1	1	0

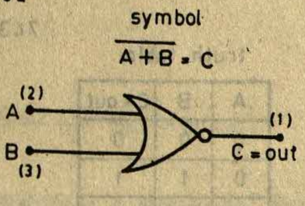


Fig. A 4.5

(6) EX-OR : The truth table and symbol of a EX-OR Gate are shown in Fig. A 4.6. Though an EX-OR chip 7486 is available, the EX-OR gate can be made using NAND/NOR gates only or a combination of gates can be used.

7486

truth table

A	B	C= out
0	0	0
0	1	1
1	0	1
1	1	0

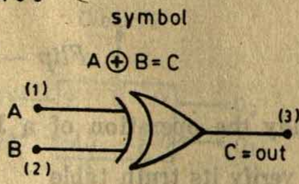


Fig. A 4.6

Exercise 1 : Realise a EX-OR gate using NAND gates only.

Exercise 2 : Realise a EX-OR gate using other gate circuits.

$$\overline{A}\cdot B + A\cdot\overline{B} = C$$

Exercise 3 : What is the action of the circuit connected as shown in Fig. A 4.7(a) ? Wire two NAND gates as in the circuit and find its truth table.

Exercise 4 : A latch circuit is shown in Fig. A 4.7(b). Find its truth table.

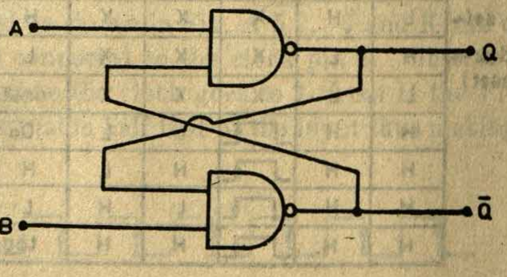


Fig. A 4.7(a)

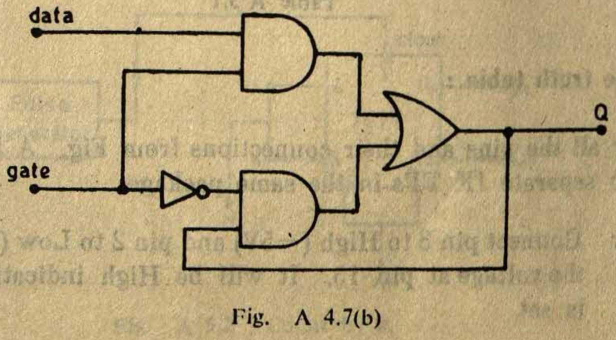


Fig. A 4.7(b)

EXPERIMENT NO. 5

Flip —Flops

Aim : To study the operation of a JK Master-slave Flip-Flop and to :

(i) verify its truth table

(ii) use it as a counter

(iii) use it as a shift register

Note : 7476 is a typical JK Master-Slave Flip-Flop (FF) with "Preset" and and "Clear". The preset allows the FF to be set, i.e., the Q output is made High (H). The clear allows the FF to be Reset such that the Q output is made LOW (L). Both preset and clear are independent of the clock. To activate the FF both preset and clear are held at High. The data is read at the J and K inputs when the clock is High and is transfered to the output when the clock goes to Low.

The Truth Table is shown in Table A 5.1.

	INPUTS					OUTPUT	
	Preset	Clear	Clock	J	K	Q	$\bar{Q}$
set→	L	H	X	X	X	H	L
clear→ (reset)	H	L	X	X	X	L	H
	L	L	X	X	X	unstable	
	H	H	⎍	L	L	Q_o	$\bar{Q}_o$
	H	H	⎍	H	L	H	L
	H	H	⎍	L	H	L	H
	H	H	⎍	H	H	toggle	

Truth table

Table A 5.1

1. Verify the truth table :

Identify all the pins and their connections from Fig. A 5.1.. Notice that there are two separate JK FFs in the same package.

(i) *Preset :* Connect pin 3 to High (=5V) and pin 2 to Low (=0V.). Observe the voltage at pin 15. It will be High indicating that the FF is set.

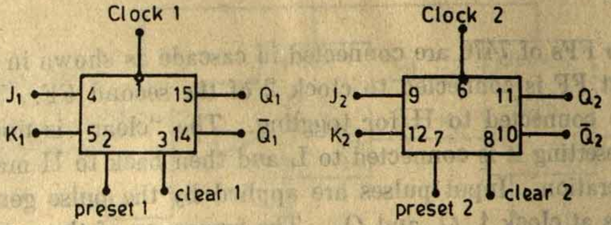


Fig. A 5.1 : JK FF (7476.

(ii) *Clear :* Connect pin 2 to H and pin 3 to L. Q_1 will be Low indicating Reset.

(iii) *Toggle :* Connect pins 2 and 3 to H and pins 4 and 5 to H. Connect 5V to pin 1 — the clock 1. Observe Q_1 and $\bar{Q}_1$. Now remove the 5V supply from pin 1 giving rise to the negative trailing edge. Observe the change at Q_1 and $\bar{Q}_1$.

(iv) Verify other entries of the truth table in a similar fashion.

2. FF as a Counter :

(a) *Count or Divide by 2 :*

The FF is connected as shown in Fig. A 5.2. J and K are connected to H and a pulse generator is connected to the clock pin 1. Observe the waveforms at pin 1 and 15. Every time the clock goes to L from H the FF toggles. The frequency of the output signal is half that of the input thus making it a divide by 2 counter.

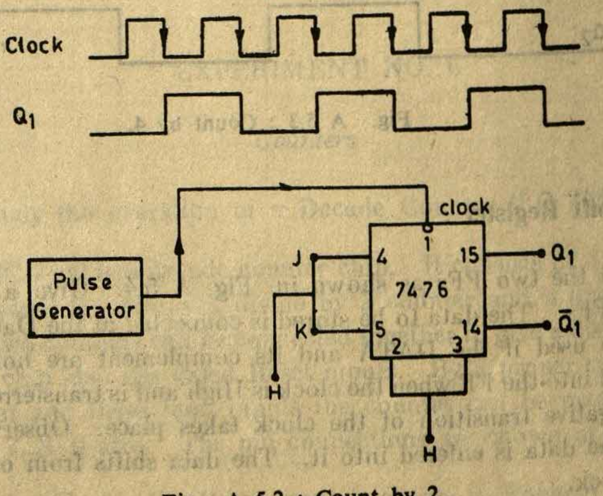


Fig. A 5.2 : Count by 2.

(b) *Divide by 4 :*

The two FFs of 7476 are connected in cascade as shown in Fig. A 5.3. The Q_1 of the first FF is connected to clock 2 of the second FF. The JK inputs of both FFs are connected to H for toggling. The "clear" is normally connected to H. For resetting it is connected to L and then back to H making the counter ready for operation. Input pulses are applied by the pulse generator. Observe the waveforms at clock 1, Q_1 and Q_2. The frequency of the output is one fourth that of the input.

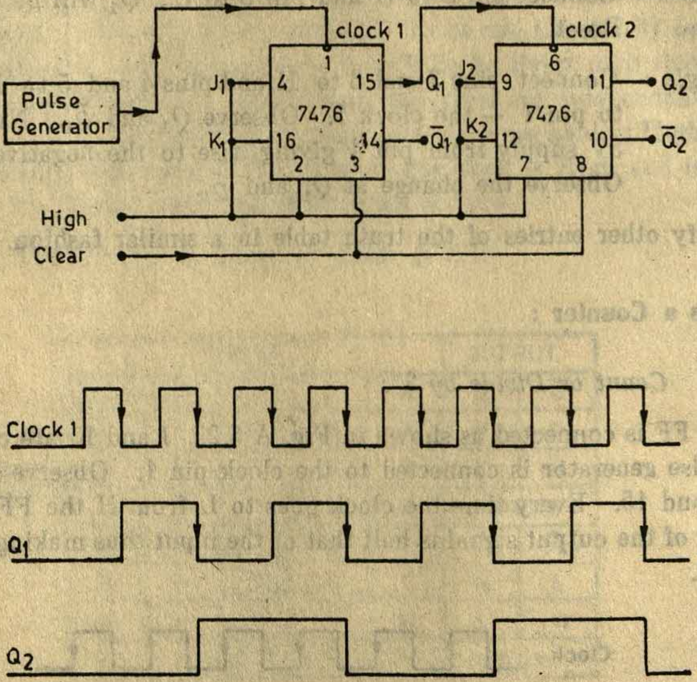


Fig. A 5.3 : Count by 4.

3. FF as Shift Register :

Connect the two FFs as shown in Fig. A 5.4. Give a 'clear' signal to initialise the FFs. The data to be stored is connected at the Data input as shown. (The NOT is used if the DATA and its complement are not available). The DATA is read into the FF when the clock is High and is transferred to the Q output when the negative transition of the clock takes place. Observe the outputs of the FFs as the data is entered into it. The data shifts from one FF to another with each clock.

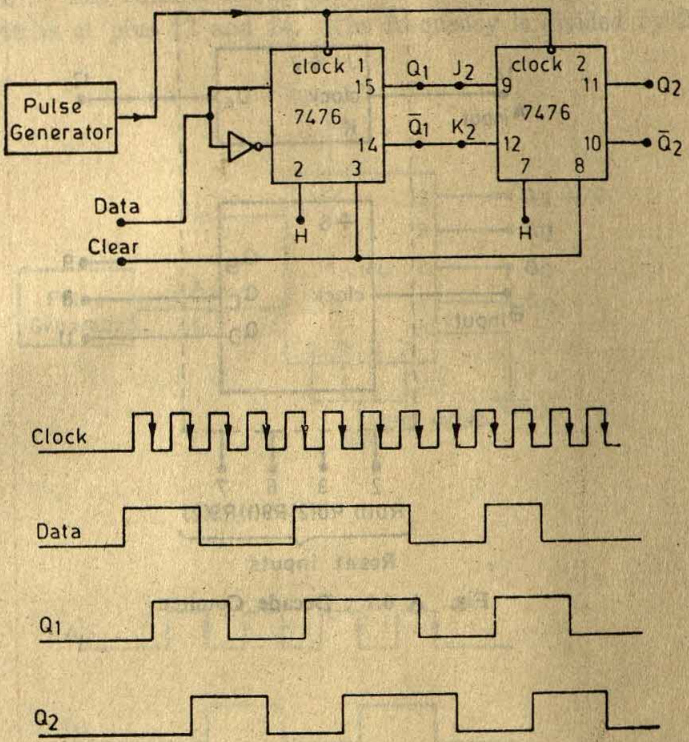


Fig. A 5.4 : Shift Register.

Exercise : Make a D FF using a JK FF.

EXPERIMENT NO. 6

Counters

Aim : To study the operation of a Decade Counter (I C 7490).

Note : The IC 7490 is a decade counter chip. It consists of 4 Master-slave FFs connected to provide a divide by 2 counter and a divide by 5 counter. The two counters can be connected together to give a divide by 10 counter. This chip also has gated Reset inputs. By a proper combination of the output and these reset inputs the counter can be made to count by 3, 4, 6, 7, 8, 9 also. The pin connections are shown in Fig. A 6.1.

The truth table for the Reset input is shown in Table A 6.1.

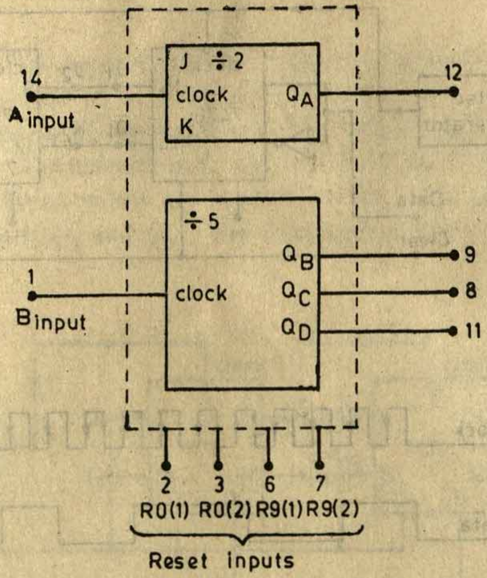


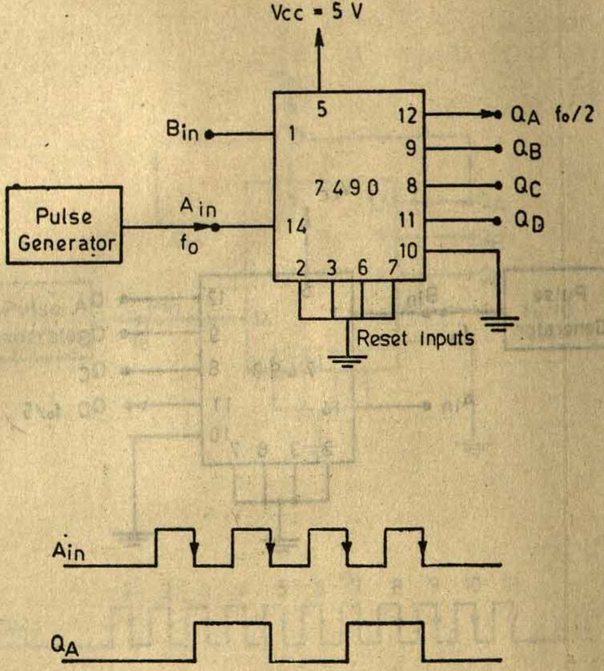
Fig. A 6.1 : Decade Counter.

	Reset	Inputs			Outputs			
	R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
1	H	H	L	X	L	L	L	L
2	H	H	X	L	L	L	L	L
3	X	X	H	H	H	L	L	H
4	X	L	X	L	COUNT			
5	L	X	L	X				
6	L	X	X	L				
7	X	L	L	X				

Table A 6.1 Truth Table

Under the conditions 1 and 2 the counter is 'reset' to all Low and under condition 3 to a specific reset with Q_B and Q_C as Low, and Q_A and Q_D as High. Under all other conditions the counter counts.

(i) *Count of* 2 *:* The counter is connected as shown in Fig. A 6.2. Observe the waveforms at pins 12 and 14. The frequency is divided by 2.



Waveform

Fig. A 6.2 : Count of 2.

(ii) *Count of* 5 *:* To count by 5, the counter is connected as shown in Fig. A 6.3. Observe the waveforms at Q_B, Q_C and Q_D.

For five pulses at the input, only one pulse is obtained at the output.

(iii) *Count of* 10 : The chip is connected as shown in Fig. A 6.4 for a count of 10. It is seen that the two stages of count by 2 and 5 are connected in cascade. Observe the waveforms. The last FF Q_D goes H at the end of the 8th pulse and goes L at the 10th pulse. The input frequency f is thus divided by ten and is available at the output point.

(iv) *Count of* 6 : For any other count other then 2, 5 and 10 the reset inputs have to be used to reset the FF at a particular instant. A count of 6 circuit is shown in Fig. A 6.5, for example, where Resets RO (1) and RO (2) are connected to Q_B and Q_C respectively and the Resets R9(1) and R9 (2) are connected to L.

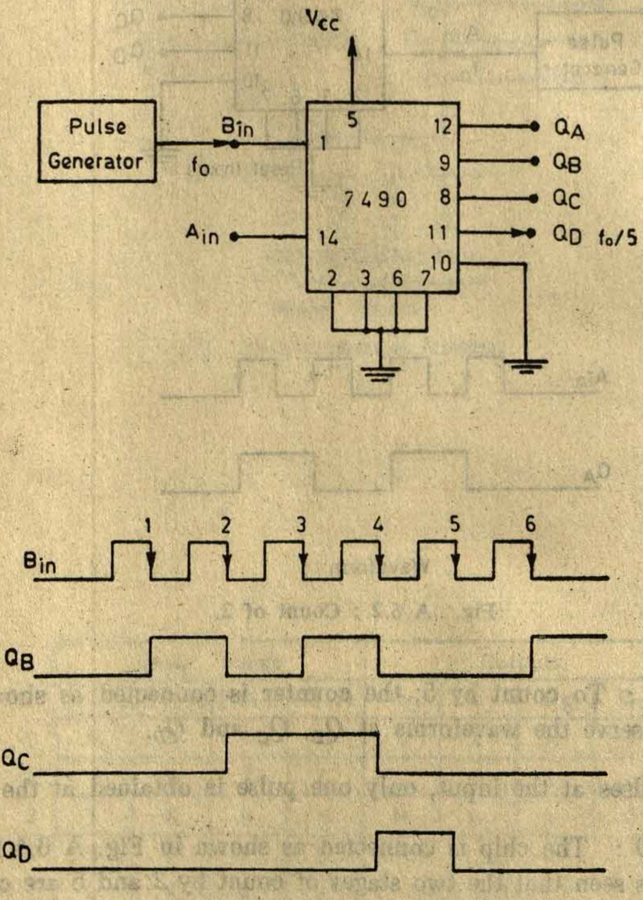
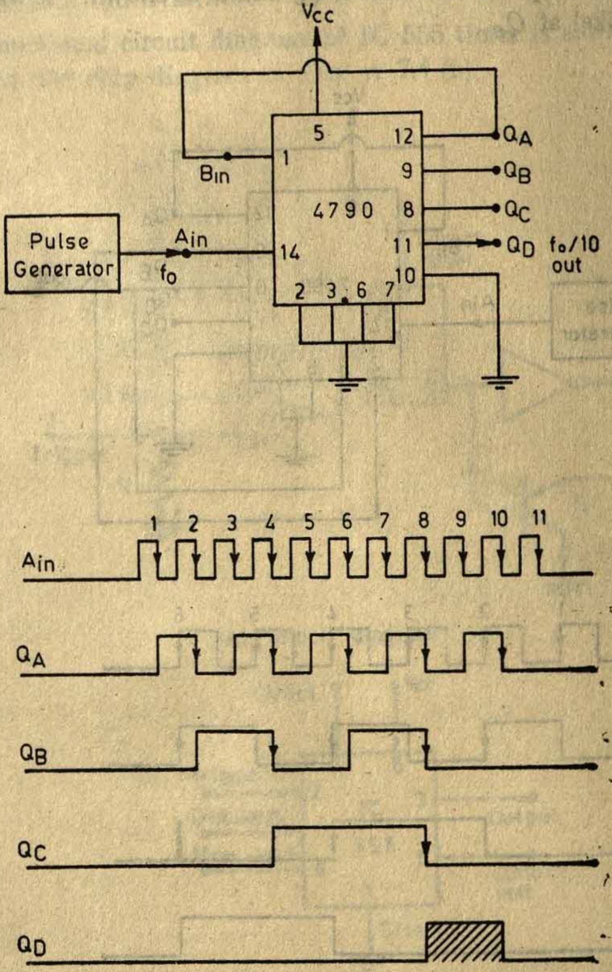


Fig. A 6.3 : Count of 5.



Waveforms

Fig. A 6.4 : Count of 10.

The count proceeds normally till the sixth pulse. When the sixth pulse occurs Q_A goes Low and Q_B goes High. Since Q_C is already High, the two reset inputs are High. From the truth table, condition 2, we see that the FFs are all reset to Low for this situation. Thus Q_A, Q_B and Q_C become Low at the end of the sixth pulse. The output is taken from Q_C and is as shown. It will be difficult to observe the 'spike' at Q_B.

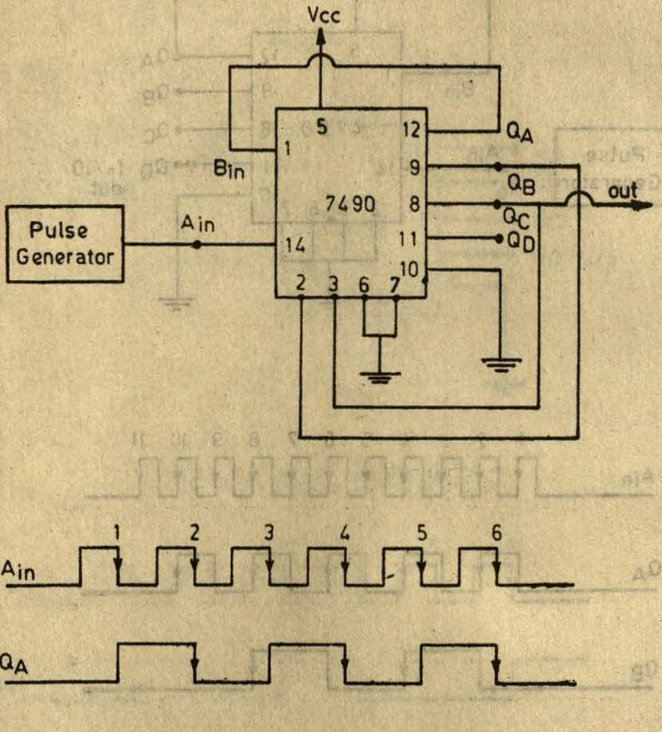


Fig. A 6.5 : Count of 6.

Exercise : Set up the decade counter to divide by 3, 4, 7, 8, 9.

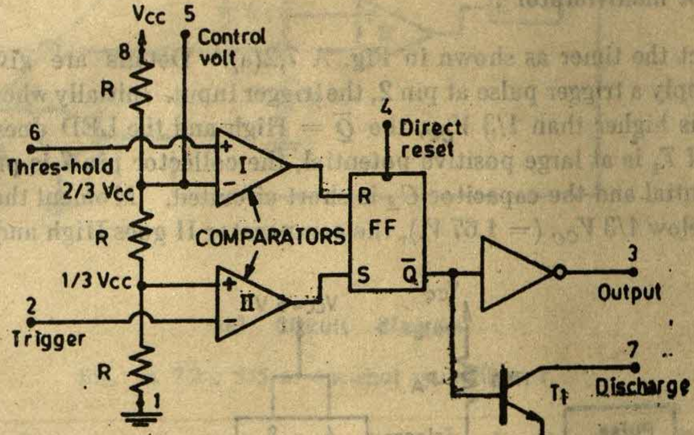
(Hint : Look into the count of 10 sequence and develop suitable 'reset' condition from the truth table).

EXPERIMENT NO. 7

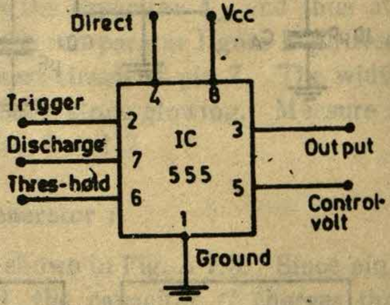
Timers

Aim : To study the timer circuit (IC 555) as a square wave oscillator and one-shot multivibrator.

Note : Functional circuit diagram of IC 555 timer is shown in Fig. A 7.1 (a) and the chip diagram in Fig. A 7.1 (b).



a) Block diagram



b) Chip diagram

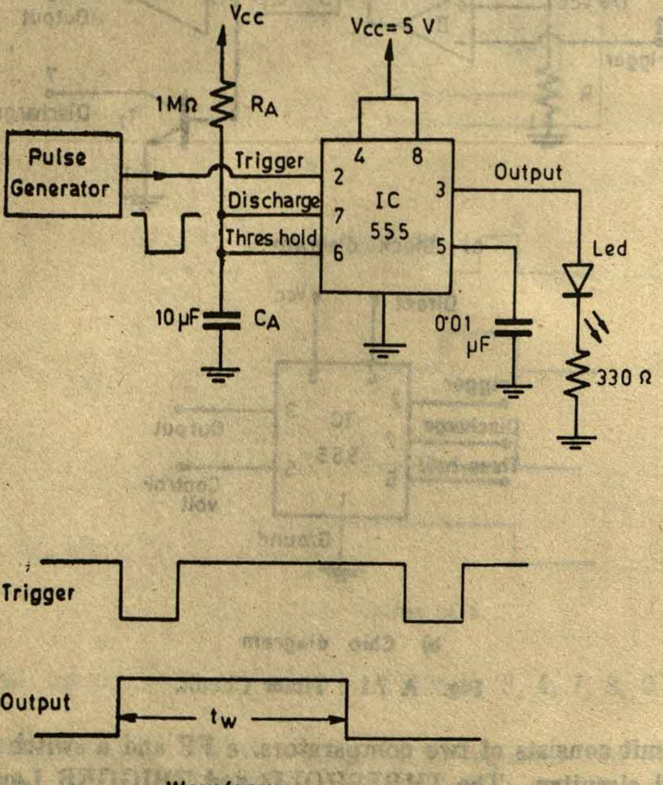
Fig. A 7.1 : Timer Circuit.

The circuit consists of two comparators. a FF and a switch T_1 along with the associated circuitry. The THRESHOLD and TRIGGER Levels are set at $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$ respectively. These levels can be altered by the use of control

voltage at pin 5. When the trigger input falls below the trigger level of 1/3 V_{CC}, the set input S of the FF goes 'High' making $\bar{Q}$ go 'Low'. The output at pin 3 will be High. Similarly when the threshold input exceeds the threshold level of 2/3 V_{CC}, the Reset R goes High making $\bar{Q}$ High. The output at pin 3 will be Low. We see that when $\bar{Q}$ is High the base of T_1 is at a large positive voltage with respect to the emitter. A low impedance path is therefore provided between the collector terminal—called the Discharge terminal—and the ground.

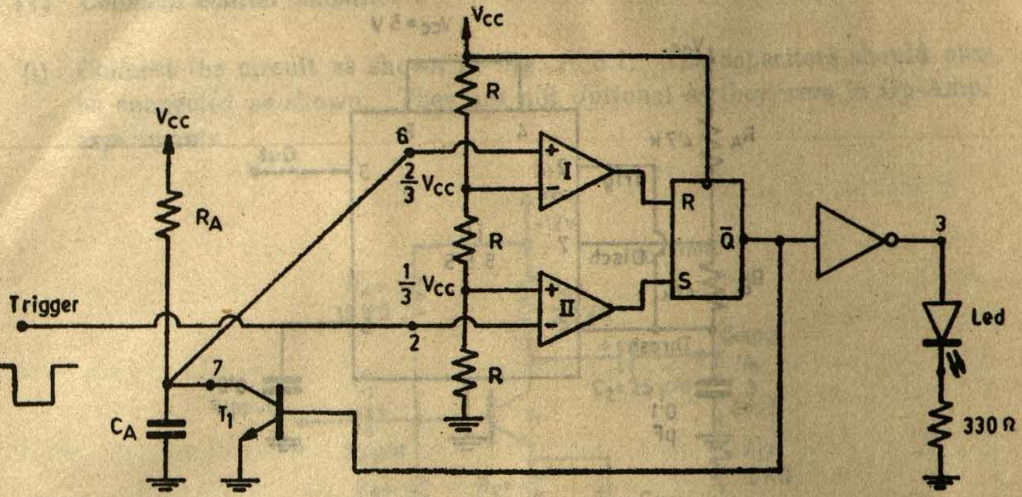
1. One Shot multivibrator :

Connect the timer as shown in Fig. A 7.2(a). Details are given in Fig. A 7.2(b). Apply a trigger pulse at pin 2, the trigger input. Initially when the trigger signal level is higher than 1/3 V_{CC}, the $\bar{Q}$ = High and the LED does not glow. Since base of T_1 is at large positive potential, the collector pin 7 is practically at ground potential and the capacitor C_A is short circuited. Moment the Voltage at pin 2 goes below 1/3 V_{CC} (= 1.67 V.), the comparator II goes High and $\bar{Q}$ = Low.



Waveforms

a) One shot multivibrator



(b) Circuit diagram

Fig. A 7.2 : 555 as one-shot multivibrator.

The transistor T_1 is open circuited and the C_A starts charging to V_{CC} through R_A. LED starts glowing (Note : the negative trigger can be applied by connecting pin 2 momentarily to ground).

As the voltage across the capacitor C_A and thus at the threshold input, reaches 2/3 V_{cc} (= 3.33V.) the comparator I goes High resetting the FF $\bar{Q}$ = H and T_I again produces a short circuit at pin 7. The width of the pulse at pin 7 is $t_w = 1.1\ R_A\ C_A$. The LED stops glowing. Measure t_w by your watch and observe the waveform at pin 3 and 7.

2. NE 555 as a Pulse Generator :

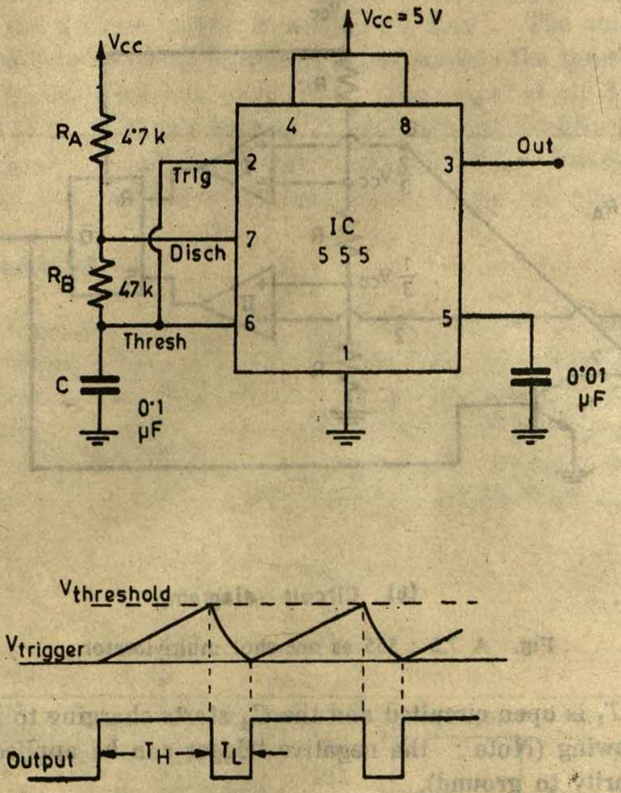
Connect the circuit as shown in Fig. A 7.3. Since pin 7 is either open circuit or short circuit to ground, the capacitor C charges through $(R_A + R_B)$ and discharges through R_B.

Observe the waveforms at pins 3, 6 and 7. Explain the operation of the circuit. It can be shown that

$$t_H = 0.693\ (R_A + R_B).\ C$$

$$t_L = 0.693\ R_B\ C$$

$$\text{and } f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$



Waveform

Fig. A 7.3 : Pulse generator using 555.

Exercise : Make the output a square wave.

EXPERIMENT – 8

Transistor Amplifiers

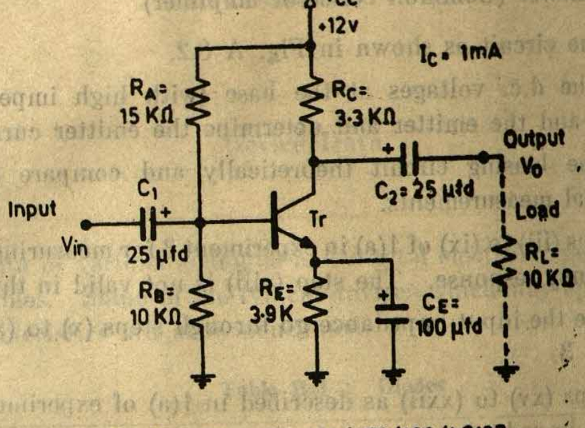
Aim :

(i) To measure the voltage gain, the frequency response the input impedance and the output impedance of a common emitter amplifier.

(ii) To measure the voltage gain, input impedance and output impedance of an emitter follower (common collector amplifier).

(1) Common emitter amplifier :

(i) Connect the circuit as shown in Fig. A 8.1. The capacitors should also be connected as shown. They are not optional as they were in Op-Amp. experiments.



Tr = Transistor : CIL 474/475/490/AC127
(or any other NPN transistor
with β = 50-150)

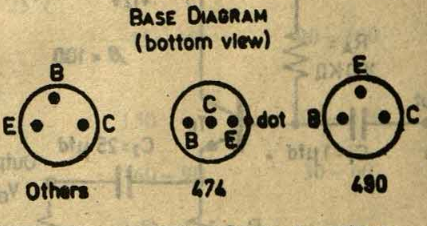


Fig. A 8.1 : C. E. Amplifier.

(ii) Study the four resistance biasing of the amplifier. Measure the d.c. voltages at the emitter and collector. The base voltage should be measured by a high impedance electronic multimeter. Calculate the collector current from those measurements.

(iii) Analyse the biasing circuit and comparo the measured and the calculated bias voltages and currents.

(iv) To measure the gain and frequency response of the CE amplifier, go through steps (iii) to (ix) of 1(a) in experiment-3. The step (viii) is not required here.

(v) Repeat steps (x) to (xiii) of 1(a) in experiment No. 3 to measure the input impedance.

(vi) Measure the output impedance by following steps (xv) to (xxii) as described in 1 (a) of experiment-3.

(vii) Compute the gain, upper cut-off frequency, the input and the output impedances theoretically and compare your results with experimental values, as measured.

(2) Emitter follower (Common collector amplifier)

(i) Connect the circuit as shown in Fig. A 8.2.

(ii) Measure the d.c. voltages at the base (with high impedance electronic voltmeter) and the emitter and determine the emitter current.

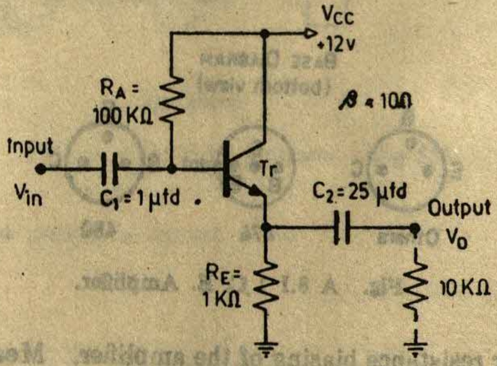
(iii) Analyse the biasing circuit theoretically and compare the results with experimental measurements.

(iv) Repeat steps (iii) to (ix) of 1(a) in experiment 3 for measuring gain, phaseshift and frequency response. The step (viii) is not valid in this case.

(v) To measure the input impedance go through steps (x) to (xiii) as in 1(a) of experiment 3.

(vi) Follow steps (xv) to (xxii) as described in 1(a) of experiment 3 to measure the output impedance.

(vii) Compute the gain, the input and the output impedances theoretically and compare with experimentally measured values.



Tr = Transistor : CIL 474 / 475 / 490 / AC127
(or any other NPN transistor
with β = 50-150)

Fig. A 8.2

APPENDIX – B

Device Data

Practical data of various analogue and digital electronic devices are given in the following tables. Some of the typical devices which may approximately meet the given characteristics are also mentioned.

Table B-1 : Diodes

	General purpose (Germanium point contact)	General purpose (Silicon)	AM & FM detectors (Germanium)	Rectifier (Silicon)
Absolute max. rations at $25^\circ C$.				
Forward current (mA)	45–60	90–100	35–50	1000 (av)
Repetitive peak forward current (mA)	150	100–120	100–150	10×10^3
Reverse voltage (volt)	60–90	30–60	15–30	400–800
Repetitive peak rev. voltage (volt)	100–115	—	30–45	600–1200
Forward voltage at forw. current = 0.1mA (volt)	0.1–0.2	0.5–0.7	0.15–0.3	1.5 at 5A.
Reverse current at rev. voltage = 1.5V. (μA)	0.5–15	0.025	0.1–2.8	10 at max. rev. voltage
Operating temp. range °C	–50 to +75	—	–50 to +75	—
Typical devices	OA 81 OA 85 OA 91 1N58A 1N294	BA100, CA282	OA79, 1N60	BY100.

Table B—2 : Transistors

	Application	Absolute max. ratings at 25°C			h_{FE}	f_T	I_{CBO}	Typical devices
		Collector current I_c (mA)	Collector emitter breakdown voltage (volts)	Collector dissipation				
1.	Low-noise audio preamplifier (npn-Ge)	8 to 10	10 to 12	150—200mW	40—120 at 0.5 mA	2.5 MHz	10 μA	AC172
2.	Audio driver (pnp—Ge)	80 to 100	10 to 12	400—500mW	80 —100 at 2mA	1.5 MHz	10 μA	AC125
3.	Low-noise audio preamplifier (npn-Si)	80—100	15 to 20	200—300mW	250—800	300 MHz	1 nA	BC109
4.	Audio driver (npn-Si)	80 to 100	20 to 45	100—220mW	125—800 at 2mA	30—300 MHz	0.02—0.1μA	BC147, BC148, CIL463
5.	Audio power (pnp-Ge)	3000	30	20W	30—60 at 1A	500 KHz	2.5 mA	AD149
6.	Audio power (pnp-Ge)	1000	15	600mW	300 at 2A.	1.5 MHz	20 μA	AC188 (complementary pair npn-Ge AC187).
7.	High freq. (pnp-Ge)	8—10	10—15	50—75mW	100—200 at 1mA	70 MHz	1—2 μA	AF114.
8.	High freq. (npn-Si)	20—30	12—20V.	100—150mW	100—150 at 1mA	150—200MHz	0.1 μA	BF115, BF194, CIL475.
9.	Video (npn-Si)	100	150—220	2—3 W	20—60 at 30 mA	125 MHz	—	BF336, BF337, BF338.
10.	General industrial (pnp-Si)	1000	35	5W	> 50 at 10 mA	70 MHz	< 50 nA	BFS95

Table B—3 : Operational Amplifiers

S.N.	Absolute max. ratings			Input current	Input resistance	CMRR dB	Unity gain band-width product MHz	Slew rate V/µs	Output resis-tance	Large signal voltage gain	Typical device	Category
	Supply voltage	Differ-ential input voltage/current	Input voltage									
1.	±18V	±30V	±15V	80-500nA	2 M Ohm	70-90	1.0	0.5	75 Ohm	20K-200K	741	General purpose
2.	±20V	±10mA	±15V	150-500nA	0.5-3M Ohm	80-100	15.0	50-70	—	25K-200K	318	Wideband
3.	±18V	±30V	±15V	30-75nA	1.5-4M Ohm	80-100	—	—	—	50K-150K	101	High Performance
4.	±22V	±30V	±22V	5-100pA	10^{14} Ohm	80	1.0	6	—	50K-100K	536	FET—input
5.	±20V	±30V	±20V	0.8-7 nA	10-70M Ohm	80-100	250KHz	0.2	75 Ohm	15K-250K	537	Precision

B.4 DIGITAL DEVICES

Table B.4.1

Supply Current

Devices	I_{CCH}(mA) Total with outputs High		I_{CCL}(mA) Total with outputs Low	
	TYP	MAX	TYP	MAX
7400	4	8	12	22
7404	6	12	18	33
7410	3	6	9	16.5
7420	2	4	6	11
7430	1	2	3	6
7402	8	16	14	27
7427	10	16	16	26
7408	11	21	20	33
7411	8	15	14	22
7432	15	22	23	38
7486	30	50	36	57
7473 7476 7474	Average per Flip-Flop		9	17
7490	26	39		

Table B.4.2 Electrical Characteristics

Parameter	NAND/INVERTER			NOR			AND			OR			EX-OR			FLIP-FLOP			COUNTER			UNITS
	7400, 7404, 7410, 7420, 7430			7402, 7427			7408, 7411			7432			7486			7473, 7476			7490			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH} **High Level Input Voltage**	2			2			2			2			2			2			2			V
V_{IL} **Low Level Input Voltage**			0.8			0.8			0.8			0.8			0.8			0.8			0.8	V
I_{OH} **High Level Output Current**			—400			—800			—800			—800			—800			—400			— 00	μA
V_{OH} **High Level Output Voltage**	2.4	3.4		2.4	3.4		2.4	3,4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
I_{OL} **Low Level Output Current**			16			16			16			16			16			16			16	mA
V_{OL} **Low Level Output Voltage**		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I **Input Current at Maximum Input Voltage**			1			1			1			1			1			1			1	mA
I_{IH} **High Level Input Current**			40			40			40			40			40			40			40	μA
I_{IL} **Low Level Input Current**			— 1.6			— 1.6			— 1.6			— 1.6			— 1.6			— 1.6			— 1.6	mA
I_{OS} **Short Circuit Output Current**	—20		—55	—20		—55			—55			—55			—55			—55			—57	mA

Table B.4.3

Switching characteristics at $V_{cc} = 5V$

Device	t_{PLH} (ns) Propagation Delay Time Low to High Level Output			t_{PHL} (ns) Propagation Delay Time High to Low level Output		
	MIN	TYP	MAX	MIN	TYP	MAX
7400, 7410		11	22		7	15
7404, 7420		12	22		8	15
7430		13	22		8	15
7402		12	22		8	15
7427		7	11		10	15
7408, 7411		17.5	27		12	19
7432		10	15		14	22
7486		15	23		11	17
* 7473, 7476		16	25		25	40
7474		—	25		—	40
**7490		10	16		12	18

* Clock frequency Typ. 20 MHz & Min 15 MHz

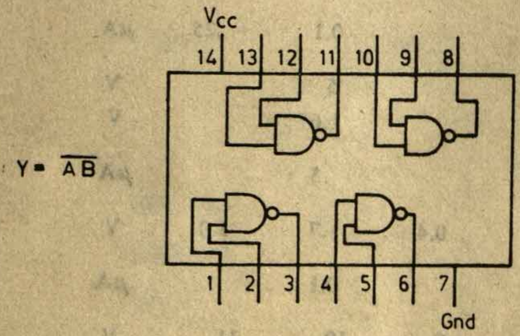
** Clock frequency Typ. 42 MHz & Min 32 MHz

Table B.4.4

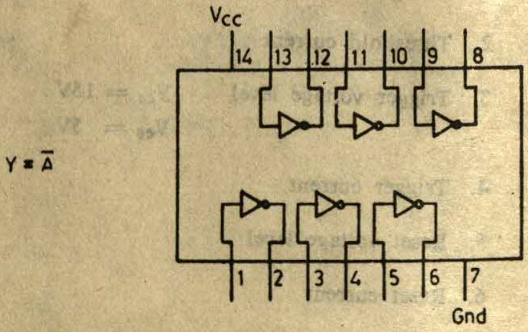
555 Precision Timer

Parameter	Test condition	555			Unit
		Min	Typ	Max	
1. Threshold voltage level as a percentage supply voltage			66.7		%
2. Threshold current			0.1	.25	μA
3. Trigger voltage level	$V_{cc} = 15V$		5		V
	$V_{cc} = 5V$		1.67		V
4. Trigger current			.5		μA
5. Reset voltage level		0.4	.7	1.0	V
6. Reset current			0.1		μA
7. Control voltage	$V_{cc} = 15V$	9	10	11	V
	$V_{cc} = 5V$	2.6	3.3	4	V
8. Low level output voltage	$V_{cc} = 15V$; $I_{OL} = 50$ mA		.4	.75	V
	$V_{cc} = 5V$; $I_{OL} = 8$ mA		.16	.35	V
9. High level output voltage	$V_{cc} = 15V$; $I_{OH} = -100$ mA	12.75	13.3		V
	$V_{cc} = 5V$; $I_{OH} = -100$ mA	2.75	3.3		V
10. Supply current	Output Low ; $V_{cc} = 15V$		10	15	mA
	Output High ; $V_{cc} = 5V$		9	14	mA
11. Initial accuracy of timing interval			10		%
12. Output pulse rise time			100		nsec.
13. Output pulse fall time			100		nsec.

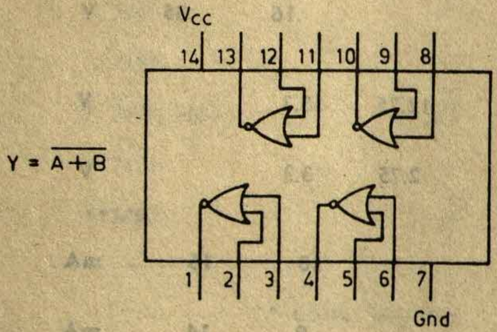
B-5 PIN ASSIGNMENT



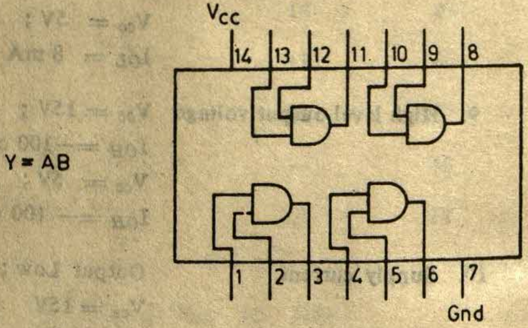
7400 Quad 2-input NAND gates



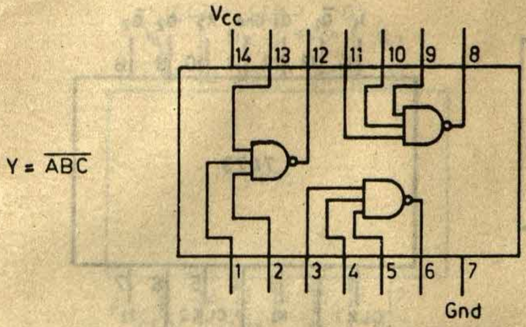
7404 Hex inverters



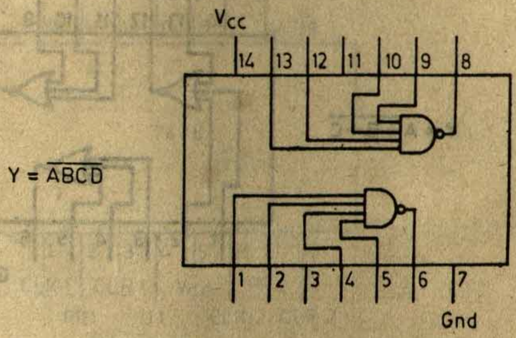
7402 Quad 2-input NOR gates



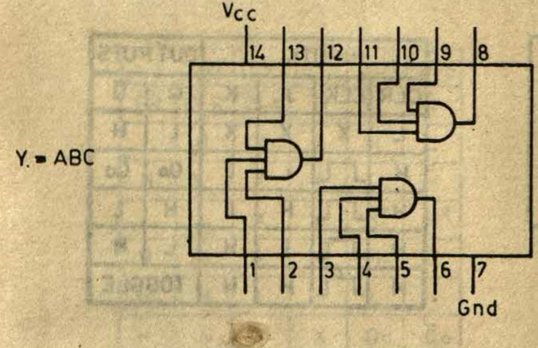
7408 Quad 2-input AND gates



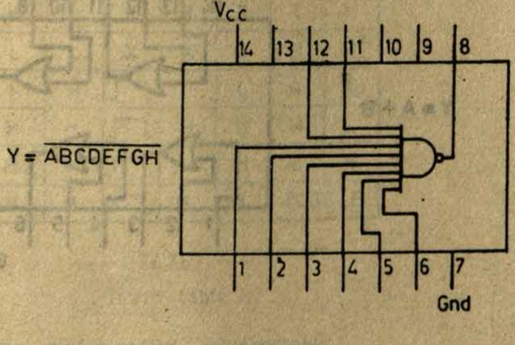
7410 Triple 3-input NAND gates



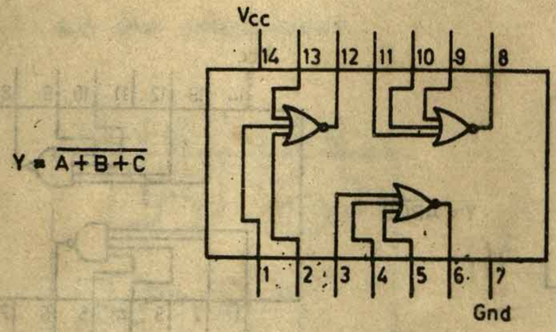
7420 Dual 4-input NAND gates



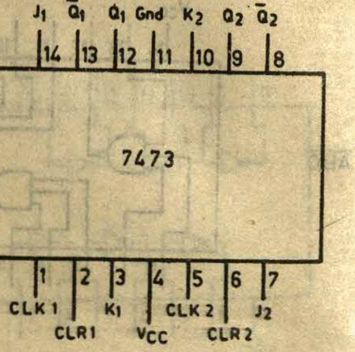
7411 Triple 3-Input AND gate



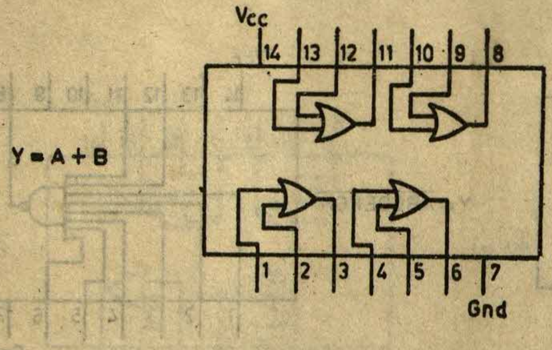
7430 8-input NAND gates



7427 Triple 3-input NOR gates



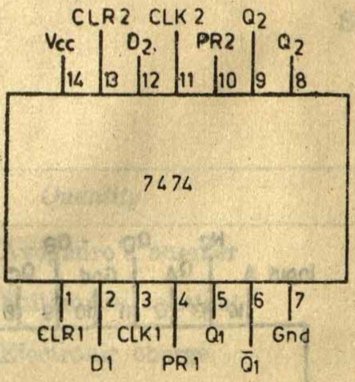
7473 Dual J-K flip-flop with clear



7432 Quad 2-input OR gates

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

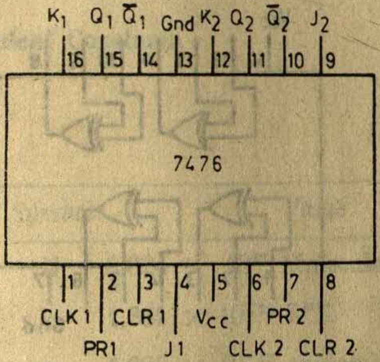
7473
Truth table



7474 Dual D positive edge triggered flip-flop with preset and clear

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Qo	$\bar{Q}$o

7474
Truth table



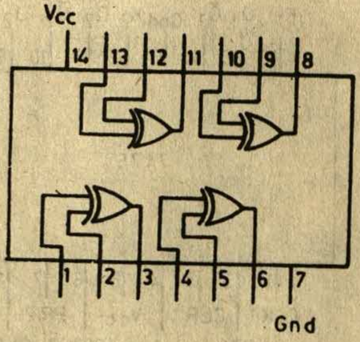
7476 Dual J-K flip-flop with preset and clear

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Qo	$\bar{Q}$o
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

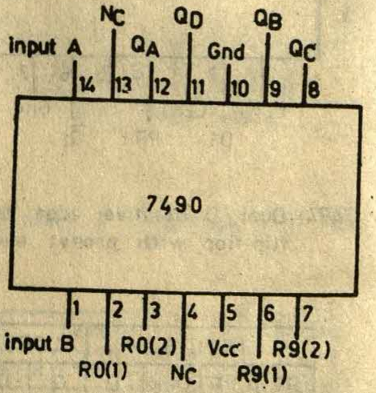
7476
Truth table

This configuration is nonstable
Qo = The level of Q before the indicated input conditions were established

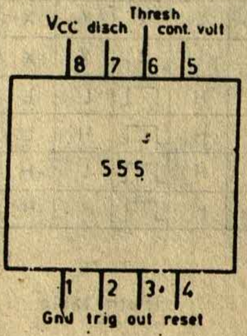
$Y = \bar{A}B + A\bar{B}$



7486 Quad 2-input EXCLUSIVE-OR gates



7490 Decade counter



555 Timer

APPENDIX C

Some Physical Constants

Quantity	*Symbol*	*Value*
Avogadro's number	N	6.024×10^{23} Molecules per mole
Boltzmann constant	k	1.381×10^{-23} J/°K
Electronic charge	q	1.602×10^{-19} coulomb
Electronic mass	m	9.1085×10^{-11} kg
Electron volt	eV	1.602×10^{-19} Joule
Electronic charge to electronic mass ratio	q/m	1.759×10^{11} coul/kg
Faraday's constant	F	9.649×10^{3} coul/mole
Gas constant	R	8.314 J/ (deg) (mole)
Permittivity of free space	ϵ_o	8.85×10^{-12} farad/m $= 1/(36\pi \times 10^{9})$ farad/m
Permeability of free space	μ_o	$4\pi \times 10^{-9}$ henry/m
Planck's constant	h	6.625×10^{-34} Joule-sec.
Proton mass	m_p	1.673×10^{-27} kg
Proton mass to electron mass ratio	m_p/m	1.837×10^{3}
Stefan-Boltzmann constant		$5.67 \times 10^{-8}\ W/(m^2)\ (o_K{}^4)$
Thermal voltage ($T = 300$°K)	$\frac{kT}{q}$	25.9×10^{-3} volts
Velocity of light	C	2.998×10^{8} m/s.

APPENDIX D

deci Bel (dB)

Power gain in dB $= 10 \log \frac{P_o}{P_i}$, Voltage gain in dB $= 20 \log \frac{V_o}{V_i}$,

Current gain in dB $= 20 \log \frac{I_o}{I_i}$

(Subscript o stands for output and subscript i stands for input).

Conversion of voltage or current and power ratios into dB and vice-versa are given in the following tables.

Table D-1 Conversion of voltage or current ratios into dB

Voltage Ratio	.0	.1	.2	.3	.4	.5	.6	.7	.8	.9
1	.000	.828	1.584	2.279	2.923	3.522	4.082	4.609	5.105	5.575
2	6.021	6.444	6.848	7.235	7.604	7.959	8.299	8.627	8.943	9.248
3	9.542	9.827	10.103	10.370	10.630	10.881	11.126	11.364	11.596	11.821
4	12.041	12.256	12.465	12.669	12.869	13.064	13.255	13.442	13.625	13.804
5	13.979	14.151	14.320	14.486	14.648	14.807	14.964	15.117	15.269	15.417
6	15.563	15.707	15.848	15.987	16.124	16.258	16.391	16.521	16.650	16.777
7	16.902	17.025	17.147	17.266	17.385	17.501	17.616	17.730	17.842	17.953
8	18.062	18.170	18.276	18.382	18.486	18.588	18.690	18.790	18.890	18.988
9	19.085	19.181	19.276	19.360	19.463	19.554	19.645	19.735	19.825	19.913

For voltage ratios between 0.01 and 0.099, use above table to get dB for 100 times the ratio and subtract 40 dB.

For voltage ratios between 0.1 and 0.99, use above table to get dB for 10 times the ratio and subtract 20 dB.

For voltage ratios between 1 and 9.9, use above table directly.

For voltage ratios between 10 and 90, use above table to get dB for 1/10th of the ratio and add 20 dB.

For voltage ratios between 100 and 990, use above table to get dB for 1/100th of the ratio and add 40 dB.

Table D-2 Conversion of power ratios into dB

Power Ratio	.0	.1	.2	3.	.4	.5	.6	.7	.8	.9
1	.000	.414	.792	1.139	1.461	1.761	2.041	2.304	2.553	2.788
2	3.010	3.222	3.424	3.617	3.802	3.979	4.150	4.314	4.472	4.624
3	4.771	4.914	5.051	5.185	5.315	5.441	5.563	5.682	5.798	5.911
4	6.021	6.128	6.232	6.335	6.435	6.532	6.628	6.721	6.812	6.902
5	6.990	7.076	7.160	7.243	7.324	7.404	7.482	7.559	7.634	7.709
6	7.782	7.853	7.924	7.993	8.062	8.129	8.195	8.261	8.325	8.388
7	8.451	8.513	8.573	8.633	8.692	8.751	8.808	8.865	8.921	8.976
8	9.031	9.085	9.138	9.191	9.243	9.294	9.345	9.395	9.445	9.494
9	9.542	9.590	9.638	9.685	9.731	9.777	9.823	9.868	9.912	9.956

For Power Ratios between 0.01 and 0.099, use above table to get dB for 100 times the ratio and subtract 20 dB.

For Power Ratios between 0.1 and 0.99, use above table to get dB for 10 times the ratio and subtract 10 dB.

For Power Ratios between 1 and 9.9, use above table directly.

For Power Ratios between 10 and 99, use above table to get dB for 1/10th of the ratio and add 10 dB.

For Power Ratios between 100 and 990, use above table to get dB for 1/100th of the ratio and add 20 dB.

Table D-3 : Conversion of dB into voltage or current and power ratios

Power Ratio	Voltage Ratio	− ← db + →	Voltage Ratio	Power Ratio
1.000	1.0000	.0	1.000	1.000
.9772	.9886	.1	1.012	1.023
.9550	.9772	.2	1.023	1.047
.9333	.9661	.3	1.035	1.072
.9120	.9550	.4	1.047	1.096
.8913	.9441	.5	1.059	1.122
.8710	.9333	.6	1.072	1.148
.8511	.9226	.7	1.084	1.175
.8318	.9120	.8	1.096	1.202
.8128	.9016	.9	1.109	1.230
.7943	.8913	1.0	1.122	1.259
.6310	.7943	2.0	1.259	1.585
.5012	.7079	3.0	1.413	1.995
.3981	.6310	4.0	1.585	2.512
.3162	.5623	5.0	1.778	3.162
.2512	.5012	6.0	1.995	3.981
.1995	.4467	7.0	2.239	5.012
.1585	.3981	8.0	2.512	6.310
.1259	.3548	9.0	2.818	7.943

Table D-3 (*Contd.*)

Power Ratio	Voltage Ratio	db $-$ ← $+$ →	Voltage Ratio	Power Ratio
.10000	.3162	10.0	3.162	10.00
.07943	.2818	11.0	3.548	12.59
.06310	.2512	12.0	3.981	15.85
.05012	.2293	13.0	4.467	19.95
.03981	.1995	14.0	5.012	25.12
.03162	.1778	15.0	5.623	31.62
.02512	.1585	16.0	6.310	39.81
.01995	.1413	17.0	7.079	50.12
.01585	.1259	18.0	7.943	63.10
.01259	.1122	19.0	8.913	79.43
.01000	.1000	20.0	10.00	100.00
10^{-3}	3.162×10^{-2}	30.0	3.162×10	10^3
10^{-4}	10^{-2}	40.0	10^2	10^4
10^{-5}	3.162×10^{-3}	50.0	3.162×10^2	10^5
10^{-6}	10^{-3}	60.0	10^3	10^6
10^{-7}	3.162×10^{-4}	70.0	3.162×10^3	10^7
10^{-8}	$\times 10^{-4}$	80.0	10^4	10^8
10^{-9}	3.162×10^{-5}	90.0	3.162×10^4	10^9
10^{-10}	10^{-5}	100.0	104^5	10^{10}

INDEX

Acceptor 18
Active devices 4
Adder, full 310
  half 310
Addition in binary 310
Alloy junction 105, 106
Alpha, 55, 317
  Inverse 317, 321

Amplifier, 121
  A.C. 280
  bridge 284
  C. E. 162
  FET 187
  ideal 121
  instrumentation 284
  inverting 251
  non-inverting 249
  Photodiode 286
  vacuum tube 200

Analogue signal 5
AND, function 299
AND Gate—TTL 324
Anode 1, 24
Associative laws 305
Astable multivibrator, 288, 357
  duty cycle 359
  frequency 359, 392
  period 392
  timing waveform 348, 358
  transistor 390
  waveform 391
Atomic structure 8
Automatic voltage regulator 436

Band, structure 12
  conduction 12
  forbidden 13
  valance 13
Bandwidth, 134
  CE Amp. 145
  FET Amp. 194
Base 3
Base spreading resistance $r_{bb'}$ 176
Battery charging 34
Berkhausen criterion of oscillation 365
Beta, 55
  d.c. 316

Biasing, 145
  biasline 201
  external (diode) 23
  FET 187
  forward (diode) 24
  modified biasing 190
  reverse (diode) 23
  self bias 187
  transistor 145
  triode 206

Binary, addition 310
  numbers 307
  signal 297

Bohr's model of atom 8
Bonds, 3, 10
  covalent 10
  ionic 10
  metallic 10
Boolean, algebra 303
  theorem 303
Breakdown, 30
  avalanche 30
  zener 30
Bridge, amp 276
  rectifier 434

Capacitance, in transistor 176
  transition 176
  diffusion 176
Capacitor input filter, 414
  half wave rectifier d.c. voltage 416
  full wave rectifier d.c. voltage 421
Cathode, 1
  by-pass 203
  ray oscilloscope (CRO) 82
  ray tube (CRT) 82
Charge carriers 3, 20
Child-Langmuir law 77
Clamper 35
Class A, B, C amplifiers 143
CLC filter 434
Clear FF 341, 342
Clipper 36
Clocked SR FF 336
CMOS, 325
  Gates 325
  inverter 326

  logic circuit 313
 CMOSFET 325
  construction 326
  n-channel 325
  p-channel 325
 CMRR 262
 Collector 3
 Collector coupled monostable multivibrator 396
 Collector saturation current I_{CO} 54, 146, 150, 316
 Common mode gain of diff. amp. 257
 Commutating capacitor 399
 Commutative laws 305
 Comparator 355

 Compensation of Op-amp. 271
 Complementary output circuit 268
 Complement of a function 304
 Concentration gradient 20
 Condition of oscillation, 371
  Berkhausen 365
  Colpitts 367
  Phase shift 378
  Wienbridge 374

 Conduction angle 416, 418
 Conduction band 13
 Conductivity 17
 Conversion from decimal to binary 308
 Counters, 346
  asynchronous 347
  Count of K 347
  Count of 3 347
  count of 4 347
  count of 5 347
  count of 16 347
  decade 347
  parallel 353
  synchronous 347, 353

 Covalent band 10
 Criterion of oscillation 364
 Critical, Current 430
  inductor 432
 Crystalline, structure 8, 9
  lattice 17
 Cut-in voltage, 28
  transistor 316, 113
  diode (V_d) 28, 33
 Cut-off (corner) frequency 137
 Darlington pair amplifier 266
 Decade counter 317, 351
  feedback 351
  state diagram 351
  timing waveform 351
  2, 5 351
 deci Bel (dB) 116
 Deflection sensitivity 88
 Depletion region 21
 Desensitivity, feedback amp. 219
 Devices, 1
  active 1
  passive 3
  semiconductor 3
  solid state 3
 D flip-flop 342
 Difference amp. 252
 Differential amp. 257
 Differential mode gain 256
 Differentiation with Op-amp. 276
 Diffusion, 22
  current 22
  technique 105
 Digital signal 5
 Diode, 24
  equation 28
  gas 24
  light emitting 46
  photo diode 48
  pn junction 20
  pnpn 70
  Schottky barrier 37, 325
  semiconductor 20, 27
  tunnel 41, 366
  vacuum 20, 77
  varactor 45
  Zener 39, 263
 Dissipation hyperbola of max. power 146
 Distortion reduction 219
 Distributive laws 305
 Donor 17
 Doping 104
 Drain saturation current 192
 Drift current 22
 Driving point parameters, impedance, admittance 115, 118
 DTL logic circuit 313
 Dual of a function 304
 ECI logic circuit 313
 Efficiency, amplifier 145
 Efficiency, full-wave rectifier 413
  half-wave rectifier 413
 Electron-volt 9
 Electrical, conduction 14
  conductors 14
  insulators 14
  semiconductor 15

Electronic structure 8
Emission 1
Emitter, 3
  bypass 167
  low frequency response 171
Emitter follower, 207
  equivalent circuit 207
  input impedance 207
  output impedance 207
Energy, levels 9, 12, 43
  hydrogen atom 8
  transition 9
Energy stored, 414
  inductor 426
Equivalent circuit, 123
  BJT 176
  crystal 388
  FET 194
  high frequency 204
  pentode 202
  triode 201
Equivalent function 304
Error Amplifier 438
Etching 103, 109
Ex-OR, function 302
  realisation 311
External voltage gain 159
Extinction angle 416
Fan out, 323
  CMOS 329
  TTL 323
Feedback, amplifier 217
  factor, F (s) 218
  function, f(s) 218
  oscillators 364
  types 224
  input impedance 224, 229, 238
  output impedance 224, 230, 238
Fermi level 13
Field effect transistor 62
FET, Junction 62
  breakdown 65
  channel 64
  characteristic 64
  depletion region 63
  pinch-off 65
FET, insulated gate 66
  enhancement mode 66
  depletion mode 68
Filaments 24
Filters, active, 291
  band pass 291
  high pass 291
  low pass 291
Filters, high pass 134
  low pass 134
Flip-flop 342
  D 342
  JK 338
  SR 333
Four layer devices 70
Four terminal network 114
Free running multivibrator 288
Frequency of oscillation,
  Colpitts oscillator 367
  multivibrator 355
  phase-shift oscillator 370
  tunnel diode 386
  Wienbridge 374
Frequency stability 384
Frequency of sweep signal 400
Frequency response of CE amplifiers, 154
  high frequency 198
  low frequency 162
  mid-band 173
Frequency response of FET amplifier, 194
  high frequency 198
  low frequency 198
  midband 194
Frequency response, magnitude 137
  phase 136
Frequency response of op-amp 137
Frequency response of vacuum tube
  amplifier, 200
  high frequency 204
  low frequency 202
Full adder 310
Full wave rectifier, 411
  d.c. current 412
  d.c. voltage 412
  ripple factor 412
Functions of binary variables 298
Gallium arsenide 3
Gain 115
  CE amp. 159
  high frequency 175
  low frequency 162
  mid-band 173
  current 115
  differential amp. 255
  common mode 256
  difference mode 256
  FET amp. 187
  Op-amp 249
  open loop 271
  margin 272
  power 115
  tube amp. 200

  voltage 115
Gas diode 24
Gas tube, 91
  hot cathode 93
Germanium 3
Generator, frequency 392
  sine wave 291, 363
  square wave 389
Glow discharge, 93
  cold cathode 92
Grid 2
Grown junction transistor 107
Half adder 310
Half wave rectifier, 407
  d.c. current 409
  d.c. voltage 409
  ripple factor 410
Harmonic content of, 409
  fullwave rectifier 412
  halfwave rectifier 409
h_{FC} 318
h_{FE} 316, 320
h_{fe} 129
High pass filters 134
High voltage in TTL 324
Holes 3, 16
Hybrid-π circuit 176
Hybrid parameters 127
I C fabrication 110
I_{CBO} 316
I_{CO} 54, 146, 150, 315
Ideal amplifier 121
Ideal op-amp. 247
Ignition angle 418
Impurity 3, 17
Inductor input filter, 425
  d.c. voltage 428
  ripple factor 428
Input bias current in op-amp. 274
Input impedance,
  CE amp. 165
  differential 266
  emitter follower 207
  feedback amp. 273
  FET amp. 190
  Op-amp. 247
Input offset current in op-amp. 274
Input offset voltage of op-amp. 274
Instrumentation amp. 204
Integration, 4
  LSI 4
  MSI 4
  SSI 4
  VLSI 4
Integrator using op-amp. 276
Inverse mode of operation of transistor 317
Inverter 300, 326
Inverting amp. 251
Ionic band 10
Ionisation energy of gases 94
JK Flip-flop, 338
  asynchronous operation 341
  Clear 341
  master-slave 341
  negative edge triggered 341
  preset 341
  synchronous operation 341
  truth table 339, 341
Junction 3, 4
Junction capacitance 45
LC filter, in rectifiers 429
  critical current 432
  critical inductor 432
  full-wave 429
  ripple factor 432
LC oscillators 367
LED 46
Load line in vacuum tube 201, 202
Logic circuits 298, 307
  CMOS 313, 325
  DTL 313
  ECL 313
  RTL 313
  TTL. 313, 320
Logical statements 298
Loop transmission function 219
Lower 3-db freq. point of CE amp. 175
Low-pass filter 134
Low voltage in TTL 324
LSI 4
Magnitude response 137
Majority carriers 29
Master-slave flip-flop, 339
  JK 341
MESFET 69
Metallic bond 10
Metal semiconductor junction 38
Microminiaturization 111
Miller's capacitance 180
Minority carriers 29
Mobility 17
Modulo, 'K' counter 352
  3 counter 349
  4 counter 348
  5 counter 350
  10 counter 351
  16 counter 348
Monostable multivibrator, 355

  collector coupled 396
  delay 355
  frequency 396
  gate time 355
  Op-amp. 396
  pulse width 355, 357
MOSFET 66
MSI 4
Multiple emitter, logic gates 321
  transistor 321
Multivibrator, astable 288
  monostable 354
NAND, function 301
  CMOS gate 327
  TTL 320, 321
Negative feedback, 217
  advantages 219
  disadvantages 219
NE 555 timer, 356
  astable multivibrator 357
  monostable multivibrator 355
Noise immunity, CMOS 329
  TTL. 221, 329
Non-inverting amp. 249
NOR, function 301
  CMOS gate 328
  RTL gate 319
  TTL gate 321
NOT function 300
n—type 3, 18
Numeric display 48
Octal number 307
One-shot multivibrator 355
Op-amp. 271
  compensation 271
  open-loop gain 271
  slew rate 274
OR function 300
Oscillators, 367
  Clapp 367
  Colpitts 367
  criterion 364
  crystal 388
  feedback 364
  harmonic content 363
  Hartley 367
  LC 367
  negative resistance 386
  phase shift 378
  RC 374
  sine wave 290. 361
  tuned output 367
  Wienbridge 291, 374
Oscilloscope 91
Output circuit of Op-amp., 266
  complementary 268
  totem pole 267
Output impedance CE amp. 161
  differential amplifier 266
  emitter follower 207
  feedback amp. 217
  FET amp. 190
  Op-amp. 266
Parallel shift register 346
Parameters, 113
  driving point 118
  hybrid 127
  open circuit 115
  short circuit 115
  T 130
  transfer 115
Pauli exclusion principle 12
Peak inverse voltage, (PIV), of a diode
  bridge rectifier 434
  fullwave rectifier 411
  halfwave rectifier 407
Peak rectifier 34
Pentode 81
Phase margin 272
Phase response 137
Phase response of CE amp. 164
  high frequency 175
  low frequency 162
Photodiode 48
Photodiode amp. 286
Photoresist 108
Piezoelectric crystal 388
Pinch-off in FET 189
Planar technique 110
Plate resistance 201
pn, junction diode 20
  charge density 21
  forward bias 24
  reverse bias 24
Potential, barrier 20, 28
  hill 22
Power dissipation, CMOS gates 328
  TTL gates 328
Precision rectifier 288
Preparation of Silicon 104
Preset in FF 341 342
Propagation delay, 324
  CMOS 327
  Schottky TTL 325
  TTL 324
p-type 3
Pull-up resistor 323

Pulse generator, 396
  waveform 397
Purification of Germanium 103
Ramp signal generator 402
Rectification 27
Rectification, controlled 73, 96
Rectifiers 32
  bridge 434
  fullwave 407
  halfwave 411
  peak 34
Register, shift 333, 344
  left shift 346
  right shift 346
Regulation, line 438
  load 437
  voltage 40, 91, 436
Regulated power supply 436
Regulator chip μA-723 439
Reset in FF 334
Response, frequency 137, 154, 194, 204
  high pass 134, 291
  low pass 134, 291
  magnitude 137
  phase 136
Reverse saturation circuit 54
Richard-Dushman equation 76
Ripple counter 347
Ripple factor, fullwave 412
  halfwave 410
Roll-off characteristic of op-amp. 272
RTL gate circuits 319
  logic circuits 309
Sample & hold circuit 288
Saw-tooth waveform 400
Schottky barrier, diode 37
  transistor 325
Self bias in FET 187
Semiconductors, 3
  diode 27
  doped 3, 18
  extrinsic 3, 16
  intrinsic 3, 16
  n-type 3, 18
  p-type 3, 18
Sequential circuit 333
Series-series feedback 225, 236
Series-shunt feedback 225
Series transistor 438
Set in FF 334
Shift register, 333
  parallel 346
  serial 344
Short-circuit current limit 440
Shunt-series feedback 225
Shunt-shunt feedback 225, 226
Signal, analogue 4, 5
  digital 5
Silicon, 3
  controlled rectified (SCR) 70
  controlled switch (SCS) 70
  planar technique 110
Sinewave oscillator 290, 363
SiO_2 107
Slew rate 274
Solar cells 50
Source, 119
  current controlled 122
  ideal current 121
  ideal voltage 121
  voltage controlled 122
Space charge 21, 77
Speech 5
Square wave generator,
  op-amp. 390
  transistor 390
SR Flip-flop, 334, 355
  clocked 336
  using NAND 334
  using NOR 334
SSI, 4
Stability, biasing 145
  crystal oscillator feedback 242
  op-amp. 271
  oscillator 388
Stability of biasing 151
Stored base charge 320
Stray capacitance,
  op-amp. 273
  triodes 201
Substrate 107
Summing amp. 254
Super-β transistor 266
Sweep, boot-strap 402
  constant current 403
  frequency 402
  Miller 404
  waveforms 401
Switch, transistor 314
Synchronous operation, JK master
  slave FF. 341
  counter 353
Teleprinter spectral content 5
Television spectral content 5
Thermal runaway 148
Thermionic emission 76
Thyratron 96

Timers 354
Toggle, FF 343
Totempole circuit 267, 323
T-parameters 127
Transconductance
  FET 194
  vacuum tube 200
Transfer parameters 115
Transistors 3,50
  bipolar junction 51
  characteristics 57
  common base 56
  common collector 56
  common emitter 50
  current flow 56
  dissipation 58, 59
  field effect, junction 62
  insulated gate FET 66
  npn 52
  operating point 59
  pnp 52
  switch 314
  unijunction 69
Transition, frequency 177
  region 20
  time (op-amp.) 274
Transistor, cut-off 315
  saturation 316
Triangular wave generator 400
Triode, 78
  amplifier 202
Truth table, 299
  AND 298, 299
  D-FF 342
  EX-OR 302
  full adder 311
  half adder 310
  JK-FF 338
  JK master slave 341
  NAND 301
  NOR 302
  NOT 300
  OR 300
  SR-FF 333, 334
TTL gate circuit 321
  integrated circuit 321
  logic circuit 309
Tunnel diode, 41
  oscillator 386
Two port network 44
Unijunction transistor 64
Upper 3db frequency point,
  CE amp. 181
  FET amp. 199
Voltage follower 284
Voltage regulation 40, 91
Voltage regulator 436
V_{REF} 439
V_{SENSE} 440
Vacuum tubes 1, 3, 75
  CRT 82
  diode 24, 75
  pentode 76
  triode 76
  tubes 1, 3, 75
Valance band 13
Varactor diode 45
Valves 1
V_{BE} (cut-in) 317
V_{BE} (cut-off) 317
V_{BE} (sat) 317
V_{CE} (sat) 317
V-i characteristics of
  diode 27
  gas tube 91
  IGFET 66
  JFET 62
  SCR 70
  transistor 51
  thyratron 94
  unijunction transistor 69
  vacuum tubes 75
VLSI 4
Voltage doubler, 435
  full wave 435
  half wave 436
  quadrupler 437
  tripler 437
Wein-bridge oscillator 291
Zener diode 39
Zone melting 103

BASIC ELECTRONICS

M.N. FARUQUI
and
S.L. MASKARA

"Basic Electronics" is a textbook of electronics meant for students of all branches of engineering at the degree level. Beginning with physical principles of electronic devices it covers fundamentals of technology of the devices, analogue and digital circuits and their applications. Operational amplifiers and digital integrated circuits (ICs) have been introduced along with circuits using discrete devices. A sound foundation has been laid with an in-depth treatment of circuits using discrete devices. Most of the examples and applications are described using ICs. More emphasis has been given to the development of a conceptual understanding rather than a rigorous analysis. It will enable the students to appreciate electronic applications better. Some experiments along with instructions of how to carry them out have been suggested as a practical support to the theoretical understanding.

Electronics pervades almost all industrial instrumentation, consumer and entertainment industry, computers and communications. A conceptual exposure to electronics is essential for all engineers and scientists. This book would be useful for learning electronics through self study as well. An exposure to physics and mathematics at the higher secondary school level supplemented with some knowledge of electrical circuits is all that is required as a background. This book would also prepare students of electronics, computer and communication engineering for taking advanced level subjects in their specialisation subsequently.

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